

# TJA1124

## Quad LIN master transceiver

Rev. 1 — 8 May 2018

Product data sheet

## 1 General description

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The TJA1124 is a quad Local Interconnect Network (LIN) master channel device. It provides the interface between a LIN master protocol controller and the physical bus in a LIN network. Each of the four channels contains a LIN transceiver and LIN master termination. The TJA1124 is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1.

The transmit data streams generated by the LIN master protocol controller are converted by the TJA1124 into optimized bus signals shaped to minimize ElectroMagnetic Emission (EME). The LIN bus output pins are pulled HIGH via internal LIN master termination resistors. The receivers detect receive data streams on the LIN bus input pins and transfer them to the microcontroller via pins RXD1 to RXD4.

Power consumption is very low in Low Power mode. However, the TJA1124 can still be woken up via pins SLP and LIN1 to LIN4.

## 2 Features and benefits

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### 2.1 General

- Four LIN master channels in a single package:
  - LIN transceiver
  - LIN master termination consisting of a diode and a 1 k $\Omega$   $\pm$ 10 % resistor
- Compliant with:
  - LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A
  - ISO 17987-4:2016 (12 V LIN)
  - SAE J2602-1
- Very low current consumption in Low Power mode with wake-up via SLP or LIN pins
- Option to control an external voltage regulator via the INHN output
- Bus signal shaping optimized for baud rates up to 20 kBd
- VIO input for direct interfacing with 3.3 V and 5 V microcontrollers
- Passive behavior in unpowered state
- Undervoltage detection
- K-line compatible
- Leadless DHVQFN24 package (3.5 mm  $\times$  5.5 mm) supporting improved Automated Optical Inspection (AOI) capability

### 2.2 Protection

- Excellent ElectroMagnetic Immunity (EMI)



- Very high ESD robustness:  $\pm 6$  kV according to IEC61000-4-2 for pins LIN1 to LIN4 and BAT
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- TXD dominant timeout function
- LIN dominant timeout function
- Thermal protection

### 3 Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
TJA1124AHG <sup>[1]</sup>	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT 815-1
TJA1124BHG <sup>[2]</sup>			

[1] The LIN master termination of TJA1124AHG is enabled in Low Power mode.  
 [2] The LIN master termination of TJA1124BHG is disabled in Low Power mode

### 4 Block diagram

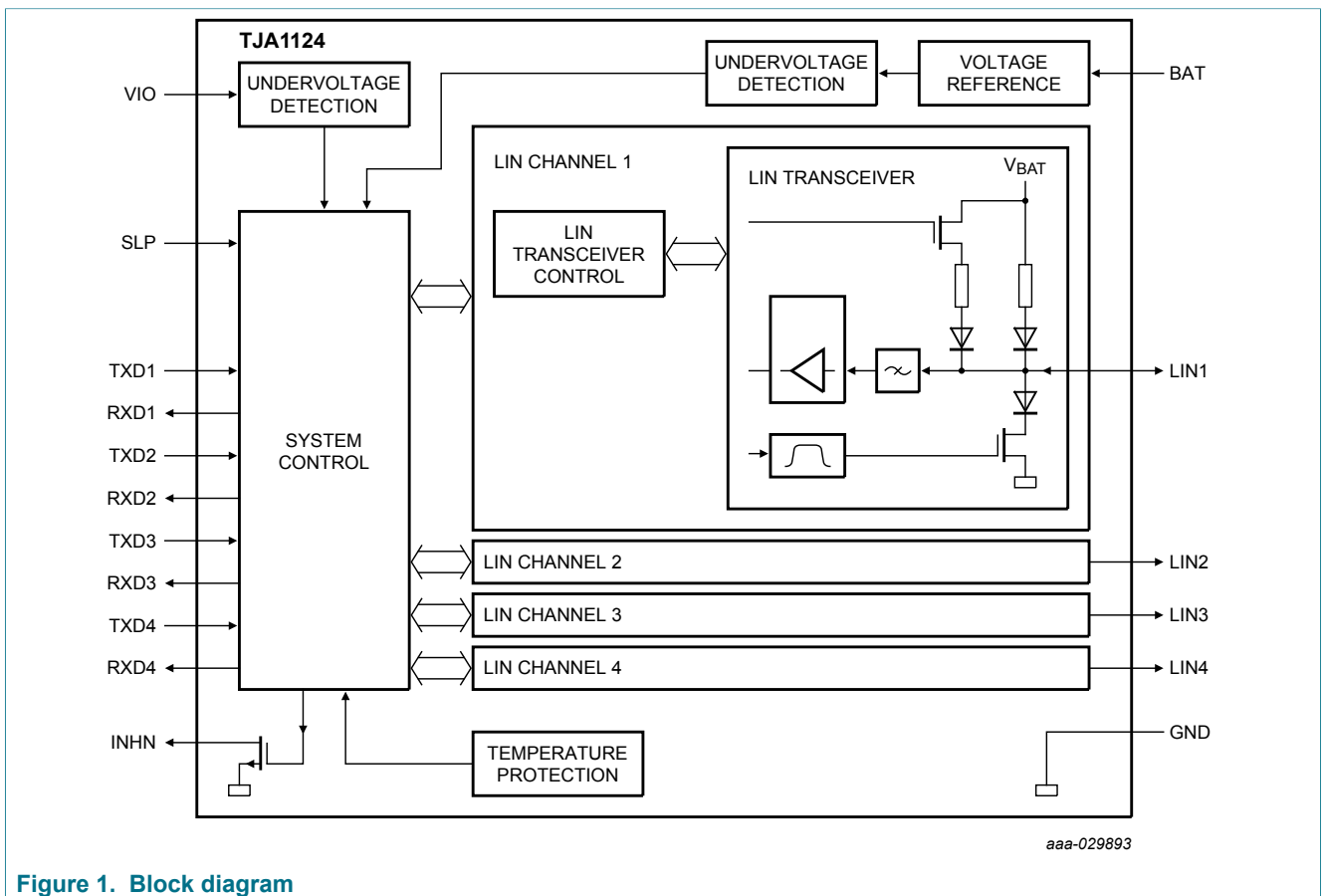


Figure 1. Block diagram

## 5 Pinning information

### 5.1 Pinning

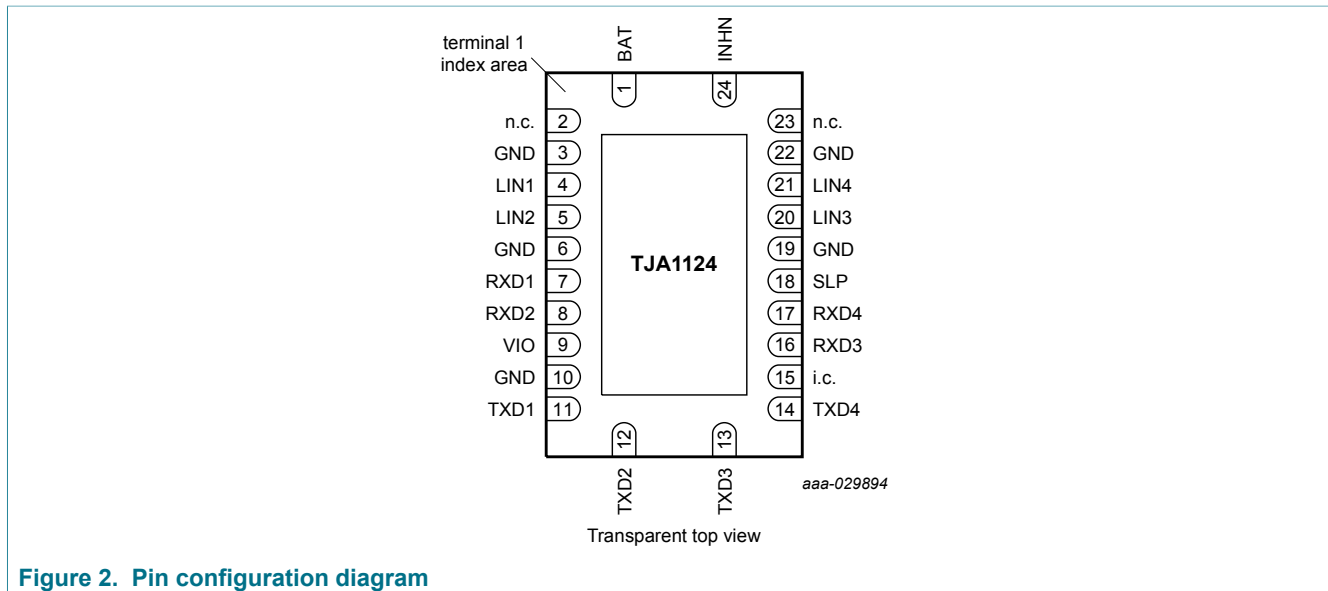


Figure 2. Pin configuration diagram

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin <sup>[1]</sup>	Description
BAT	1	battery supply
n.c.	2	not connected
GND	3	ground
LIN1	4	LIN bus line 1 input/output
LIN2	5	LIN bus line 2 input/output
GND	6	ground
RXD1	7	receive data output 1; active LOW after a wake-up event on LIN1
RXD2	8	receive data output 2; active LOW after a wake-up event on LIN2
VIO	9	supply voltage for I/O level adapter
GND	10	ground
TXD1	11	transmit data input 1
TXD2	12	transmit data input 2
TXD3	13	transmit data input 3
TXD4	14	transmit data input 4
i.c.	15	internally connected; should be connected to ground
RXD3	16	receive data output 3; active LOW after a wake-up event on LIN3

Symbol	Pin <sup>[1]</sup>	Description
RXD4	17	receive data output 4; active LOW after a wake-up event on LIN4
SLP	18	sleep control input; resets wake-up request on RXD
GND	19	ground
LIN3	20	LIN bus 3 input/output
LIN4	21	LIN bus 4 input/output
GND	22	ground
n.c.	23	not connected
INH	24	inhibit output for controlling an external voltage regulator; open-drain; active LOW

[1] For enhanced thermal and electrical performance, solder the exposed center pad of the DHVQFN24 package to board ground.

## 6 Functional description

The TJA1124 is the interface between the LIN master protocol controller and the physical bus in a LIN network. Each of its four channels incorporates a LIN transceiver and LIN master termination. According to the Open System Interconnect (OSI) model, this device comprises the LIN physical layer.

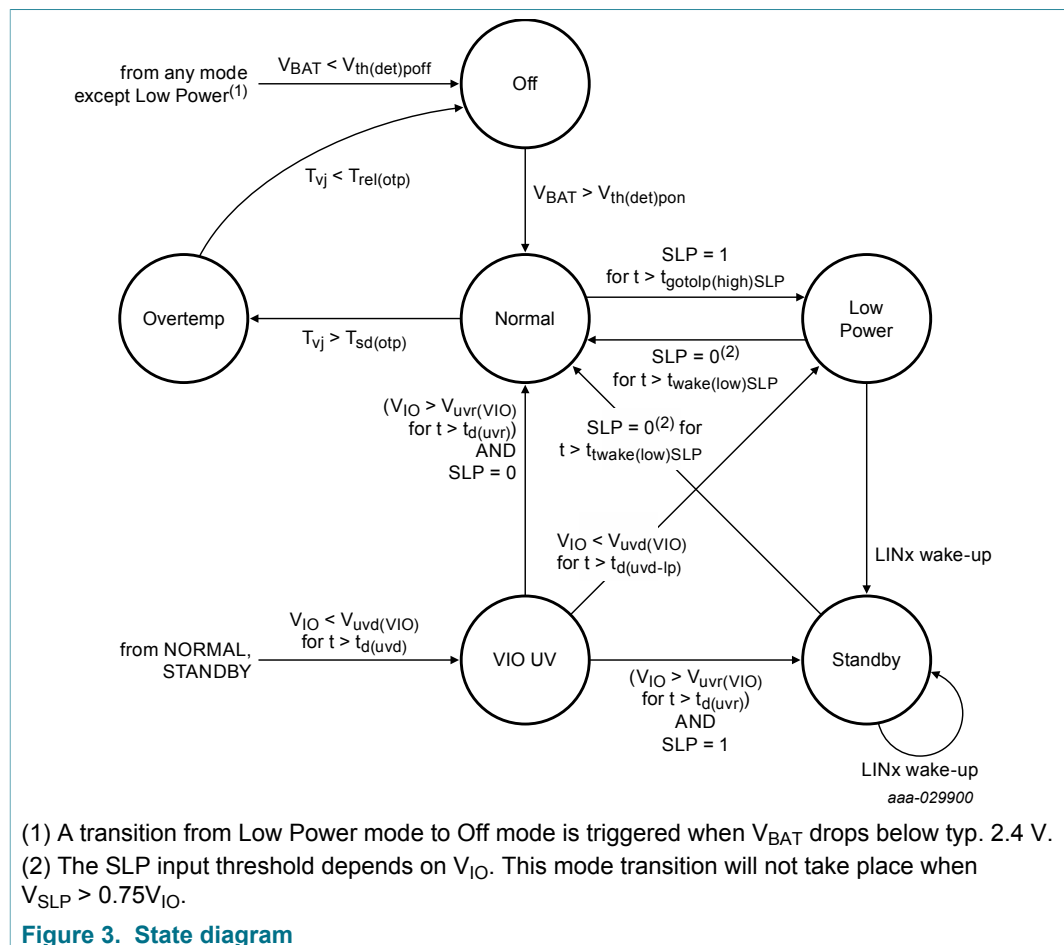
The TJA1124 is intended for, but not limited to, automotive LIN master applications with multiple LIN master channels. It provides excellent ElectroMagnetic Compatibility (EMC) performance.

### 6.1 LIN 2.x/SAE J2602 compliance

The TJA1124 is fully compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO 17987-4:2016 (12 V LIN) and SAE J2602-1.

### 6.2 Operating modes

The TJA1124 supports two main operating modes: Normal mode and Low Power mode. Additional battery supply undervoltage (Off), intermediate VIO undervoltage (VIO UV), intermediate wake-up signalling (Standby) and overtemperature protection (Overtemp) modes are supported. The TJA1124 state diagram is shown in [Figure 3](#).



### 6.2.1 Off mode

When the TJA1124 is in Off mode, all input signals are ignored and all output drivers are off. All pending LIN wake-up event flags are reset. The device is in a defined passive, low-power state in Off mode.

The TJA1124 switches to Off mode when the voltage on pin BAT drops below the power-off detection threshold,  $V_{th(det)poff}$ . When the TJA1124 is in Overtemp mode, it switches to Off mode when the junction temperature drops below  $T_{rel(otp)}$ .

### 6.2.2 Low Power mode

The TJA1124 consumes significantly less power in Low Power mode than in Normal mode. While current consumption is very low in Low Power mode, the TJA1124 can still detect remote wake-up events on pins LINx (see [Section 6.3.1](#)) and microcontroller wake-up events on pin SLP (see [Section 6.3.2](#)).

Pin INHN is set floating when the TJA1124 switches to Low Power mode.

A HIGH level on pin SLP in Normal mode lasting longer than  $t_{gotolp(high)SLP}$  initiates a transition to Low Power mode. The LIN transmit path is disabled when pin SLP is HIGH. The transition to Low Power mode takes up to  $t_{d(lp)}$ .

The TJA1124 switches from VIO UV mode to Low Power mode if the voltage on pin VIO remains below  $V_{uvd(VIO)}$  for longer than  $t_{d(uvd-lp)}$ .

### 6.2.3 Standby mode

In Standby mode, the LIN transmitter is off and the INHN output is LOW. The TJA1124 switches from Low Power mode to Standby mode when a remote wake-up is detected on one or more of the LIN pins (LIN1 to LIN4). The source(s) of a wake-up event(s) is indicated to the microcontroller by a LOW level on the respective RXD pin(s) (RXD1 to RXD4).

The remaining LIN channels are still able to detect remote wake-up events during and after the transition to Standby mode. The transition to Standby mode takes  $t_{init}$ .

The TJA1124 switches from VIO UV mode to Standby mode when the voltage on pin VIO remains above  $V_{uvr(VIO)}$  for longer than  $t_{d(uvr)}$  and pin SLP is HIGH.

### 6.2.4 Normal mode

The TJA1124 can transmit and receive data via the LIN bus in Normal mode.

The receiver detects a data stream on a LIN bus input pin (LIN1 to LIN4) and transfers it to the microcontroller via the associated RXD pin (RXD1 to RXD4): HIGH for a recessive level and LOW for a dominant level on the bus. The receiver has a supply-voltage related threshold with hysteresis and an integrated filter to suppress bus line noise.

The transmitter converts a transmit data stream, received from the protocol controller and detected on pin TXDx, into optimized bus signals. The optimized bus signals are shaped to minimize EME. The LINx bus output pin is pulled HIGH via an internal master termination resistor.

If pin SLP is pulled LOW for longer than  $t_{wake(low)SLP}$  while the TJA1124 is in Low Power or Standby mode, the LIN transceiver switches to Normal mode. The transition to Normal mode from Low Power or Off modes takes  $t_{init}$ .

The TJA1124 switches from VIO UV mode to Normal mode when the voltage on pin VIO remains above  $V_{uvr(VIO)}$  for longer than  $t_{d(uvr)}$  and pin SLP is LOW.

**6.2.5 VIO UV mode**

In VIO UV mode, the LINx outputs are recessive, the INHN output is LOW, the RXDx outputs are HIGH, and the digital inputs are ignored.

The TJA1124 switches from Normal or Standby mode to VIO UV mode when the voltage on pin VIO drops below the VIO undervoltage detection threshold,  $V_{uvd(VIO)}$ , for longer than  $t_{d(ugd)}$ .

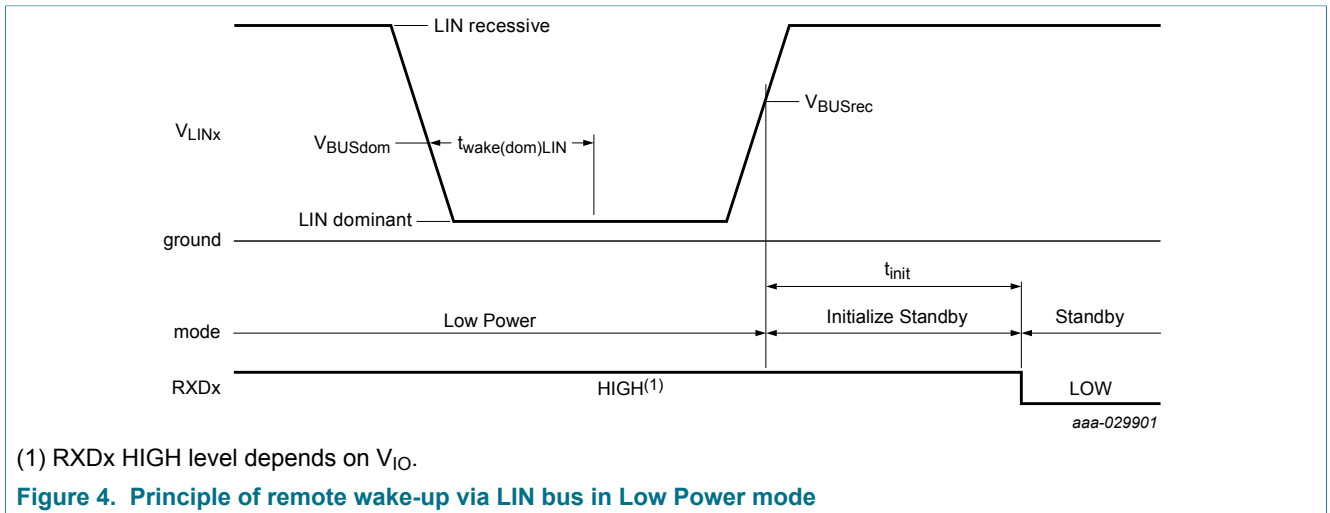
**6.2.6 Overtemp mode**

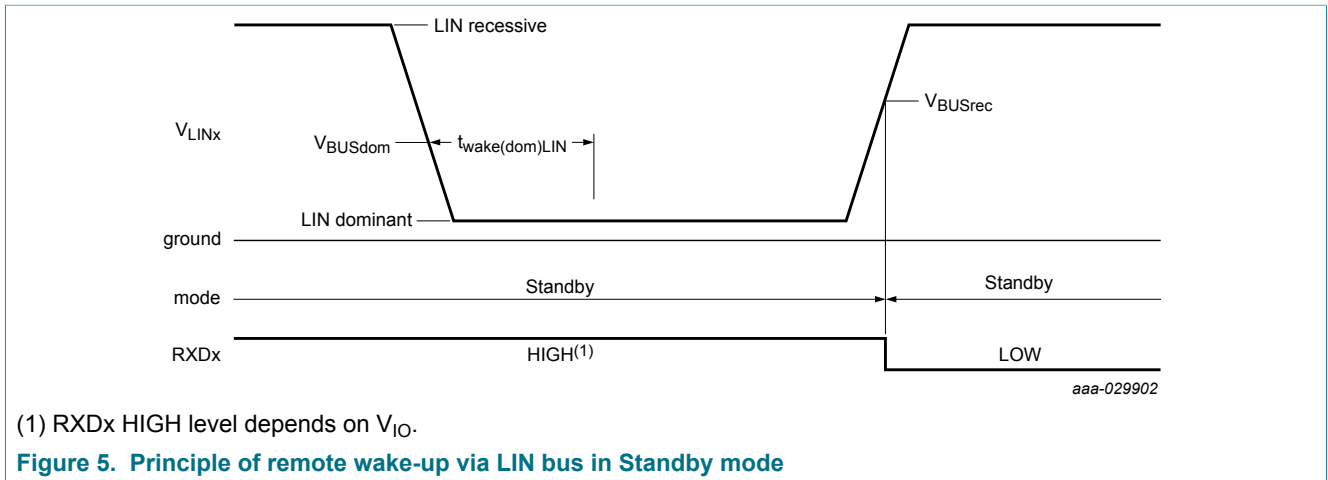
Overtemp mode prevents the TJA1124 from being damaged by excessive temperatures. If the junction temperature exceeds the shutdown threshold,  $T_{sd(otp)}$ , the thermal protection circuit disables the LIN channel output drivers and the LIN master pull-up resistors (see Section 6.8) and pending wake-up events are cleared.

**6.3 Device wake-up**

**6.3.1 Remote wake-up via the LIN bus**

The TJA1124 can detect remote LIN wake-up events in Low Power and Standby modes. A falling edge on pin LINx followed by a dominant level maintained for  $t_{wake(dom)LIN}$ , followed by a recessive level, is regarded as a remote wake-up request. The detection of a remote LIN wake-up event is signaled on pin RXDx (see Figure 4 and Figure 5).





(1) RXDx HIGH level depends on  $V_{IO}$ .

Figure 5. Principle of remote wake-up via LIN bus in Standby mode

### 6.3.2 Local wake-up via pin SLP

A LOW level on pin SLP lasting at least  $t_{wake(low)SLP}$  is interpreted as a local wake-up request.

### 6.4 Operation during automotive cranking pulses

The TJA1124 remains fully operational during automotive cranking pulses because it is specified down to  $V_{BAT} = 5\text{ V}$ .

### 6.5 Operation when supply voltage is outside specified operating range

If  $V_{BAT} > 28\text{ V}$  or  $V_{BAT} < 5\text{ V}$ , the TJA1124 may remain operational, but parameter values (as specified in Table 5 and Table 6) cannot be guaranteed.

If the voltage on pin BAT drops below the power-off detection threshold,  $V_{th(det)poff}$ , the TJA1124 switches to Off mode (see Section 6.2.1).

In Normal mode:

- If the input level on pin LINx is recessive, the respective receiver output on pin RXDx will be HIGH.
- If the input level on pin TXDx is HIGH, the respective LIN transmitter output on pin LINx will be recessive.

### 6.6 TXD dominant time-out function

Once a transmitter has been enabled, its TXD dominant timeout timer is started every time the associated TXD pin goes LOW. If the LOW state on TXDx persists for longer than the TXD dominant timeout time ( $t_{to(dom)TXD}$ ), the transmitter is disabled, releasing the bus line to recessive state. The TXD dominant timeout timer is reset when pin TXDx goes HIGH.



### 6.7 LIN dominant timeout function

Each LIN channel has an associated LIN dominant timeout function. This function switches off the LIN master termination resistor,  $R_{master}$  or  $R_{master(lp)}$ , if the LIN bus level remains dominant for longer than  $t_{to(dom)LIN}$ . LIN termination resistor  $R_{slave}$  remains active as pull-up when  $R_{master}$  or  $R_{master(lp)}$  is switched off.

Once the LIN bus level is recessive again, the LIN master termination is switched on and the LIN dominant timeout timer is reset.

### 6.8 LIN master pull-up

In Normal and Standby modes, the integrated LIN master termination,  $R_{master}$ , is a trimmed 1 kΩ pull-up with a tolerance of ±10 %.

In Low Power mode, the integrated LIN pull-up depends on the TJA1124 variant. In the TJA1124A, an untrimmed LIN master termination,  $R_{master(lp)}$ , is enabled. In the TJA1124B, LIN master termination is disabled and the LINx pins are terminated with the LIN termination resistor,  $R_{slave}$ .

### 6.9 Fail-safe features

A loss of power (pin BAT or GND) has no impact on the bus lines or on the microcontroller interface pins. When the battery supply is lost, reverse current  $I_{BUS\_NO\_BAT}$  flows from the bus into pins LINx. When the ground connection is lost, current  $I_{BUS\_NO\_GND}$  continues to flow from BAT to LINx via an integrated LIN termination resistor,  $R_{slave}$ . The current path through the LIN master termination is disabled.

The output drivers on the LINx pins are protected against overtemperature conditions (see [Section 6.2.6](#)).

## 7 Limiting values

**Table 3. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to pin GND; unless otherwise specified. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_x$	voltage on pin x	pins BAT, INHN	-0.3	+43	V
		pin VIO	-0.3	+6	V
		pins SLP, RXDx, TXDx	-0.3	$V_{IO} + 0.3$	V
		pins LINx with respect to any other pin	-43	+43	V
$I_{INHN}$	input current on pin INHN		-	3	mA
$V_{trt}$	transient voltage on pin BAT	on pin BAT with inverse-polarity protection diode and 22 μF capacitor to ground on pins LIN1, LIN2, LIN3, LIN4 coupled via 1 nF capacitor	[1] -150	+100	V
$V_{ESD}$	electrostatic discharge voltage	IEC61000-4-2	[2]		
		on pins LIN1, LIN2, LIN3 and LIN4; on pin BAT with capacitor	-6	+6	kV

Symbol	Parameter	Conditions	Min	Max	Unit
		Human Body Model (HBM)			
		on pins LIN1, LIN2, LIN3 and LIN4	-6	+6	kV
		on pin BAT, INHN	-4	+4	kV
		on pins SLP, RXDx, TXDx	-2	+2	kV
		Charged Device Model			
		all pins	-500	+500	V
T <sub>vj</sub>	virtual junction temperature		-40	+150	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C

- [1] According to ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.
- [2] Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.
- [3] According to AEC-Q100-002; equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
- [4] BAT and VIO connected to GND, emulating the application circuit.
- [5] According to AEC-Q100-011.
- [6] Junction temperature in accordance with IEC 60747-1. An alternative definition is:  $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ , where  $R_{th(vj-a)}$  is a fixed value. The rating for T<sub>vj</sub> limits the allowable combinations of power dissipation (P) and ambient temperature (T<sub>amb</sub>).

## 8 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	DHVQFN24; four-layer board	51	K/W

- [1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer

## 9 Static characteristics

Table 5. Static characteristics

T<sub>vj</sub> = -40 °C to +150 °C; V<sub>BAT</sub> = 5.0 V to 28 V; V<sub>IO</sub> = 2.97 V to 5.5 V; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V<sub>BAT</sub> = 12 V; unless otherwise specified [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V <sub>BAT</sub>	battery supply voltage	operating range	5	-	28	V
V <sub>IO</sub>	supply voltage for I/O level adapter	operating range	2.97	-	5.5	V
I <sub>BAT</sub>	battery supply current	TJA1124A; Low Power mode; [2] V <sub>SLP</sub> = V <sub>IO</sub> ; V <sub>LINx</sub> = V <sub>BAT</sub> ; -40 °C < T <sub>vj</sub> < 85 °	-	7.3	17.2	μA
		TJA1124B; Low Power mode; [2] V <sub>SLP</sub> = V <sub>IO</sub> ; V <sub>LINx</sub> = V <sub>BAT</sub> ; -40 °C < T <sub>vj</sub> < 85 °	-	6	15	μA
		Normal mode; bus recessive; V <sub>TXDx</sub> = V <sub>IO</sub> ; V <sub>SLP</sub> = 0 V; V <sub>LINx</sub> = V <sub>BAT</sub>	-	12	22	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Normal mode; bus dominant; $V_{LINx} = V_{SLP} = 0\text{ V}$ ; $V_{BAT} = 12\text{ V}$	-	66	87	mA
$I_{IO}$	supply current on pin VIO	Low Power mode; $-40\text{ °C} < T_{Vj} < 85\text{ °C}$	-	6	9	$\mu\text{A}$
		Normal mode	-	-	1	mA
<b>Supply undervoltage; pins BAT and VIO</b>						
$V_{th(det)poff}$	power-off detection threshold voltage		4.0	-	4.51	V
$V_{th(det)pon}$	power-on detection threshold voltage		4.25	-	4.77	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage		200	-	-	mV
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO		2.7	2.8	2.9	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin VIO		2.8	2.9	3.1	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin VIO		50	-	-	mV
<b>Sleep control input and LIN transmit data inputs: SLP and TXDx; all measurements taken in Normal mode</b>						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.035V_{IO}$	-	-	V
$R_{pu}$	pull-up resistance	on pin SLP	38	60	88	k $\Omega$
		on pins TXDx; $V_{TXD} > 0.75 V_{IO}$	38	60	88	k $\Omega$
$R_{pd}$	pull-down resistance	on pins TXDx; $V_{TXD} < 0.25 V_{IO}$	38	60	88	k $\Omega$
<b>LIN receive data outputs; pins RXDx; all measurements taken in Normal mode</b>						
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -4\text{ mA}$	$V_{IO} - 0.4$			V
$V_{OL}$	LOW-level output voltage	$I_{OL} = 4\text{ mA}$			0.4	V
$R_{pu}$	pull-up resistance		38	60	88	k $\Omega$
$I_{LO(off)}$	off-state output leakage current	$V_O = 0\text{ V to } V_{IO}$	-5		+5	$\mu\text{A}$
<b>Inhibit output; pin INHN</b>						
$V_{OL}$	LOW-level output voltage	$I_{OL} = 0.2\text{ mA}$			0.4	V
$I_{LO(off)}$	off-state output leakage current		-5		+5	$\mu\text{A}$
<b>LIN bus line; pins LIN1, LIN2, LIN3, LIN4</b>						
$V_{O(dom)}$	dominant output voltage	Normal mode; $V_{BAT} = 7.0\text{ V}$	-	-	1.4	V
		Normal mode; $V_{BAT} = 18.0\text{ V}$	-	-	3.6	V
$I_{BUS\_LIM}$	current limitation for driver dominant state	$V_{BAT} = 18\text{ V}$ ; $V_{LINx} = 18\text{ V}$ ; LIN driver on; $R_{master}$ off	40	-	200	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>BUS_PAS_dom</sub>	receiver dominant input leakage current including pull-up resistor	V <sub>BAT</sub> = 12 V; V <sub>LINx</sub> = 0 V; LIN driver off; R <sub>master</sub> off	-1	-	-	mA
		V <sub>BAT</sub> = 28 V; V <sub>LINx</sub> = 0 V; LIN driver off; R <sub>master</sub> off	-1.5	-	-	mA
I <sub>BUS_PAS_rec</sub>	receiver recessive input leakage current	5 V < V <sub>BAT</sub> < 18 V; 5 V < V <sub>LINx</sub> < 18 V; V <sub>LINx</sub> ≥ V <sub>BAT</sub> ; LIN driver off	-	-	20	μA
		18 V < V <sub>BAT</sub> < 28 V; 18 V < V <sub>LINx</sub> < 28 V; V <sub>LINx</sub> ≥ V <sub>BAT</sub> ; LIN driver off	-	-	30	μA
I <sub>BUS_NO_GND</sub>	loss-of-ground bus current	V <sub>BAT</sub> = 12 V; V <sub>GND</sub> = V <sub>BAT</sub> ; 0 V < V <sub>LINx</sub> < 18 V <sup>[2]</sup>	-1	-	+1	mA
		V <sub>BAT</sub> = 12 V; V <sub>GND</sub> = V <sub>BAT</sub> ; 0 V < V <sub>LINx</sub> < 28 V <sup>[2]</sup>	-1.5	-	+1.5	mA
I <sub>BUS_NO_BAT</sub>	loss-of-battery bus current	V <sub>BAT</sub> = 0 V; 0 V < V <sub>LINx</sub> < 28 V <sup>[2]</sup>	-	-	30	μA
V <sub>BUSdom</sub>	receiver dominant state		-	-	0.4V <sub>BAT</sub>	V
V <sub>BUSrec</sub>	receiver recessive state		0.6V <sub>BAT</sub>	-	-	V
V <sub>BUS_CNT</sub>	receiver center voltage	Normal mode; V <sub>BUS_CNT</sub> = (V <sub>th_rec</sub> + V <sub>th_dom</sub> ) / 2; 7 V ≤ V <sub>BAT</sub> < 28 V <sup>[3]</sup>	0.475V <sub>BAT</sub>	0.5V <sub>BAT</sub>	0.525V <sub>BAT</sub>	V
		Normal mode; V <sub>BUS_CNT</sub> = (V <sub>th_rec</sub> + V <sub>th_dom</sub> ) / 2; 5 V < V <sub>BAT</sub> < 7 V	0.45V <sub>BAT</sub>	0.5V <sub>BAT</sub>	0.55V <sub>BAT</sub>	V
		Low Power mode; V <sub>BUS_CNT</sub> = (V <sub>th_rec</sub> + V <sub>th_dom</sub> ) / 2	0.47V <sub>BAT</sub>	0.5V <sub>BAT</sub>	0.54V <sub>BAT</sub>	V
V <sub>HYS</sub>	receiver hysteresis voltage	V <sub>HYS</sub> = (V <sub>th_rec</sub> - V <sub>th_dom</sub> ) <sup>[3]</sup>	-	-	0.175V <sub>BAT</sub>	V
V <sub>SerDiode</sub>	voltage drop at the serial diodes	in pull-up path with R <sub>master</sub> ; I <sub>SerDiode</sub> = 12 mA <sup>[2]</sup>	0.4	-	1.0	V
		in pull-up path with R <sub>slave</sub> ; I <sub>SerDiode</sub> = 0.9 mA <sup>[2]</sup>	0.4	-	1.0	V
R <sub>master</sub>	master resistance	Normal mode; including R <sub>slave</sub>	900	1000	1100	Ω
R <sub>master(lp)</sub>	low -power master resistance	Low Power mode; including R <sub>slave</sub>	900	1200	1500	Ω
R <sub>slave</sub>	slave resistance	R <sub>master</sub> off	20	30	60	kΩ
C <sub>LIN</sub>	capacitance on pin LINx	<sup>[2]</sup>	-	-	20	pF
<b>Thermal shutdown</b>						
T <sub>sd(otp)</sub>	overtemperature protection shutdown temperature	<sup>[2]</sup>	150	165	179	°C
T <sub>rel(otp)</sub>	overtemperature protection release temperature	<sup>[2]</sup>	122	137	150	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.  
 [2] Not tested in production; guaranteed by design.  
 [3] V<sub>th\_dom</sub>: receiver threshold of the recessive to dominant LIN bus edge. V<sub>th\_rec</sub>: receiver threshold of the dominant to recessive LIN bus edge.

## 10 Dynamic characteristics

**Table 6. Dynamic characteristics**

$T_{vj} = -40\text{ °C to }+150\text{ °C}$ ;  $V_{BAT} = 5.0\text{ V to }28\text{ V}$ ;  $V_{IO} = 2.97\text{ V to }5.5\text{ V}$ ; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at  $V_{BAT} = 12\text{ V}$ ; unless otherwise specified <sup>[1]</sup>

Symbols	Parameter	Conditions	Min	Typ	Max	Unit	
Duty cycles; pins LIN1, LIN2, LIN3, LIN4							
δ1	duty cycle 1	$V_{th(rec)(max)} = 0.744 \times V_{BAT}$ ; $V_{th(dom)(max)} = 0.581 \times V_{BAT}$ ; $t_{bit} = 50\ \mu\text{s}$ ; $V_{BAT} = 7\text{ V to }28\text{ V}$	[2] [3] [4]	0.396	-	-	
		$V_{th(rec)(max)} = 0.744 \times V_{BAT}$ ; $V_{th(dom)(max)} = 0.581 \times V_{BAT}$ ; $t_{bit} = 50\ \mu\text{s}$ ; $V_{BAT} = 5\text{ V to }7\text{ V}$	[2] [3] [4]	0.37	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)} = 0.442 \times V_{BAT}$ ; $V_{th(dom)(min)} = 0.284 \times V_{BAT}$ ; $t_{bit} = 50\ \mu\text{s}$ ; $V_{BAT} = 7.6\text{ V to }28\text{ V}$	[2] [3] [4]	-	-	0.581	
		$V_{th(rec)(min)} = 0.442 \times V_{BAT}$ ; $V_{th(dom)(min)} = 0.284 \times V_{BAT}$ ; $t_{bit} = 50\ \mu\text{s}$ ; $V_{BAT} = 5.6\text{ V to }7.6\text{ V}$	[2] [3] [4]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)} = 0.778 \times V_{BAT}$ ; $V_{th(dom)(max)} = 0.616 \times V_{BAT}$ ; $t_{bit} = 96\ \mu\text{s}$ ; $V_{BAT} = 7\text{ V to }28\text{ V}$	[2] [3] [4]	0.417	-	-	
		$V_{th(rec)(max)} = 0.778 \times V_{BAT}$ ; $V_{th(dom)(max)} = 0.616 \times V_{BAT}$ ; $t_{bit} = 96\ \mu\text{s}$ ; $V_{BAT} = 5\text{ V to }7\text{ V}$	[2] [3] [4]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)} = 0.389 \times V_{BAT}$ ; $V_{th(dom)(min)} = 0.251 \times V_{BAT}$ ; $t_{bit} = 96\ \mu\text{s}$ ; $V_{BAT} = 7.6\text{ V to }28\text{ V}$	[2] [3] [4]	-	-	0.590	
		$V_{th(rec)(min)} = 0.389 \times V_{BAT}$ ; $V_{th(dom)(min)} = 0.251 \times V_{BAT}$ ; $t_{bit} = 96\ \mu\text{s}$ ; $V_{BAT} = 5.6\text{ V to }7.6\text{ V}$	[2] [3] [4]	-	-	0.590	
LIN receiver; pins LIN1, LIN2, LIN3, LIN4							
$t_{rx\_pd}$	receiver propagation delay	rising and falling edge; $7\text{ V} \leq V_{BAT} < 28\text{ V}$	[4]	-	-	6	$\mu\text{s}$
		rising and falling edge; $5\text{ V} < V_{BAT} < 7\text{ V}$		-	-	6.5	$\mu\text{s}$
$t_{rx\_sym}$	receiver propagation delay symmetry	rising edge with respect to falling edge	[4]	-2	-	+2	$\mu\text{s}$
$t_{wake(dom)LIN}$	LIN dominant wake-up time			30	80	150	$\mu\text{s}$
$t_{to(dom)LIN}$	LIN dominant time-out time	timer started at falling edge on LINx		17.5	20	23.5	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	timer started at falling edge on TXDx		6	-	10	ms
Mode transition							
$t_{wake(low)SLP}$	sleep LOW wake-up timeout time	for wake-up from Low Power or Standby to Normal mode		1.75	-	4.65	$\mu\text{s}$

Symbols	Parameter	Conditions	Min	Typ	Max	Unit
$t_{\text{tgotolp(high)SLP}}$	sleep HIGH to low power time	for transition form Normal to Low Power mode	5.2	6	6.7	$\mu\text{s}$
$t_{\text{init}}$	initialization time	Normal and Standby modes	-	-	1	ms
$t_{\text{d(lp)}}$	low power mode delay time		-	-	2	ms
$t_{\text{d(uvd-lp)}}$	delay time from VIO UV to low power mode		175	-	225	ms
$t_{\text{d(uvd)}}$	undervoltage detection delay time		5	-	10	$\mu\text{s}$
$t_{\text{d(uvr)}}$	undervoltage recovery delay time		5	-	10	$\mu\text{s}$

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2]  $\delta 1, \delta 3 = \frac{t_{\text{bus(rec)min}}}{2 \times t_{\text{bit}}}$ ;  $\delta 2, \delta 4 = \frac{t_{\text{bus(rec)max}}}{2 \times t_{\text{bit}}}$

[3] Bus load conditions:  $R_{\text{master}} = \text{off}$ ;  $C_{\text{LIN}} = 1 \text{ nF}$  and  $R_{\text{LIN}} = 1 \text{ k}\Omega$ ;  $C_{\text{LIN}} = 6.8 \text{ nF}$  and  $R_{\text{LIN}} = 660 \Omega$ ;  $C_{\text{LIN}} = 10 \text{ nF}$  and  $R_{\text{LIN}} = 500 \Omega$ . See timing test circuit in Fig. 9.

[4] See timing diagram in Fig. 10.

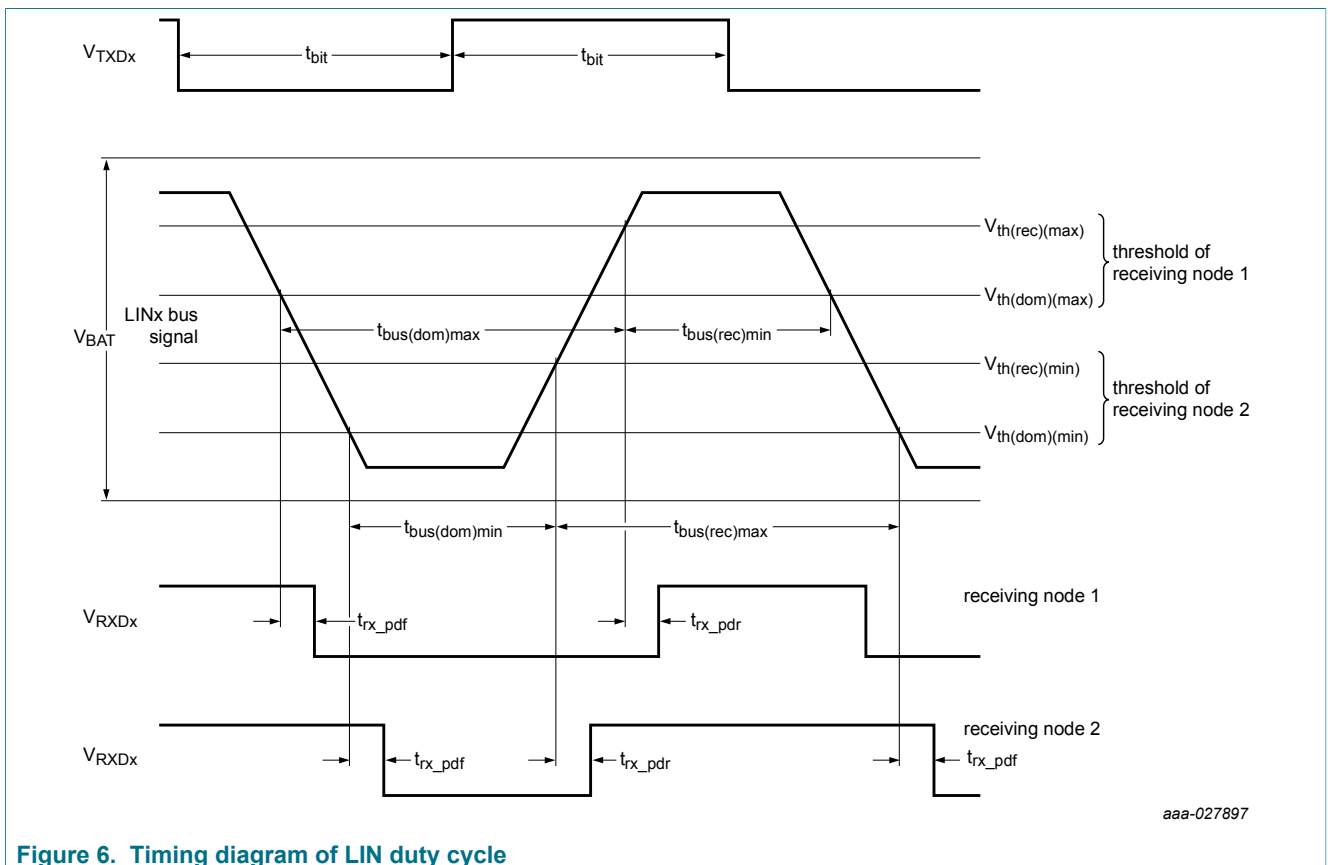


Figure 6. Timing diagram of LIN duty cycle

## 11 Application information

### 11.1 Application diagram

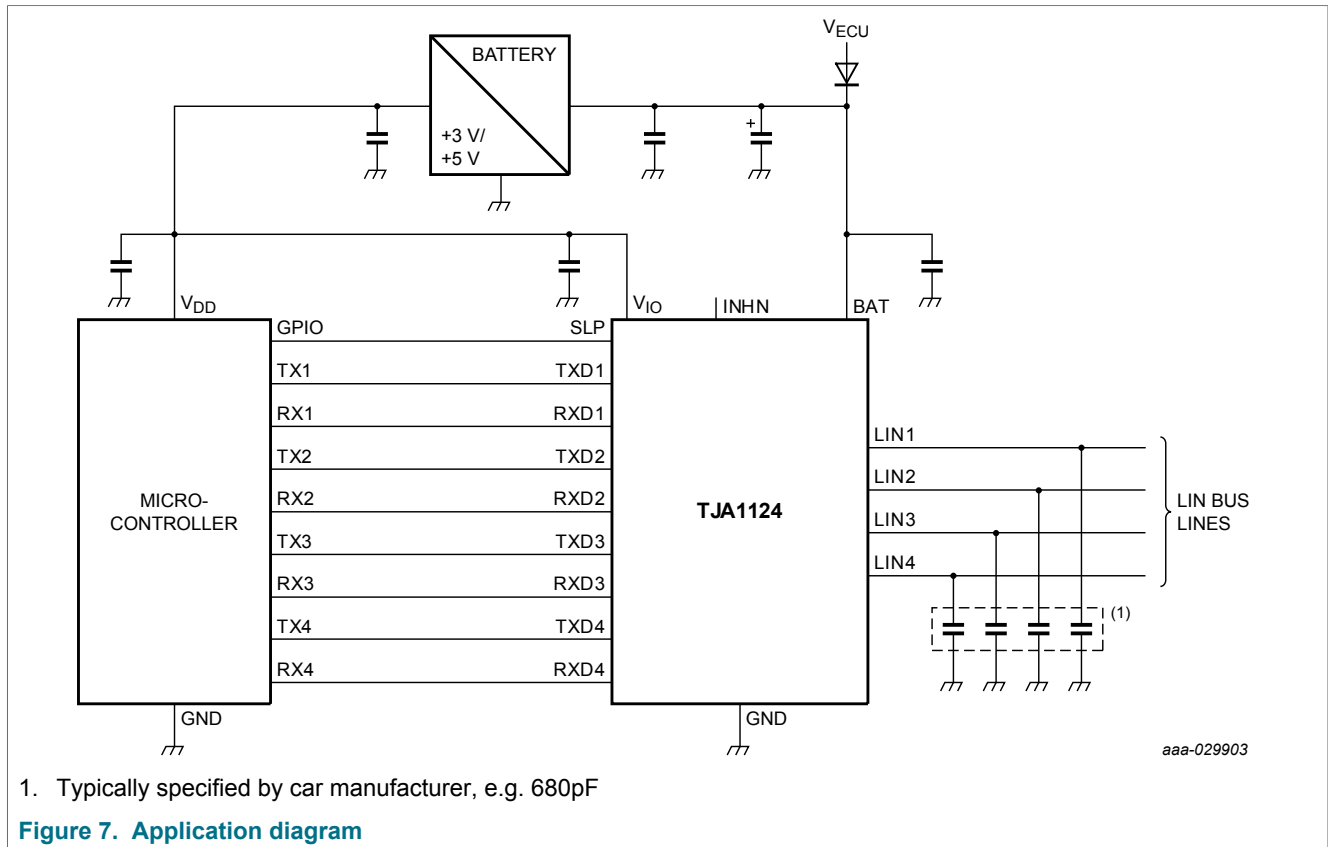


Figure 7. Application diagram

## 11.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 7. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LINx	no capacitor connected to LINx pin	±8	kV
	220 pF capacitor connected to LINx pin	±8	kV
BAT	22 µF and 100 nF capacitors connected to pin BAT	> 15	kV

## 12 Test information

### 12.1 Quality information

After product release this product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 - *Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.



13 Package outline

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

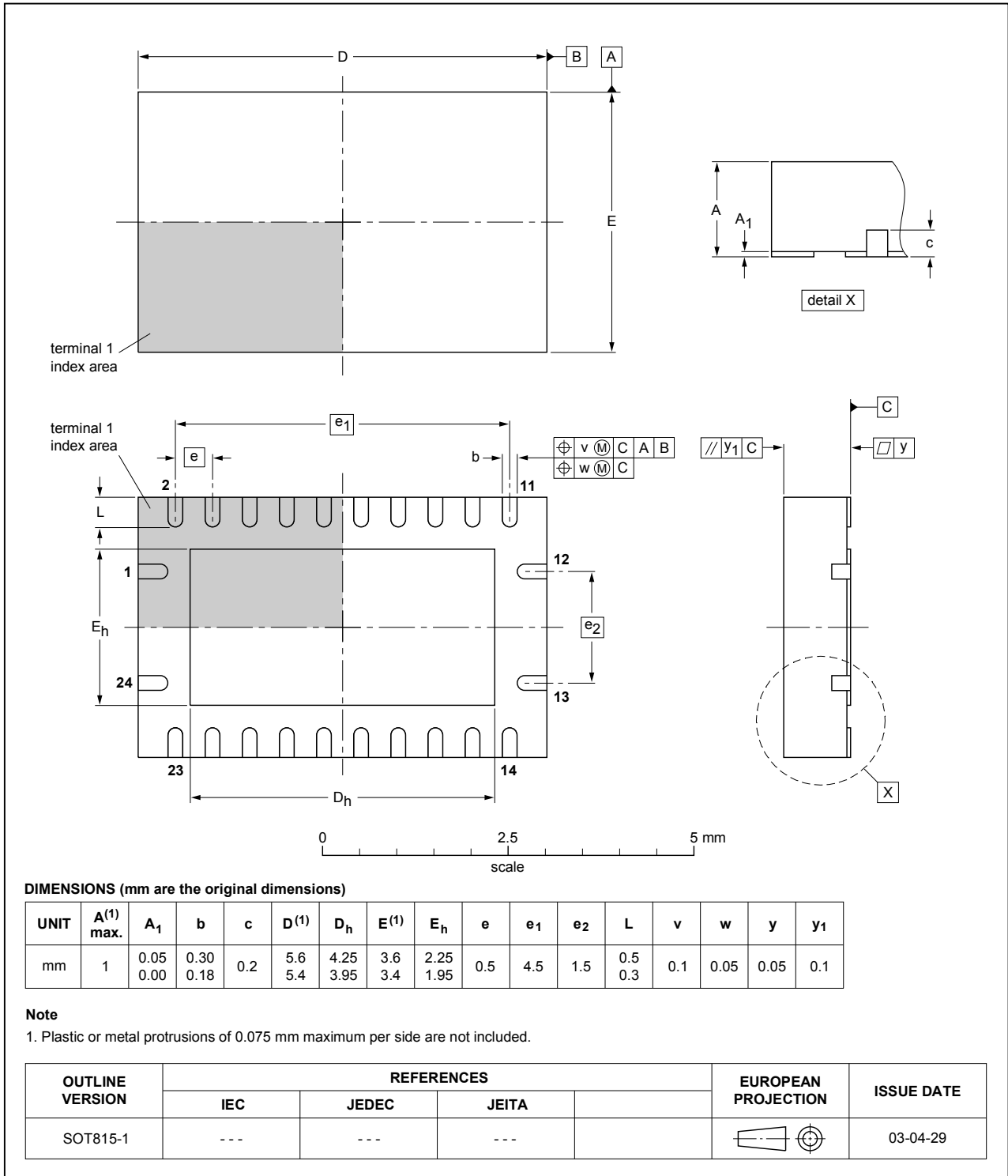


Figure 8. Package outline DHVQFN24

## 14 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 9](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [Table 9](#).

**Table 8. SnPb eutectic process (from J-STD-020C)**

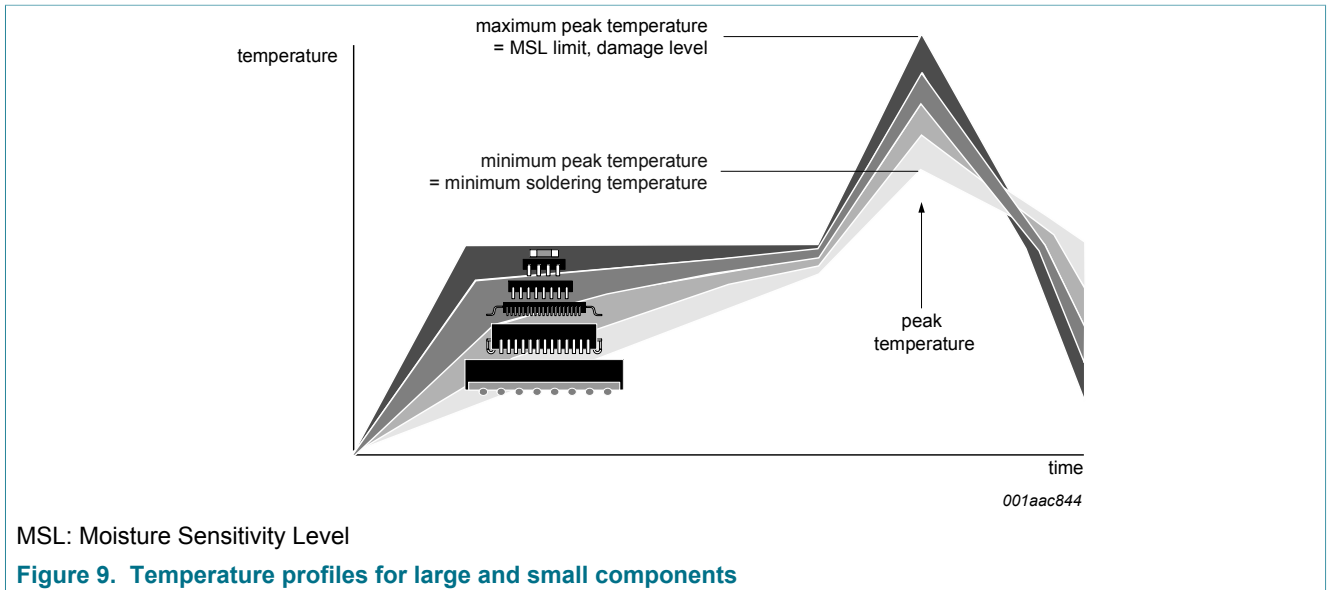
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	350
< 2.5	235	220
2.5	220	220

**Table 9. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	>2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 9](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 16 Soldering of DHVQFN packages

Section 15 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application notes:

- AN10365 “Surface mount reflow soldering description”
- AN10366 “HVQFN application information”

## 17 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1124 v.1	20180508	Product data sheet	-	-

## 18 Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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