

Kinetis V Series KV10 and KV11, 128/64 KB Flash

75 MHz Cortex-M0+ Based Microcontroller

The Kinetis V Series KV11x MCU family is built on Arm® Cortex®-M0+ core and enabled by innovative 90nm thin film storage (TFS) flash process technology. The KV11x is an extension of the existing KV10x family providing increased memory, higher pin count, additional FTMs and a FlexCAN serial interface.

- Dual 16-bit ADCs sampling at up to 1.2 MS/s in 12-bit mode
- Highly accurate and flexible motor control timers
- Ideal for industrial motor control applications, inverters, and low-end power conversion applications

Performance

- Up to 75 MHz Arm Cortex-M0+ based core

Memories and memory interfaces

- Up to 128 KB of program flash memory
- Up to 16 KB of RAM

System peripherals

- Nine low-power modes to provide power optimization based on application requirements
- 8-channel DMA controller
- SWD interface and Micro Trace buffer
- Bit Manipulation Engine (BME)
- External watchdog timer
- Advanced independent clocked watchdog
- Memory Mapped Divide and Square Root (MMDV SQ) module

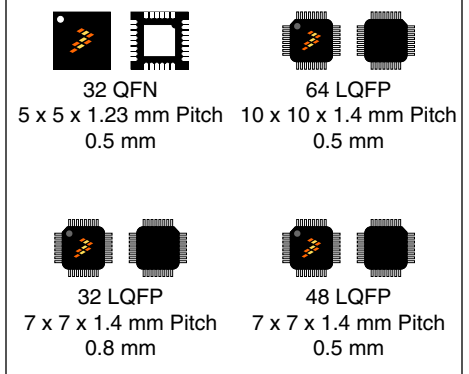
Clocks

- 32-40 kHz or 4-32 MHz external crystal oscillator
- Multipurpose clock generator (MCG) with frequency-locked loop referencing either internal or external reference clock

Security and integrity modules

- 80-bit unique identification (ID) number per chip
- Hardware CRC module

MKV11Z128VXX7
MKV11Z64VXX7
MKV10Z64VXX7
MKV10Z128VXX7



Communication interfaces

- One 16-bit SPI module
- One I2C module
- Two UART modules
- One FlexCAN module¹

Timers

- Programmable delay block
- Two 6-channel FlexTimers (FTM) for motor control/general purpose applications
- Four 2-channel FlexTimers (FTM) with quadrature decoder functionality
- 16-bit low-power timer (LPTMR)

Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

Analog modules

- Two 16-bit SAR ADCs
- 12-bit DAC
- Two analog comparators (ACMP) containing a 6-bit DAC and programmable reference input

Human-machine interface

- General-purpose I/O

1. Available only on KV11 parts

Ordering Information

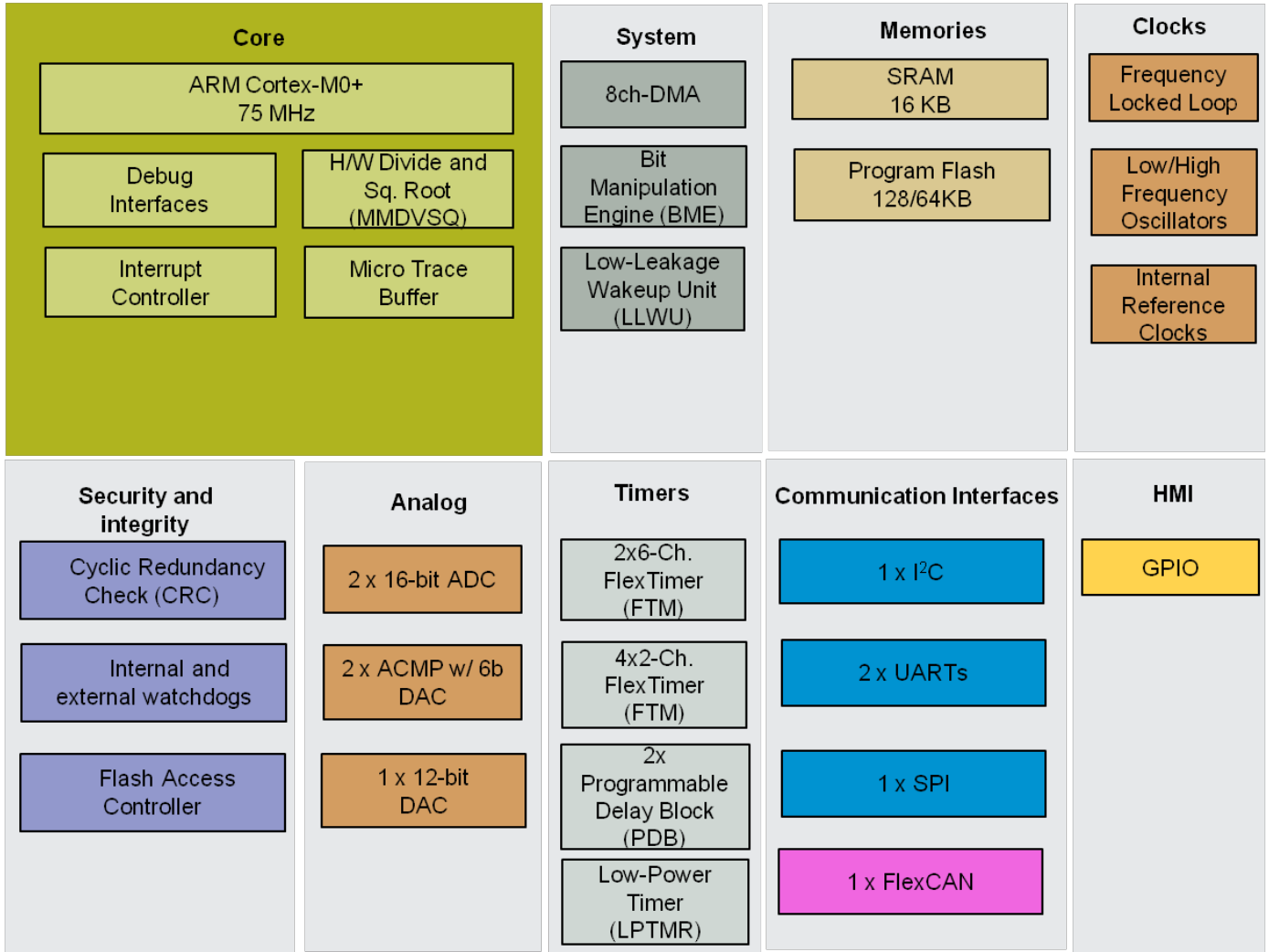
| Part Number ¹ | Memory | | FlexCAN | Maximum number of I/O's |
|----------------------------|------------|-----------|---------|-------------------------|
| | Flash (KB) | SRAM (KB) | | |
| MKV11Z128VLH7 | 128 | 16 | Yes | 46 |
| MKV11Z128VLF7 | 128 | 16 | Yes | 35 |
| MKV11Z128VLC7 ² | 128 | 16 | Yes | 26 |
| MKV11Z128VFM7 | 128 | 16 | Yes | 26 |
| MKV11Z64VLH7 | 64 | 16 | Yes | 46 |
| MKV11Z64VLF7 | 64 | 16 | Yes | 35 |
| MKV11Z64VLC7 ² | 64 | 16 | Yes | 26 |
| MKV11Z64VFM7 | 64 | 16 | Yes | 26 |
| MKV10Z64VLH7 | 64 | 16 | No | 46 |
| MKV10Z64VLF7 | 64 | 16 | No | 35 |
| MKV10Z64VLC7 ² | 64 | 16 | No | 26 |
| MKV10Z64VFM7 | 128 | 16 | No | 26 |
| MKV10Z128VLH7 | 128 | 16 | No | 46 |
| MKV10Z128VLF7 | 128 | 16 | No | 35 |
| MKV10Z128VLC7 ² | 128 | 16 | No | 26 |
| MKV10Z128VFM7 | 128 | 16 | No | 26 |

1. To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.
2. The 32-pin LQFP package supporting this part number is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit <http://www.nxp.com/KPYW> for more details.

Related Resources

| Type | Description | Resource |
|------------------|--|---|
| Product Selector | The Product Selector is a web-based tool to assist in selecting the MCU product for your application. | Product Selector |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. | KV10PB ¹ |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. | KV10P48M75RM ¹ |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. | This document |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. | <ul style="list-style-type: none"> • KV10Z_1N81H¹ • KINETIS_V_0N63P¹ |
| Package drawing | Package dimensions are provided in package drawings. | <ul style="list-style-type: none"> • QFN 32-pin: 98ASA00473D¹ • LQFP 32-pin: 98ASH70029A¹ • LQFP 48-pin: 98ASH00962A¹ • LQFP 64-pin: 98ASS23234W¹ |

1. To find the associated resource, go to <http://www.nxp.com> and perform a search using this term.



LEGEND ■ Not available on all parts. See ordering information table.

Figure 1. KV11 block diagram

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1 Ratings

1.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T _{STG} | Storage temperature | -55 | 150 | °C | 1 |
| T _{SDR} | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-------|-------|------|-------|
| V _{HBM} | Electrostatic discharge voltage, human-body model | -2000 | +2000 | V | 1 |
| V _{CDM} | Electrostatic discharge voltage, charged-device model | -500 | +500 | V | 2 |
| I _{LAT} | Latch-up current at ambient temperature of 105 °C | -100 | +100 | mA | |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

1.4 Voltage and current operating ratings

General

| Symbol | Description | Min. | Max. | Unit |
|-----------|---|----------------|-----------------------------|------|
| V_{DD} | Digital supply voltage | -0.3 | 3.8 | V |
| I_{DD} | Digital supply current | — | 120 | mA |
| V_{IO} | Digital pin input voltage (except open drain pins) | -0.3 | $V_{DD} + 0.3$ ¹ | V |
| | Open drain pins (PTC6 and PTC7) | -0.3 | 5.5 | V |
| I_D | Instantaneous maximum current single pin limit (applies to all port pins) | -25 | 25 | mA |
| V_{DDA} | Analog supply voltage | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V |

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

2 General

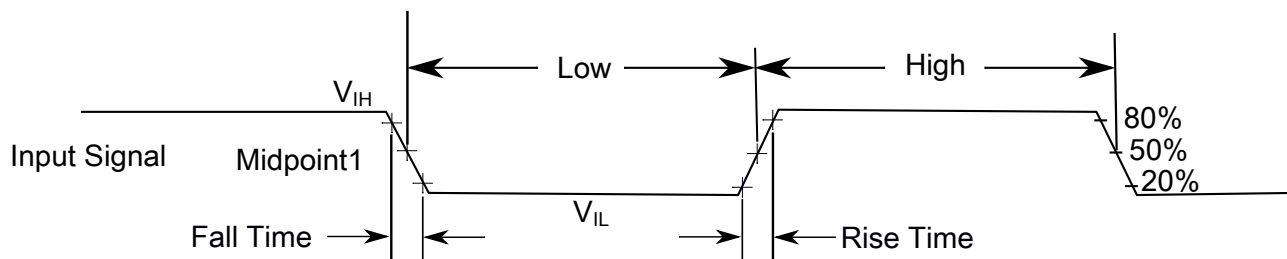
Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on nxp.com for guidelines on optimizing EMC performance.

- [AN2321: Designing for Board Level Electromagnetic Compatibility](#)
- [AN1050: Designing for Electromagnetic Compatibility \(EMC\) with HCMOS Microcontrollers](#)
- [AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers](#)
- [AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications](#)
- [AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems](#)

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are slew rate disabled, and
 - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------|--|---|---|--------|-------|
| V_{DD} | Supply voltage | 1.71 | 3.6 | V | |
| V_{DDA} | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | |
| $V_{SS} - V_{SSA}$ | V_{SS} -to- V_{SSA} differential voltage | -0.1 | 0.1 | V | |
| V_{IH} | Input high voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | $0.7 \times V_{DD}$ $0.75 \times V_{DD}$ | — — | V V | |
| V_{IL} | Input low voltage <ul style="list-style-type: none"> • $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ • $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$ | — — | $0.35 \times V_{DD}$ $0.3 \times V_{DD}$ | V V | |
| V_{HYS} | Input hysteresis | $0.06 \times V_{DD}$ | — | V | |
| I_{ICIO} | Pin negative DC injection current—single pin <ul style="list-style-type: none"> • $V_{IN} < V_{SS}-0.3\text{V}$ | -5 | — | mA | 1 |

Table continues on the next page...

General

Table 1. Voltage and current operating requirements (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------|--|------|------|------|-------|
| I_{ICcont} | Contiguous pin DC injection current—regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> Negative current injection | -25 | — | mA | |
| V_{RAM} | V_{DD} voltage required to retain RAM | 1.2 | — | V | |

- All I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3$ V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/I_{ICIO}$.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------|---|------|------|------|------|-------|
| V_{POR} | Falling V_{DD} POR detect voltage | 0.8 | 1.1 | 1.5 | V | |
| V_{LVDH} | Falling low-voltage detect threshold — high range (LVDV=01) | 2.48 | 2.56 | 2.64 | V | |
| V_{LVW1H} | Low-voltage warning thresholds — high range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) | 2.62 | 2.70 | 2.78 | V | 1 |
| V_{LVW2H} | <ul style="list-style-type: none"> Level 2 falling (LVWV=01) | 2.72 | 2.80 | 2.88 | V | |
| V_{LVW3H} | <ul style="list-style-type: none"> Level 3 falling (LVWV=10) | 2.82 | 2.90 | 2.98 | V | |
| V_{LVW4H} | <ul style="list-style-type: none"> Level 4 falling (LVWV=11) | 2.92 | 3.00 | 3.08 | V | |
| V_{HYSH} | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | |
| V_{LVDL} | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | |
| V_{LVW1L} | Low-voltage warning thresholds — low range <ul style="list-style-type: none"> Level 1 falling (LVWV=00) | 1.74 | 1.80 | 1.86 | V | 1 |
| V_{LVW2L} | <ul style="list-style-type: none"> Level 2 falling (LVWV=01) | 1.84 | 1.90 | 1.96 | V | |
| V_{LVW3L} | <ul style="list-style-type: none"> Level 3 falling (LVWV=10) | 1.94 | 2.00 | 2.06 | V | |
| V_{LVW4L} | <ul style="list-style-type: none"> Level 4 falling (LVWV=11) | 2.04 | 2.10 | 2.16 | V | |
| V_{HYSL} | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | |
| V_{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |
| t_{LPO} | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | |

- Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 3. Voltage and current operating behaviors

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|-----------------------|-------|------|-------|
| V _{OH} | Output high voltage — Normal drive pad All port pins, except PTC6 and PTC7 <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -1.5 mA | V _{DD} - 0.5 | — | V | |
| | | V _{DD} - 0.5 | — | V | |
| V _{OH} | Output high voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -6 mA | V _{DD} - 0.5 | — | V | |
| | | V _{DD} - 0.5 | — | V | |
| I _{OHT} | Output high current total for all ports | — | 100 | mA | |
| V _{OL} | Output low voltage — Normal drive pad All port pins <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA | — | 0.5 | V | |
| | | — | 0.5 | V | |
| V _{OL} | Output low voltage — High drive pad PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 pins <ul style="list-style-type: none"> • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 18 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 6 mA | — | 0.5 | V | |
| | | — | 0.5 | V | |
| I _{OLT} | Output low current total for all ports | — | 100 | mA | |
| I _{IN} | Input leakage current (per pin) for full temperature range | — | 1 | μA | |
| I _{IN} | Input leakage current (per pin) at 25 °C | — | 0.025 | μA | 1 |
| I _{IN} | Input leakage current (total all pins) for full temperature range | — | 41 | μA | 1 |
| I _{OZ} | Hi-Z (off-state) leakage current (per pin) | — | 1 | μA | |
| R _{PU} | Internal pullup resistors | 20 | 50 | kΩ | 2 |

1. Measured at V_{DD} = 3.6 V
2. Measured at V_{DD} supply voltage = V_{DD} min and V_{input} = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow RUN$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 4. Power mode transition operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------|---|------|------|------|---------|-------|
| t_{POR} | After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | — | — | 300 | μs | 1 |
| | • VLLS0 \rightarrow RUN | — | 123 | 132 | μs | |
| | • VLLS1 \rightarrow RUN | — | 123 | 132 | μs | |
| | • VLLS3 \rightarrow RUN | — | 67 | 72 | μs | |
| | • VLPS \rightarrow RUN | — | 4 | 5 | μs | |
| | • STOP \rightarrow RUN | — | 4 | 5 | μs | |

1. Normal boot FTFA_FOPT[LPBOOT]=11

2.2.5 KV11x Power consumption operating behaviors

Table 5. KV11x power consumption operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------|--|------|------|------|------|------------|
| I_{DDA} | Analog supply current | — | — | 5 | mA | 1 |
| I_{DD_RUN} | Run mode current — all peripheral clocks disabled, code executing from flash | | | | | Target IDD |
| | • at 1.8 V 50 MHz (25 MHz Bus) | — | 5.3 | 6.2 | mA | |
| | • at 3.0 V 50 MHz (25 MHz Bus) | — | 5.4 | 6.3 | mA | |
| | • at 1.8 V 75 MHz (25 MHz Bus) | — | 7.2 | 8.3 | mA | |
| | • at 3.0 V 75 MHz (25 MHz Bus) | — | 7.3 | 8.3 | mA | |
| I_{DD_RUN} | Run mode current — all peripheral clocks enabled, code executing from flash | | | | | Target IDD |

Table continues on the next page...

Table 5. KV11x power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|------|-------|------|------|-----------------------------------|
| | <ul style="list-style-type: none"> at 1.8 V 50 MHz at 3.0 V 50 MHz at 1.8 V 75 MHz at 3.0 V 75 MHz | — | 8.5 | 9.7 | mA | |
| I _{DD_WAIT} | Wait mode high frequency 75 MHz current at 3.0 V — all peripheral clocks disabled | — | 4 | — | mA | — |
| I _{DD_WAIT} | Wait mode reduced frequency 50 MHz current at 3.0 V — all peripheral clocks disabled | — | 3.4 | — | mA | — |
| I _{DD_VLPR} | Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks disabled | — | 268 | — | μA | 4 MHz CPU speed, 1 MHz bus speed. |
| I _{DD_VLPR} | Very-Low-Power Run mode current 4 MHz at 3.0 V — all peripheral clocks enabled | — | 437 | — | μA | 4 MHz CPU speed, 1 MHz bus speed. |
| I _{DD_VLPW} | Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks enabled | — | 348.9 | — | μA | 4 MHz CPU speed, 1 MHz bus speed. |
| I _{DD_VLPW} | Very-Low-Power Wait mode current at 3.0 V — all peripheral clocks disabled | — | 173.4 | — | μA | 4 MHz CPU speed, 1 MHz bus speed. |
| I _{DD_STOP} | Stop mode current at 3.0 V <ul style="list-style-type: none"> -40 °C to 25 °C at 50 °C at 70 °C at 85 °C at 105 °C | — | 247.2 | 286 | μA | — |
| | | — | 260.7 | 300 | | |
| | | — | 286 | 312 | | |
| | | — | 324 | 353 | | |
| | | — | 422.7 | 494 | | |
| I _{DD_VLPS} | Very-Low-Power Stop mode current at 3.0 V <ul style="list-style-type: none"> -40 °C to 25 °C at 50 °C at 70 °C at 85 °C at 105 °C | — | 2.9 | 3 | μA | — |
| | | — | 6.8 | 5.9 | | |
| | | — | 15.4 | 13 | | |
| | | — | 29.1 | 39 | | |
| | | — | 66.4 | 86 | | |
| I _{DD_VLLS3} | Very-Low-Leakage Stop mode 3 current at 3.0 V <ul style="list-style-type: none"> -40 °C to 25 °C at 50 °C at 70 °C at 85 °C at 105 °C | — | 1.3 | 1.6 | μA | — |
| | | — | 2 | 2.3 | | |
| | | — | 3.7 | 4.3 | | |
| | | — | 6.7 | 7.5 | | |
| | | — | 15.1 | 16 | | |
| I _{DD_VLLS1} | Very-Low-Leakage Stop mode 1 current at 3.0 V | | | | μA | — |

Table continues on the next page...

Table 5. KV11x power consumption operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|------|-------|-------|------|-------|
| | <ul style="list-style-type: none"> -40°C to 25°C at 50°C at 70°C at 85°C at 105°C | — | 0.8 | 1.2 | | |
| I _{DD_VLLS0} | Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> -40 °C to 25 °C at 50 °C at 70 °C at 85 °C at 105 °C | — | 0.279 | 0.386 | μA | — |
| | | — | 0.638 | 0.854 | | |
| | | — | 1.63 | 2.2 | | |
| | | — | 3.4 | 4.5 | | |
| | | — | 8.9 | 11.2 | | |
| I _{DD_VLLS0} | Very-Low-Leakage Stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V <ul style="list-style-type: none"> -40 °C to 25 °C at 50 °C at 70 °C at 85 °C at 105 °C | — | 0.098 | 0.452 | μA | 2 |
| | | — | 0.448 | 0.674 | | |
| | | — | 1.4 | 1.9 | | |
| | | — | 3.19 | 4.3 | | |
| | | — | 8.47 | 10.6 | | |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. No brownout

Table 6. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|----------------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| I _{IREFSTEN4MHZ} | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | μA |
| I _{IREFSTEN32KHZ} | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | μA |
| I _{EREFSTEN4MHZ} | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |
| I _{EREFSTEN32KHZ} | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by | | | | | | | |

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|-------------------|--|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | entering all modes with the crystal enabled. | 440 | 490 | 540 | 560 | 570 | 580 | nA |
| | VLLS1 | 440 | 490 | 540 | 560 | 570 | 580 | |
| | VLLS3 | 510 | 560 | 560 | 560 | 610 | 680 | |
| | VLPS | 510 | 560 | 560 | 560 | 610 | 680 | |
| | STOP | 510 | 560 | 560 | 560 | 610 | 680 | |
| I _{CMP} | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | μA |
| I _{UART} | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | μA |
| | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | |
| | OSCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| I _{SPI} | SPI peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | μA |
| | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | |
| | OSCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| I _{I2C} | I2C peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. | | | | | | | μA |
| | MCGIRCLK (4 MHz internal reference clock) | 66 | 66 | 66 | 66 | 66 | 66 | |
| | OSCERCLK (4 MHz external crystal) | 214 | 237 | 246 | 254 | 260 | 268 | |
| I _{FTM} | FTM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the | | | | | | | |

Table continues on the next page...

Table 6. Low power mode peripheral adders — typical value (continued)

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|-------------------|---|------------------|-----|-----|-----|-----|-----|------|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| | clock signal. Includes selected clock source and I/O switching currents. MCGIRCLK (4 MHz internal reference clock) OSCERCLK (4 MHz external crystal) | 150 | 150 | 150 | 150 | 150 | 150 | μA |
| I _{BG} | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | μA |
| I _{ADC} | ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | μA |
| I _{WDOG} | WDOG peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. MCGIRCLK (4 MHz internal reference clock) OSCERCLK (4 MHz external crystal) | 66 | 66 | 66 | 66 | 66 | 66 | μA |
| | | 214 | 237 | 246 | 254 | 260 | 268 | |

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode (except for 75 MHz which is in FEE mode), and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

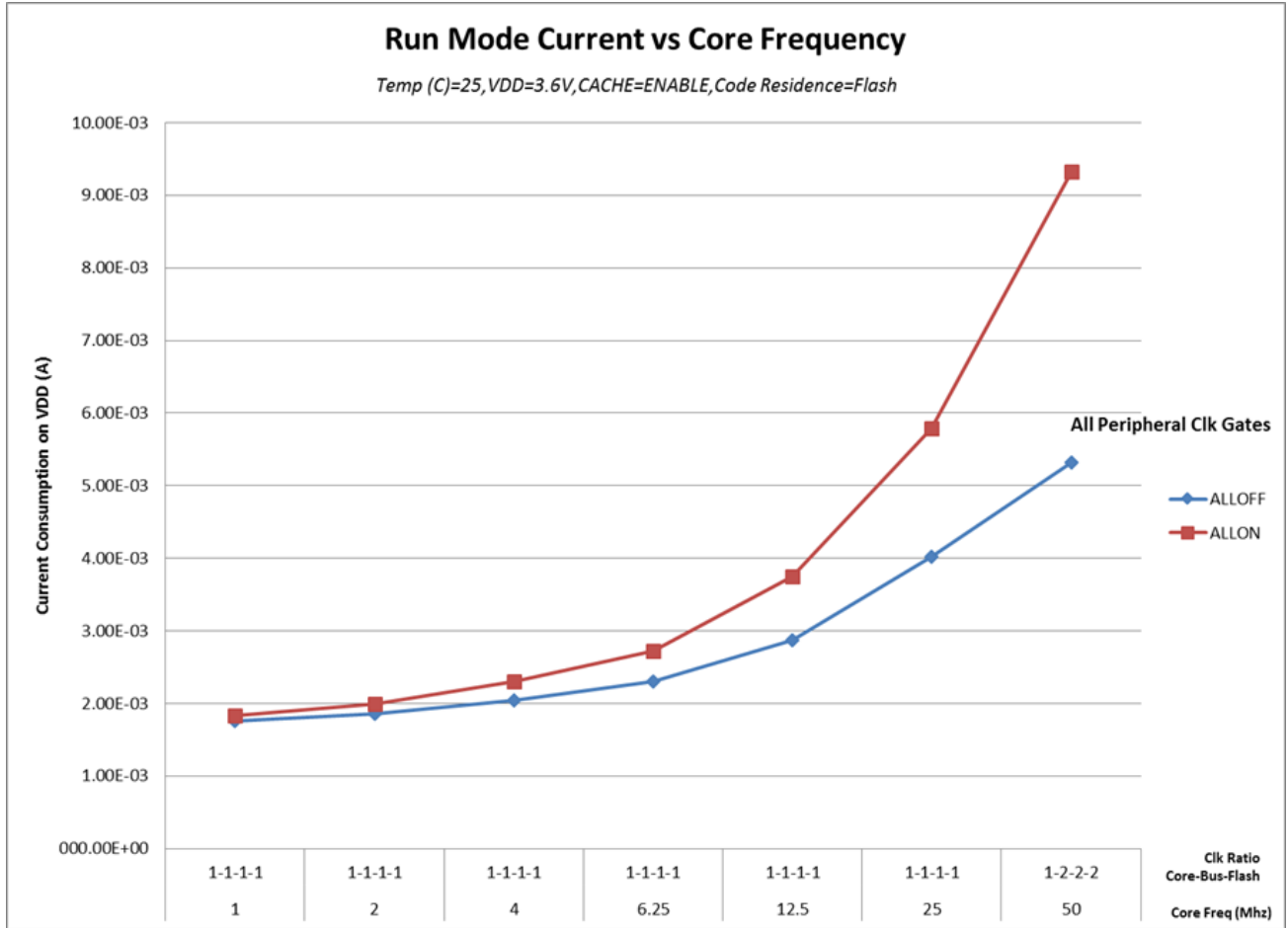


Figure 3. Run mode supply current vs. core frequency

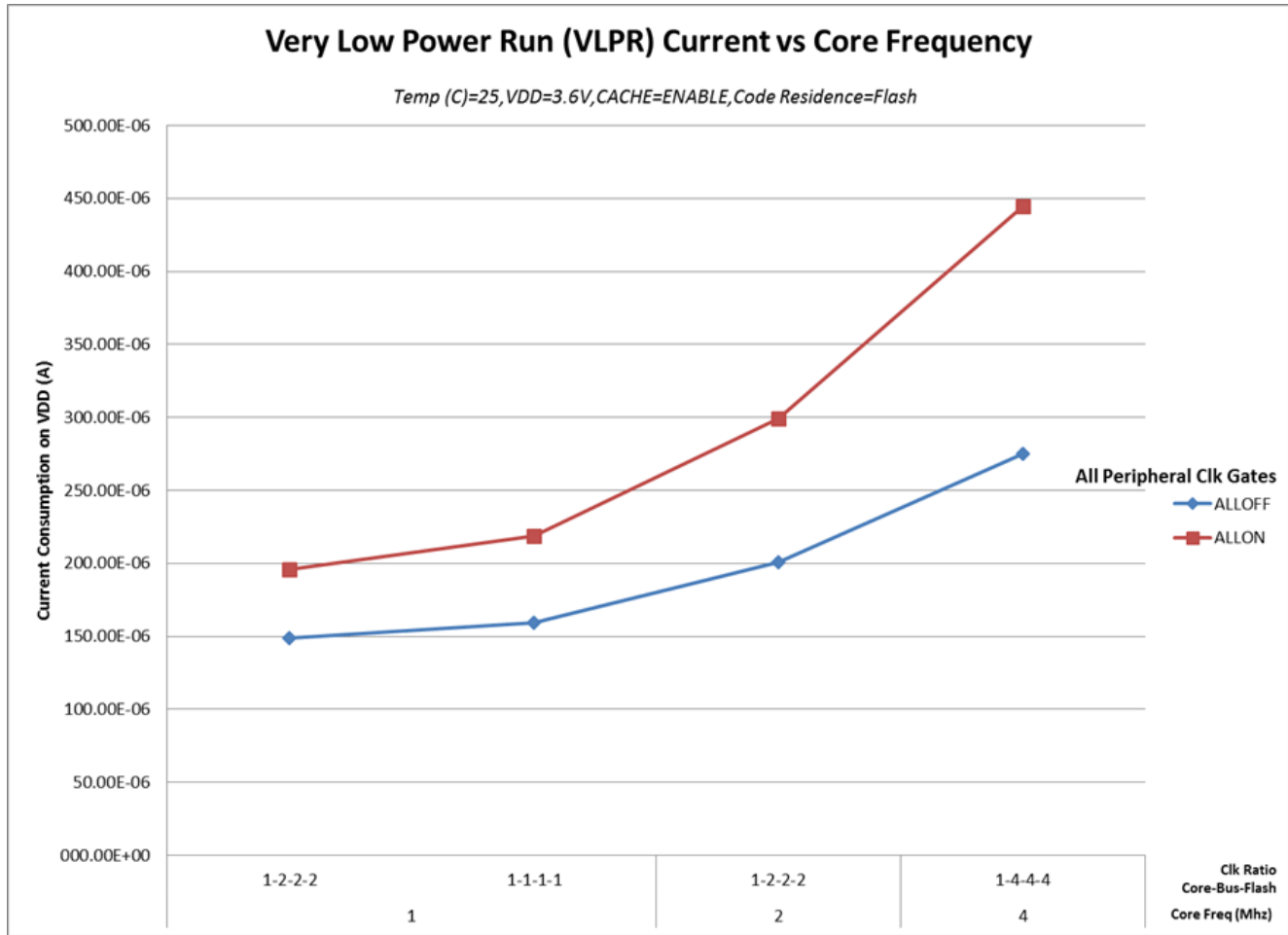


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

| Symbol | Description | Frequency band (MHz) | Typ. | Unit | Notes |
|---------------------|------------------------------------|----------------------|------|------|-------|
| V _{RE1} | Radiated emissions voltage, band 1 | 0.15–50 | 15 | dBμV | 1, 2 |
| V _{RE2} | Radiated emissions voltage, band 2 | 50–150 | 17 | dBμV | |
| V _{RE3} | Radiated emissions voltage, band 3 | 150–500 | 12 | dBμV | |
| V _{RE4} | Radiated emissions voltage, band 4 | 500–1000 | 4 | dBμV | |
| V _{RE_IEC} | IEC level | 0.15–1000 | M | — | 2, 3 |

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code.

The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ °C}$, $f_{OSC} = 10\text{ MHz}$ (crystal), $f_{SYS} = 75\text{ MHz}$, $f_{BUS} = 25\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 8. Capacitance attributes

| Symbol | Description | Min. | Max. | Unit |
|-------------|---------------------------------|------|------|------|
| C_{IN_A} | Input capacitance: analog pins | — | 7 | pF |
| C_{IN_D} | Input capacitance: digital pins | — | 7 | pF |

2.3 Switching specifications

2.3.1 Device clock specifications

Table 9. Device clock specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|---------------------|-----------------------|------|------|------|-------|
| Normal run mode | | | | | |
| f_{SYS} | System and core clock | — | 48 | MHz | |
| f_{BUS} | Bus clock | — | 24 | MHz | |
| f_{FLASH} | Flash clock | — | 24 | MHz | |
| f_{LPTMR} | LPTMR clock | — | 24 | MHz | |
| High Speed run mode | | | | | |
| f_{SYS} | System and core clock | — | 75 | MHz | |
| f_{BUS} | Bus clock | — | 25 | MHz | |
| f_{FLASH} | Flash clock | — | 25 | MHz | |
| f_{LPTMR} | LPTMR clock | — | 25 | MHz | |

Table continues on the next page...

Table 9. Device clock specifications (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------------------------|--|------|------|------|-------|
| f _{FTM} | FTM clock | — | 75 | MHz | |
| VLPR mode | | | | | |
| f _{SYS} | System and core clock | — | 4 | MHz | |
| f _{BUS} | Bus clock | — | 1 | MHz | |
| f _{FLASH} | Flash clock | — | 1 | MHz | |
| f _{LPTMR} | LPTMR clock | — | 25 | MHz | |
| f _{ERCLK} | External reference clock | — | 16 | MHz | |
| f _{LPTMR_pin} | LPTMR clock | — | 25 | MHz | |
| f _{LPTMR_ERCLK} | LPTMR external reference clock | — | 16 | MHz | |
| f _{osc_hi_2} | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz | |

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, and I²C signals.

Table 10. General switching specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|------|------|------------------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1 |
| | External RESET and NMI pin interrupt pulse width — Asynchronous path | 100 | — | ns | 2 |
| | GPIO pin interrupt pulse width — Asynchronous path | 16 | — | ns | 2 |
| | Port rise and fall time | | | | 3 |
| | Fast slew rate | | | | |
| | 1.71 ≤ VDD ≤ 2.7 V | — | 8 | ns | |
| | 2.7 ≤ VDD ≤ 3.6 V | — | 7 | ns | |
| | Port rise and fall time | | | | |
| | Slow slew rate | | | | |
| | 1.71 ≤ VDD ≤ 2.7 V | — | 15 | ns | |
| | 2.7 ≤ VDD ≤ 3.6 V | — | 25 | ns | |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

| Symbol | Description | Min. | Max. | Unit |
|----------------|----------------------------------|------|------|------|
| T _J | Die junction temperature | −40 | 125 | °C |
| T _A | Ambient temperature ¹ | −40 | 105 | °C |

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is:

$$T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$$

2.4.2 Thermal attributes

Table 12. Thermal attributes

| Board type | Symbol | Description | 64 LQFP | 48 LQFP | 32 LQFP | 32 QFN | Unit | Notes |
|-------------------|-------------------|---|---------|---------|---------|--------|------|-------|
| Single-layer (1S) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 64 | 81 | 85 | 98 | °C/W | 1 |
| Four-layer (2s2p) | R _{θJA} | Thermal resistance, junction to ambient (natural convection) | 46 | 57 | 57 | 34 | °C/W | |
| Single-layer (1S) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 52 | 68 | 72 | 82 | °C/W | |
| Four-layer (2s2p) | R _{θJMA} | Thermal resistance, junction to ambient (200 ft./min. air speed) | 39 | 51 | 50 | 28 | °C/W | |
| — | R _{θJB} | Thermal resistance, junction to board | 28 | 35 | 33 | 14 | °C/W | 2 |
| — | R _{θJC} | Thermal resistance, junction to case | 15 | 25 | 25 | 2.5 | °C/W | 3 |
| — | Ψ _{JT} | Thermal characterization parameter, junction to package top outside center (natural convection) | 2 | 7 | 7 | 8 | °C/W | 4 |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.

Peripheral operating requirements and behaviors

2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 13. SWD full voltage range electricals

| Symbol | Description | Min. | Max. | Unit |
|--------|--|------|------|------|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | SWD_CLK frequency of operation <ul style="list-style-type: none"> • Serial wire debug | 0 | 25 | MHz |
| J2 | SWD_CLK cycle period | 1/J1 | — | ns |
| J3 | SWD_CLK clock pulse width <ul style="list-style-type: none"> • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

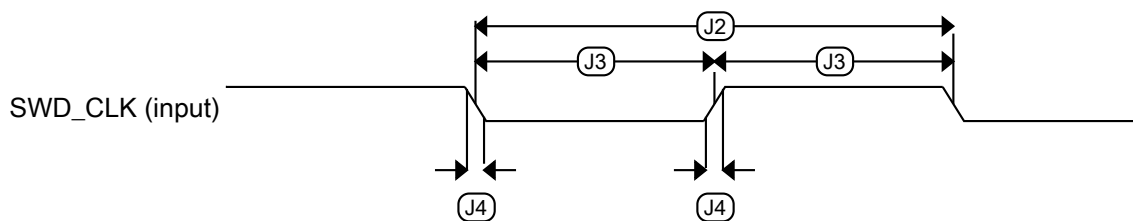


Figure 5. Serial wire clock input timing

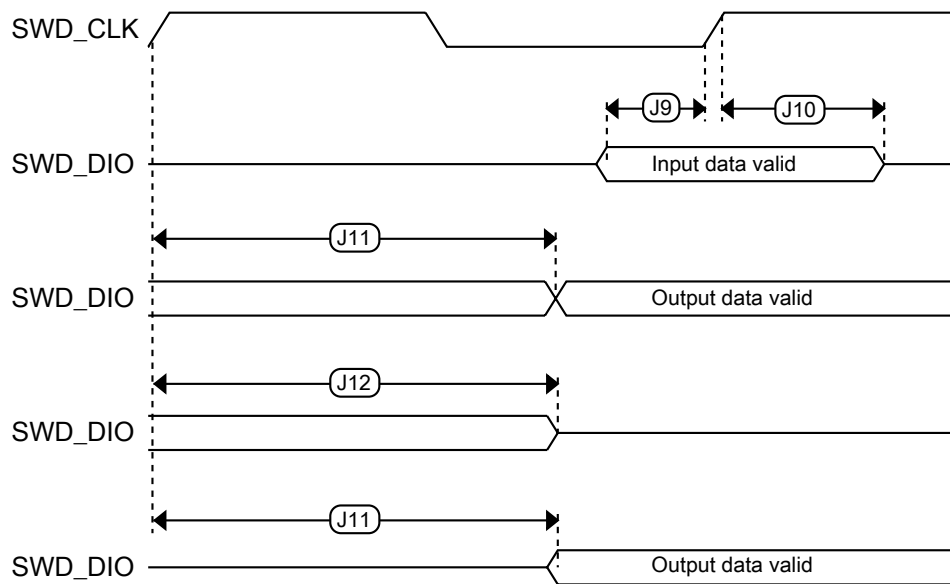


Figure 6. Serial wire data timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 14. MCG specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---------------------------------|--|-------|-----------|-----------|--------------------|-------|
| $f_{\text{ints_ft}}$ | Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C | — | 32.768 | — | kHz | |
| $f_{\text{ints_t}}$ | Internal reference frequency (slow clock) — user trimmed | 31.25 | — | 39.0625 | kHz | |
| $\Delta f_{\text{dco_res_t}}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM | — | ± 0.3 | ± 0.6 | $\%f_{\text{dco}}$ | 1 |

Table continues on the next page...

Table 14. MCG specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes | |
|--------------------------|---|--|-----------|-----------|------------------|-------|--------|
| Δf_{dco_t} | Total deviation of trimmed average DCO output frequency over voltage and temperature | — | +0.5/-0.7 | ± 2 | % f_{dco} | 1, 2 | |
| Δf_{dco_t} | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C | — | ± 0.4 | ± 1.5 | % f_{dco} | 1, 2 | |
| f_{intf_ft} | Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25 °C | — | 4 | — | MHz | | |
| Δf_{intf_ft} | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V_{DD} and 25 °C | — | +1/-2 | ± 3 | % f_{intf_ft} | 2 | |
| f_{intf_t} | Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C | 3 | — | 5 | MHz | | |
| f_{loc_low} | Loss of external clock minimum frequency — RANGE = 00 | $(3/5) \times f_{ints_t}$ | — | — | kHz | | |
| f_{loc_high} | Loss of external clock minimum frequency — RANGE = 01, 10, or 11 | $(16/5) \times f_{ints_t}$ | — | — | kHz | | |
| FLL | | | | | | | |
| f_{fill_ref} | FLL reference frequency range | 31.25 | — | 39.0625 | kHz | | |
| f_{dco} | DCO output frequency range | Low range (DRS = 00, DMX32 = 0) $640 \times f_{fill_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS = 01, DMX32 = 0) $1280 \times f_{fill_ref}$ | 40 | 41.94 | 48 | MHz | |
| | | Mid range (DRS = 10, DMX32 = 0) $1920 \times f_{fill_ref}$ | 60 | 62.915 | 75 | MHz | |
| $f_{dco_t_DMX32}$ 2 | DCO output frequency | Low range (DRS = 00, DMX32 = 1) $732 \times f_{fill_ref}$ | — | 23.99 | — | MHz | 5 6 |
| | | Mid range (DRS = 01, DMX32 = 1) $1464 \times f_{fill_ref}$ | — | 47.97 | — | MHz | |
| | | Mid range (DRS = 10, DMX32 = 1) $2197 \times f_{fill_ref}$ | — | 71.991 | — | MHz | |
| J_{cyc_fill} | FLL period jitter • $f_{VCO} = 75$ MHz | — | 180 | — | ps | 7 | |
| $t_{fill_acquire}$ | FLL target frequency acquisition time | — | — | 1 | ms | 8 | |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal V_{DD} and 25 °C, f_{ints_ft} .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.

4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or there is a change from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|------------------|-------|
| V_{DD} | Supply voltage | 1.71 | — | 3.6 | V | |
| I_{DDOSC} | Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> • 32 kHz • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz | — | 500 | — | nA | 1 |
| | | — | 200 | — | μA | |
| | | — | 300 | — | μA | |
| | | — | 950 | — | μA | |
| | | — | 1.2 | — | mA | |
| | | — | 1.5 | — | mA | |
| I_{DDOSC} | Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz | — | 500 | — | μA | 1 |
| | | — | 600 | — | μA | |
| | | — | 2.5 | — | mA | |
| | | — | 3 | — | mA | |
| | | — | 4 | — | mA | |
| C_x | EXTAL load capacitance | — | — | — | | 2, 3 |
| C_y | XTAL load capacitance | — | — | — | | 2, 3 |
| R_F | Feedback resistor — low-frequency, low-power mode (HGO=0) | — | — | — | $\text{M}\Omega$ | 2, 4 |
| | Feedback resistor — low-frequency, high-gain mode (HGO=1) | — | 10 | — | $\text{M}\Omega$ | |
| | Feedback resistor — high-frequency, low-power mode (HGO=0) | — | — | — | $\text{M}\Omega$ | |
| | Feedback resistor — high-frequency, high-gain mode (HGO=1) | — | 1 | — | $\text{M}\Omega$ | |

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|------------------------------|--|------|-----------------|------|------|-------|
| R _S | Series resistor — low-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — low-frequency, high-gain mode (HGO=1) | — | 200 | — | kΩ | |
| | Series resistor — high-frequency, low-power mode (HGO=0) | — | — | — | kΩ | |
| | Series resistor — high-frequency, high-gain mode (HGO=1) | — | 0 | — | kΩ | |
| V _{pp} ⁵ | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1) | — | V _{DD} | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | — | 0.6 | — | V | |
| | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | — | V _{DD} | — | V | |

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|---|------|------|------|------|-------|
| f _{osc_lo} | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| f _{osc_hi_1} | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| f _{osc_hi_2} | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| f _{ec_extal} | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1, 2 |
| t _{dc_extal} | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |

Table continues on the next page...

Table 16. Oscillator frequency specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------|--|------|------|------|------|-------|
| t_{cst} | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | 1000 | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | 250 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces**3.4.1 Flash electrical specifications**

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 17. NVM program/erase timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|------------------------------------|------|------|------|---------|-------|
| t_{hvpgm4} | Longword Program high-voltage time | — | 7.5 | 18 | μ s | — |
| $t_{hversscr}$ | Sector Erase high-voltage time | — | 13 | 113 | ms | 1 |
| $t_{hversall}$ | Erase All high-voltage time | — | 104 | 904 | ms | 1 |

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 18. Flash command timing specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------|---|------|------|------|---------------|-------|
| $t_{rd1sec2k}$ | Read 1s Section execution time (flash sector) | — | — | 60 | μs | 1 |
| t_{pgmchk} | Program Check execution time | — | — | 45 | μs | 1 |
| t_{rdsrc} | Read Resource execution time | — | — | 30 | μs | 1 |
| t_{pgm4} | Program Longword execution time | — | 65 | 145 | μs | — |
| t_{ersscr} | Erase Flash Sector execution time | — | 14 | 114 | ms | 2 |
| t_{rd1all} | Read 1s All Blocks execution time | — | — | 0.9 | ms | 1 |
| t_{rdonce} | Read Once execution time | — | — | 30 | μs | 1 |
| $t_{pgmonce}$ | Program Once execution time | — | 100 | — | μs | — |
| t_{ersall} | Erase All Blocks execution time | — | 140 | 1150 | ms | 2 |
| t_{vfykey} | Verify Backdoor Access Key execution time | — | — | 30 | μs | 1 |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3.4.1.3 Flash high voltage current behaviors

Table 19. Flash high voltage current behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| I_{DD_PGM} | Average current adder during high voltage flash programming operation | — | 2.5 | 12.0 | mA |
| I_{DD_ERS} | Average current adder during high voltage flash erase operation | — | 1.5 | 8.0 | mA |

3.4.1.4 Reliability specifications

Table 20. NVM reliability specifications

| Symbol | Description | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------------|--|------|-------------------|------|--------|-------|
| Program Flash | | | | | | |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5 | 50 | — | years | — |
| $t_{nvmretp1k}$ | Data retention after up to 1 K cycles | 20 | 100 | — | years | — |
| $n_{nvmcycp}$ | Cycling endurance | 10 K | 50 K | — | cycles | 2 |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40\text{ °C} \leq T_j \leq 125\text{ °C}$.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

3.6.1.1 16-bit ADC operating conditions

Table 21. 16-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|--------------------------------|---|--|-------------------|--|------|-------|
| V _{DDA} | Supply voltage | Absolute | 1.71 | — | 3.6 | V | |
| ΔV _{DDA} | Supply voltage | Delta to V _{DD} (V _{DD} – V _{DDA}) | -100 | 0 | +100 | mV | 2 |
| ΔV _{SSA} | Ground voltage | Delta to V _{SS} (V _{SS} – V _{SSA}) | -100 | 0 | +100 | mV | 2 |
| V _{REFH} | ADC reference voltage high | | 1.13 | V _{DDA} | V _{DDA} | V | |
| V _{REFL} | ADC reference voltage low | | V _{SSA} | V _{SSA} | V _{SSA} | V | |
| V _{ADIN} | Input voltage | <ul style="list-style-type: none"> 16-bit differential mode All other modes | V _{REFL} V _{REFL} | — — | 31/32 * V _{REFH} V _{REFH} | V | |
| C _{ADIN} | Input capacitance | <ul style="list-style-type: none"> 16-bit mode 8-bit / 10-bit / 12-bit modes | — — | 8 4 | 10 5 | pF | |
| R _{ADIN} | Input resistance | | — | 2 | 5 | kΩ | |
| R _{AS} | Analog source resistance | 13-bit / 12-bit modes f _{ADCK} < 4 MHz | — | — | 5 | kΩ | 3 |
| f _{ADCK} | ADC conversion clock frequency | ≤ 13-bit mode | 1.0 | — | 24.0 | MHz | 4 |
| f _{ADCK} | ADC conversion clock frequency | 16-bit mode | 2.0 | — | 12.0 | MHz | 4 |
| C _{rate} | ADC conversion rate | ≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 20.000 | — | 1200 | Ksps | 5 |

Table continues on the next page...

Table 21. 16-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------|---------------------|--|--------|-------------------|---------|------|-------|
| C_{rate} | ADC conversion rate | 16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time | 37.037 | — | 461.467 | Ksps | 5 |

1. Typical values assume $V_{DDA} = 3.0\text{ V}$, $Temp = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 1.0\text{ MHz}$, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8\ \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to $< 1\text{ ns}$.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

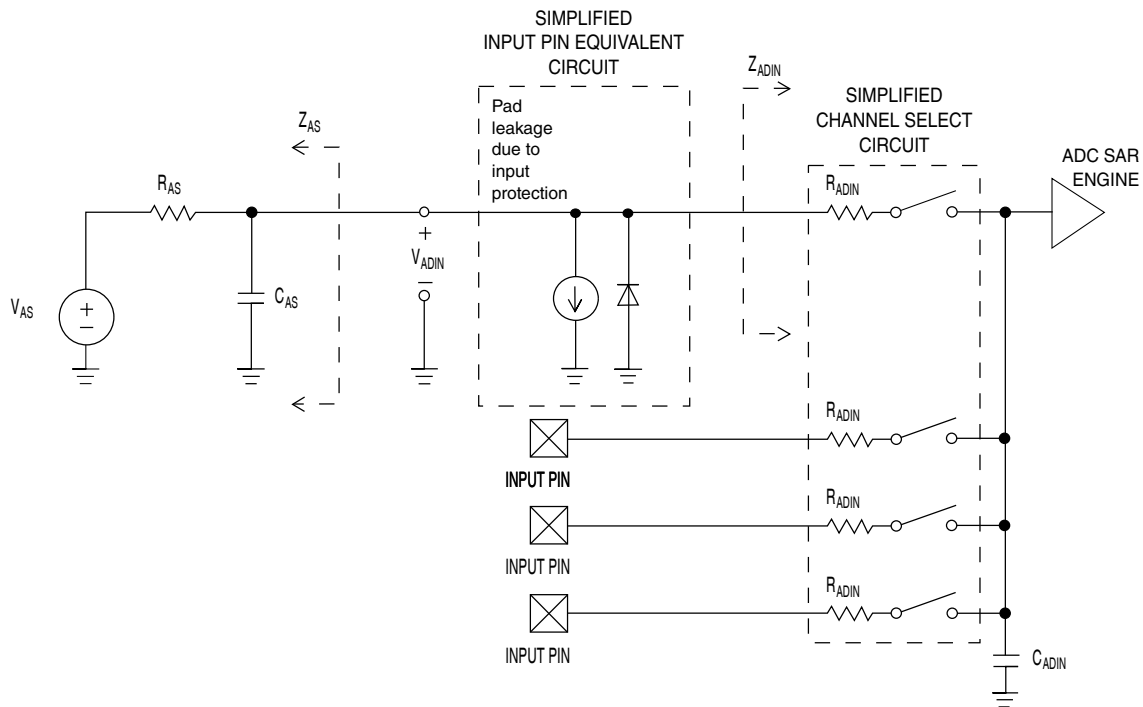


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

| Symbol | Description | Conditions ¹ . | Min. | Typ. ² | Max. | Unit | Notes |
|----------------|----------------|---------------------------|-------|-------------------|------|------|-------|
| I_{DDA_ADC} | Supply current | | 0.215 | — | 1.7 | mA | 3 |

Table continues on the next page...

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes | |
|-------------|---------------------------------|---|--------------------|------------------------|------------------------------|--------------------------|-----------------------------------|------|
| f_{ADACK} | ADC asynchronous clock source | • ADLPC = 1, ADHSC = 0 | 1.2 | 2.4 | 3.9 | MHz MHz MHz MHz | $t_{ADACK} = 1/f_{ADACK}$ | |
| | | • ADLPC = 1, ADHSC = 1 | 2.4 | 4.0 | 6.1 | | | |
| | | • ADLPC = 0, ADHSC = 0 | 3.0 | 5.2 | 7.3 | | | |
| | | • ADLPC = 0, ADHSC = 1 | 4.4 | 6.2 | 9.5 | | | |
| | Sample Time | See Reference Manual chapter for sample times | | | | | | |
| TUE | Total unadjusted error | • 12-bit modes • <12-bit modes | — — | ± 4 ± 1.4 | ± 6.8 ± 2.1 | LSB ⁴ | 5 | |
| DNL | Differential non-linearity | • 12-bit modes • <12-bit modes | — — | ± 0.7 ± 0.2 | -1.1 to +1.9 -0.3 to 0.5 | LSB ⁴ | 5 | |
| INL | Integral non-linearity | • 12-bit modes • <12-bit modes | — — | ± 1.0 ± 0.5 | -2.7 to +1.9 -0.7 to +0.5 | LSB ⁴ | 5 | |
| E_{FS} | Full-scale error | • 12-bit modes • <12-bit modes | — — | -4 -1.4 | -5.4 -1.8 | LSB ⁴ | $V_{ADIN} = V_{DDA}$ ⁵ | |
| E_Q | Quantization error | • 16-bit modes • ≤ 13 -bit modes | — — | -1 to 0 — | — ± 0.5 | LSB ⁴ | | |
| ENOB | Effective number of bits | 16-bit differential mode | | | | | 6, 7 | |
| | | • Avg = 32 | 12.8 | 14.5 | — | bits | | |
| | | • Avg = 4 | 11.9 | 13.8 | — | bits | | |
| | | 16-bit single-ended mode | | | | | | |
| • Avg = 32 | 12.2 | 13.7 | — | bits | | | | |
| • Avg = 4 | 11.4 | 13.1 | — | bits | | | | |
| SINAD | Signal-to-noise plus distortion | See ENOB | 6.02 × ENOB + 1.76 | | | dB | 7 | |
| THD | Total harmonic distortion | 16-bit differential mode | | | | | 7, 8 | |
| | | • Avg = 32 | — | -97 | — | dB | | |
| | | 16-bit single-ended mode | | | | | | |
| | | • Avg = 32 | — | -91 | — | dB | | |
| SFDR | Spurious free dynamic range | 16-bit differential mode | | 82 | 100 | — | dB | 7, 8 |

Table continues on the next page...

Table 22. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

| Symbol | Description | Conditions ¹ . | Min. | Typ. ² | Max. | Unit | Notes |
|--------------|---------------------|--|------------------------|-------------------|------|-------|---|
| | | <ul style="list-style-type: none"> Avg = 32 16-bit single-ended mode <ul style="list-style-type: none"> Avg = 32 | 78 | 92 | — | dB | |
| E_{IL} | Input leakage error | | $I_{in} \times R_{AS}$ | | | mV | I_{in} = leakage current (refer to the MCU's voltage and current operating ratings) |
| | Temp sensor slope | Across the full temperature range of the device | 1.55 | 1.62 | 1.69 | mV/°C | 9 |
| V_{TEMP25} | Temp sensor voltage | 25 °C | 706 | 716 | 726 | mV | 9 |

- All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
- Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- This data was collected with an external clock.
- Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- ADC conversion clock < 3 MHz

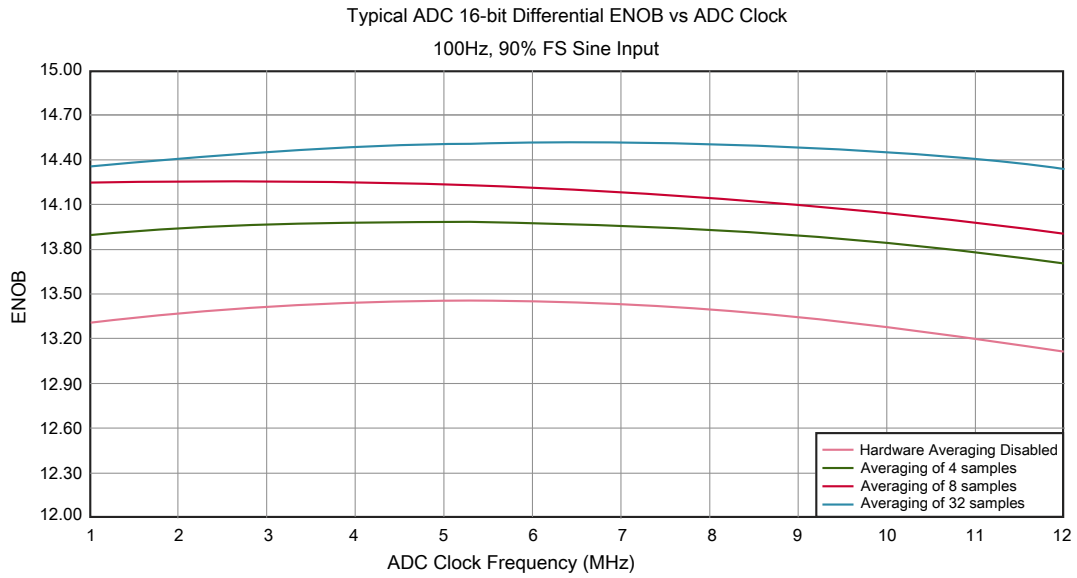


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit differential mode

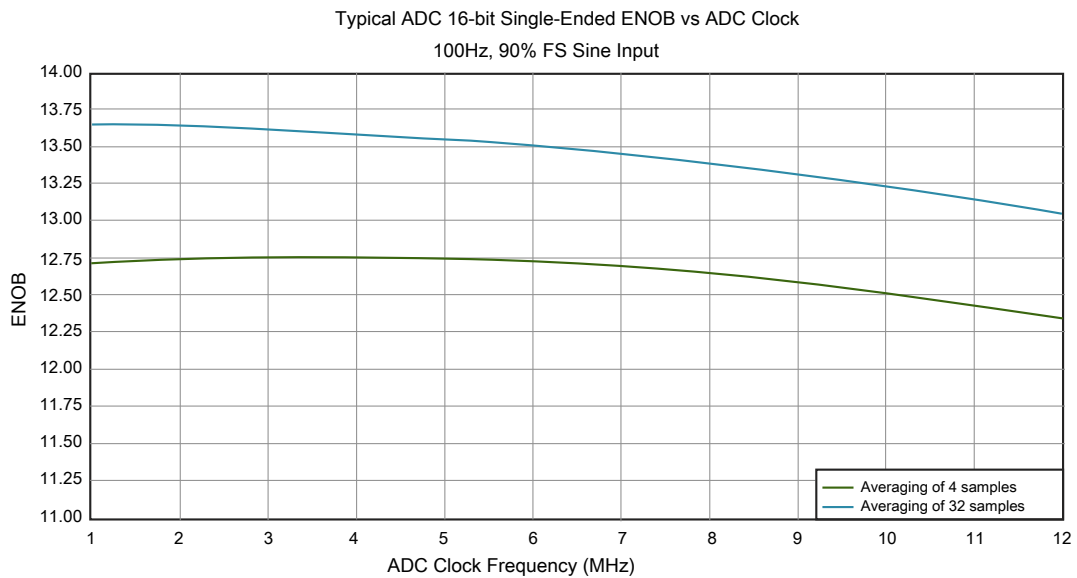


Figure 9. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 23. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------------|----------------|------|------|------|------|
| V _{DD} | Supply voltage | 1.71 | — | 3.6 | V |

Table continues on the next page...

Table 23. Comparator and 6-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-------------|--|----------------|------|----------|------------------|
| I_{DDHS} | Supply current, high-speed mode (EN = 1, PMODE = 1) | — | — | 200 | μA |
| $I_{DDL S}$ | Supply current, low-speed mode (EN = 1, PMODE = 0) | — | — | 20 | μA |
| V_{AIN} | Analog input voltage | V_{SS} | — | V_{DD} | V |
| V_{AIO} | Analog input offset voltage | — | — | 20 | mV |
| V_H | Analog comparator hysteresis ¹ <ul style="list-style-type: none"> • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11 | — | 5 | — | mV |
| | | — | 10 | — | mV |
| | | — | 20 | — | mV |
| | | — | 30 | — | mV |
| V_{CMPOh} | Output high | $V_{DD} - 0.5$ | — | — | V |
| V_{CMPOl} | Output low | — | — | 0.5 | V |
| t_{DHS} | Propagation delay, high-speed mode (EN = 1, PMODE = 1) | 20 | 35 | 200 | ns |
| t_{DLS} | Propagation delay, low-speed mode (EN = 1, PMODE = 0) | 80 | 100 | 600 | ns |
| | Analog comparator initialization delay ² | — | — | 40 | μs |
| I_{DAC6b} | 6-bit DAC current adder (enabled) | — | 7 | — | μA |
| INL | 6-bit DAC integral non-linearity | -0.5 | — | 0.5 | LSB ³ |
| DNL | 6-bit DAC differential non-linearity | -0.3 | — | 0.3 | LSB |

1. Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD} - 0.7$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

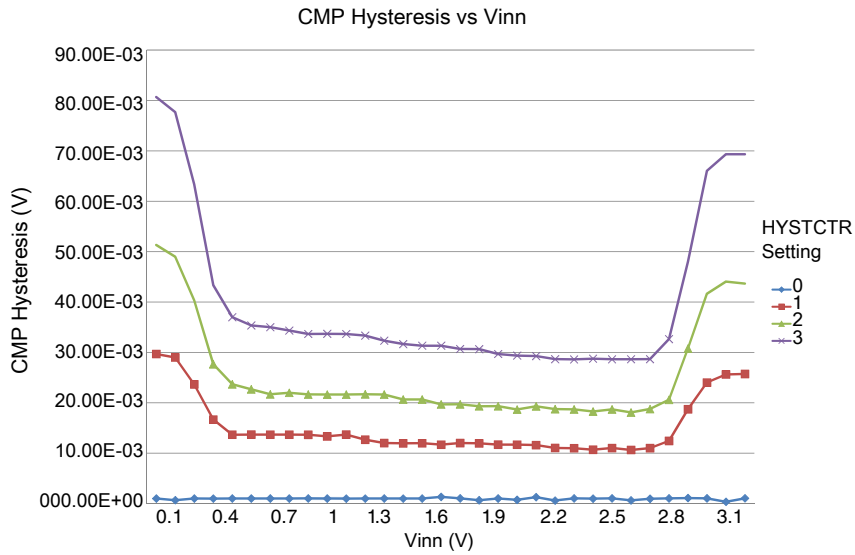


Figure 10. Typical hysteresis vs. Vin level ($V_{DD} = 3.3\text{ V}$, $PMODE = 0$)

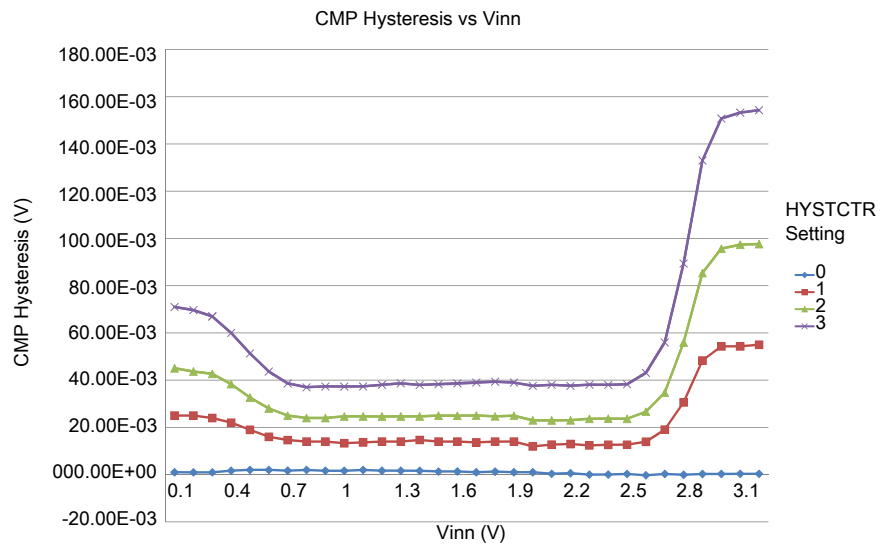


Figure 11. Typical hysteresis vs. Vin level ($V_{DD} = 3.3\text{ V}$, $PMODE = 1$)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 24. 12-bit DAC operating requirements

| Symbol | Description | Min. | Max. | Unit | Notes |
|-------------------|-------------------------|------|------|------|-------|
| V _{DDA} | Supply voltage | 1.71 | 3.6 | V | |
| V _{DACR} | Reference voltage | 1.13 | 3.6 | V | 1 |
| C _L | Output load capacitance | — | 100 | pF | 2 |
| I _L | Output load current | — | 1 | mA | |

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 25. 12-bit DAC operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|----------------------------|--|------------------------|----------|-------------------|--------|-------|
| I _{DDA_DACL} P | Supply current — low-power mode | — | — | 150 | μA | |
| I _{DDA_DACH} P | Supply current — high-speed mode | — | — | 700 | μA | |
| t _{DACLP} | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | μs | 1 |
| t _{DACHP} | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | μs | 1 |
| t _{CCDACLP} | Code-to-code settling time (0xBF8 to 0xC08)—high-speed mode | — | 1 | — | μs | 1 |
| | —low-power mode | — | — | 5 | μs | 1 |
| V _{dacoutl} | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| V _{dacouth} | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | V _{DACR} -100 | — | V _{DACR} | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — V _{DACR} > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — V _{DACR} = VREF_OUT | — | — | ±1 | LSB | 4 |
| V _{OFFSET} | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| E _G | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, V _{DDA} ≥ 2.4 V | 60 | — | 90 | dB | |
| T _{CO} | Temperature coefficient offset voltage | — | 3.7 | — | μV/C | 6 |
| T _{GE} | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| R _{op} | Output resistance (load = 3 kΩ) | — | — | 250 | Ω | |
| SR | Slew rate -80h → F7Fh → 80h | | | | V/μs | |

Table continues on the next page...

Table 25. 12-bit DAC operating behaviors (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------|---|------|------|------|------|-------|
| | <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) | 1.2 | 1.7 | — | | |
| BW | 3dB bandwidth | | | | kHz | |
| | <ul style="list-style-type: none"> High power (SP_{HP}) Low power (SP_{LP}) | 550 | — | — | | |
| | | 40 | — | — | | |

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4$ V
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
6. $V_{DDA} = 3.0$ V, reference select set for V_{DDA} (DAC_{X_CO}:DACRFS = 1), high power mode (DAC_{X_CO}:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

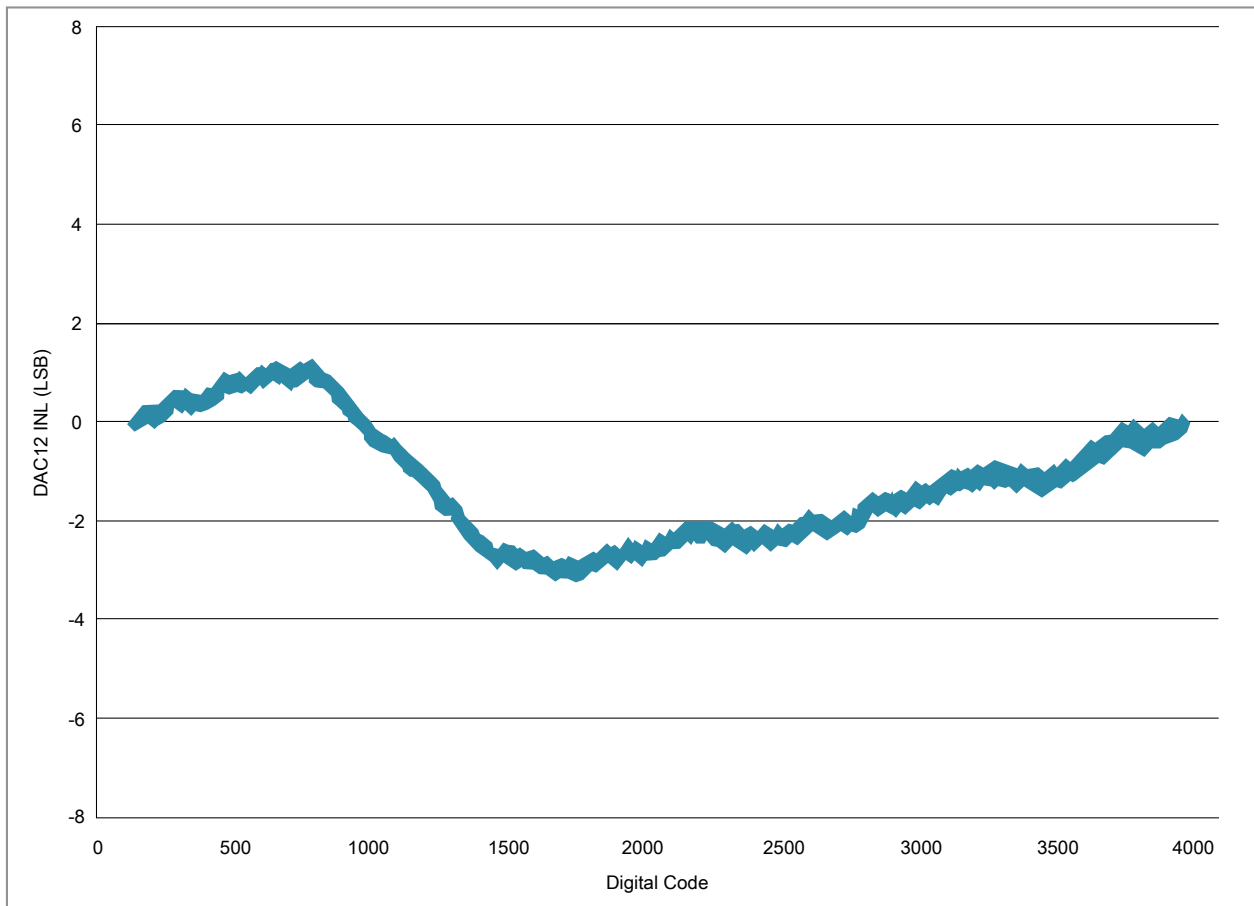


Figure 12. Typical INL error vs. digital code



Figure 13. Offset at half scale vs. temperature

3.7 Timers

See [General switching specifications](#).

3.8 Communication interfaces

3.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 26. Master mode DSPI timing (limited voltage range)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|---|--------------------|-------------------|------------|----------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | | 25 | MHz | 1 |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | – | ns | 2 |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS3 | DSPI_PCS _n valid to DSPI_SCK delay | $(t_{SCK}/2) - 2$ | – | ns | 3 |
| DS4 | DSPI_SCK to DSPI_PCS _n invalid delay | $(t_{SCK}/2) - 2$ | – | ns | 4 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | – | 8.7 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –2 | – | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 17 | – | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | – | ns | |
| | Frequency of operation | – | 25 | MHz | 5 |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | – | ns | 2 |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS3 | DSPI_PCS _n valid to DSPI_SCK delay | $(t_{SCK}/2) - 2$ | – | ns | 3 |
| DS4 | DSPI_SCK to DSPI_PCS _n invalid delay | $(t_{SCK}/2) - 2$ | – | ns | 4 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | – | 14.7 | ns | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –2 | – | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 17 | – | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | – | ns | |
| | Frequency of operation | – | 37.5 | MHz | 6 |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | – | ns | 2 |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 2$ | $(t_{SCK}/2) + 2$ | ns | |
| DS3 | DSPI_PCS _n valid to DSPI_SCK delay | $(t_{SCK}/2) - 2$ | – | ns | 3 |
| DS4 | DSPI_SCK to DSPI_PCS _n invalid delay | $(t_{SCK}/2) - 2$ | – | ns | 4 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | – | 8.7 | ns | |

Table continues on the next page...

Table 26. Master mode DSPI timing (limited voltage range) (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|----------------------------------|------|------|------|-------|
| DS6 | DSPI_SCK to DSPI_SOUT invalid | -2 | - | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 13 | - | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | - | ns | |

1. Normal pads
2. The SPI module is clocked by the system clock
3. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
4. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].
5. Open Drain pads: SIN: PTC7, SOUT:PTC6
6. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

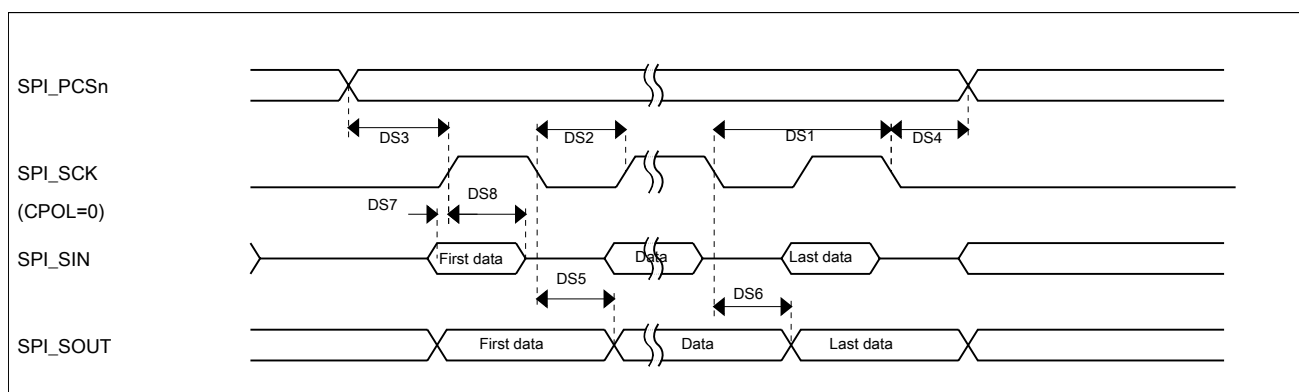


Figure 14. DSPI classic SPI timing — master mode

Table 27. Slave mode DSPI timing (limited voltage range)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|---------------------------|---------------------------|------------|----------|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | - | 12.5 | MHz | 1 |
| DS9 | DSPI_SCK input cycle time | 4 x t _{BUS} | - | ns | 2 |
| DS10 | DSPI_SCK input high/low time | (t _{SCK} /2) - 2 | (t _{SCK} /2) + 2 | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | - | 21 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | - | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.2 | - | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | - | ns | |
| DS15 | DSPI_SS active to DSPI_SOUT driven | - | 15 | ns | |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | - | 15 | ns | |
| | Frequency of operation | - | 12.5 | MHz | 3 |
| DS9 | DSPI_SCK input cycle time | 4 x t _{BUS} | - | ns | 2 |
| DS10 | DSPI_SCK input high/low time | (t _{SCK} /2) - 2 | (t _{SCK} /2) + 2 | ns | |

Table continues on the next page...

Table 27. Slave mode DSPI timing (limited voltage range) (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|---|---------------------------|--------------------------|------------|----------|
| DS11 | DSPI_SCK to DSPI_SOUT valid | – | 27 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | – | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.2 | – | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | – | ns | |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | – | 15 | ns | |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | – | 21 | ns | |
| | Frequency of operation | – | 18.75 | MHz | 4 |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{\text{BUS}}$ | – | ns | 2 |
| DS10 | DSPI_SCK input high/low time | $(t_{\text{SCK}}/2) - 2$ | $(t_{\text{SCK}}/2) + 2$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | – | 17 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | – | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.2 | – | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | – | ns | |
| DS15 | $\overline{\text{DSPI_SS}}$ active to DSPI_SOUT driven | – | 15 | ns | |
| DS16 | $\overline{\text{DSPI_SS}}$ inactive to DSPI_SOUT not driven | – | 11 | ns | |

1. Normal pads
2. The SPI module is clocked by the system clock
3. Open Drain pads: SIN: PTC7, SOUT:PTC6
4. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

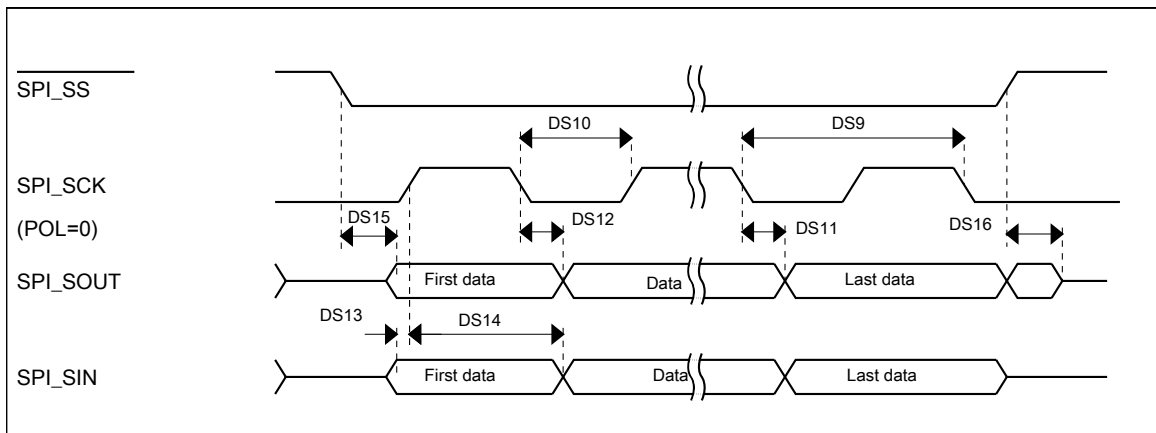


Figure 15. DSPI classic SPI timing — slave mode

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 28. Master mode DSPI timing (full voltage range)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|--------------------|-------------------|------------|----------|
| | Operating voltage | 1.7 | 3.6 | V | 1 |
| | Frequency of operation | – | 18.75 | MHz | 2 |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | – | ns | 3 |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS3 | DSPI_PCS n valid to DSPI_SCK delay | $(t_{SCK}/2) - 4$ | – | ns | 4 |
| DS4 | DSPI_SCK to DSPI_PCS n invalid delay | $(t_{SCK}/2) - 4$ | – | ns | 5 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | – | 10 | | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –7.8 | – | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 24 | – | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | – | ns | |
| | Frequency of operation | – | 18.75 | MHz | 6 |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | – | ns | 3 |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS3 | DSPI_PCS n valid to DSPI_SCK delay | $(t_{SCK}/2) - 4$ | – | ns | 4 |
| DS4 | DSPI_SCK to DSPI_PCS n invalid delay | $(t_{SCK}/2) - 4$ | – | ns | 5 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | – | 26 | | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –7.8 | – | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 24 | – | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | – | ns | |

Table continues on the next page...

Table 28. Master mode DSPI timing (full voltage range) (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------------------------------|--------------------|-------------------|------------|----------|
| | Frequency of operation | – | 25 | MHz | 7 |
| DS1 | DSPI_SCK output cycle time | $2 \times t_{BUS}$ | – | ns | 3 |
| DS2 | DSPI_SCK output high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS3 | DSPI_PCSn valid to DSPI_SCK delay | $(t_{SCK}/2) - 4$ | – | ns | 4 |
| DS4 | DSPI_SCK to DSPI_PCSn invalid delay | $(t_{SCK}/2) - 4$ | – | ns | 5 |
| DS5 | DSPI_SCK to DSPI_SOUT valid | – | 10 | | |
| DS6 | DSPI_SCK to DSPI_SOUT invalid | –7.8 | – | ns | |
| DS7 | DSPI_SIN to DSPI_SCK input setup | 17 | – | ns | |
| DS8 | DSPI_SCK to DSPI_SIN input hold | 0 | – | ns | |

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. Normal pads
3. The SPI module is clocked by the system clock
4. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
5. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC]
6. Open Drain pads: SIN: PTC7, SOUT:PTC6
7. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

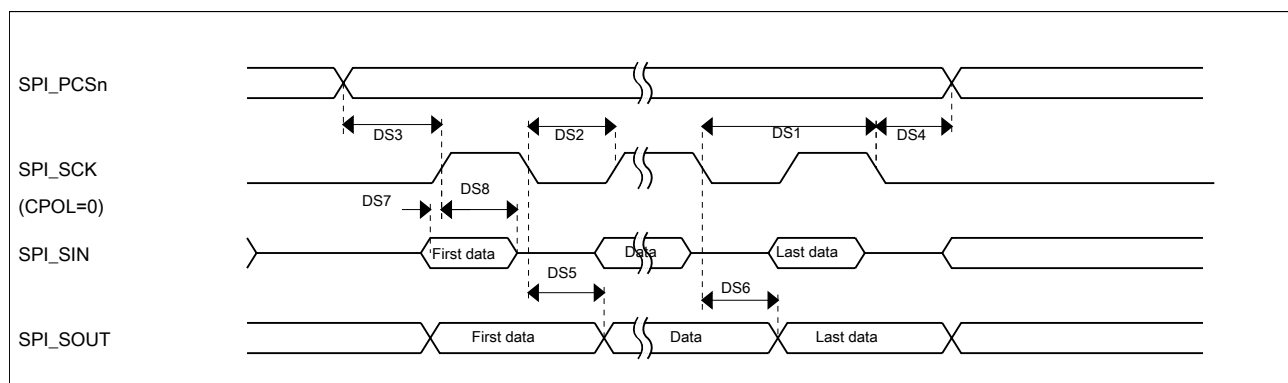


Figure 16. DSPI classic SPI timing — master mode

Table 29. Slave mode DSPI timing (full voltage range)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|-------------------------------|------|--------------|------------|----------|
| | Operating voltage | 1.7 | 3.6 | V | |
| | Frequency of operation | – | 9.375 | MHz | 1 |

Table continues on the next page...

Table 29. Slave mode DSPI timing (full voltage range) (continued)

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|--------------------|-------------------|------------|----------|
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns | 2 |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 27.8 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.7 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 22 | ns | |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 22 | ns | |
| | Frequency of operation | — | 9.375 | MHz | 3 |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns | 2 |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 43.8 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.7 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 22 | ns | |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 38 | ns | |
| | Frequency of operation | | 12.5 | MHz | 4 |
| DS9 | DSPI_SCK input cycle time | $4 \times t_{BUS}$ | — | ns | 2 |
| DS10 | DSPI_SCK input high/low time | $(t_{SCK}/2) - 4$ | $(t_{SCK}/2) + 4$ | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 20.8 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.7 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | DSPI_SS active to DSPI_SOUT driven | — | 22 | ns | |
| DS16 | DSPI_SS inactive to DSPI_SOUT not driven | — | 15 | ns | |

1. Normal pads
2. The SPI module is clocked by the system clock
3. Open Drain pads: SIN: PTC7, SOUT:PTC6
4. Fast pads: SIN: PTD7, SOUT:PTD6, SCK: PTD5, PCS:PTD4

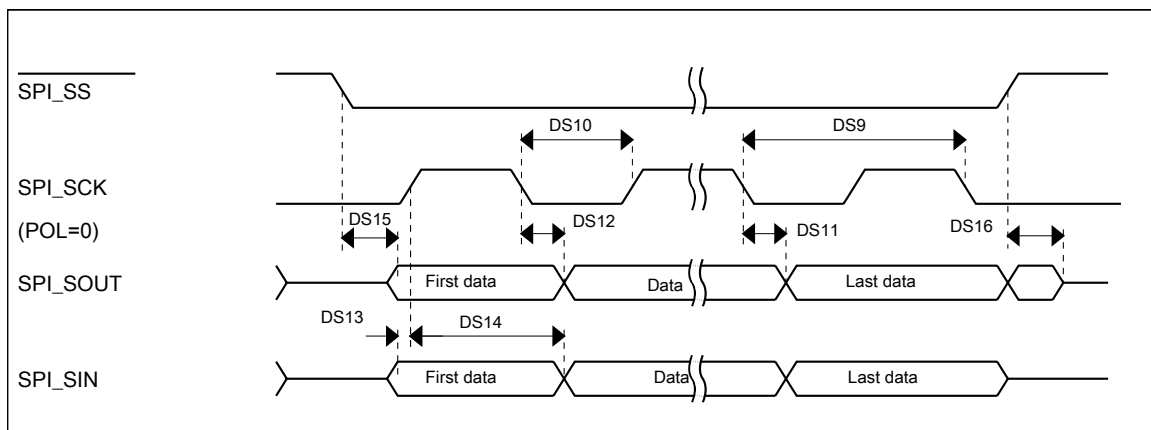


Figure 17. DSPI classic SPI timing — slave mode

3.8.3 I²C

See [General switching specifications](#).

3.8.4 UART

See [General switching specifications](#).

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 32-pin QFN | 98ASA00473D |
| 32-pin LQFP ¹ | 98ASH70029A |
| 48-pin LQFP | 98ASH00962A |
| 64-pin LQFP | 98ASS23234W |

1. The 32-pin LQFP package for this product is not yet available, however it is included in a Package Your Way program for Kinetis MCUs. Please visit <http://www.nxp.com/KPYW> for more details.

5 Pinout

5.1 KV11 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

- PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, PTD7 are high current pins.
- PTC6 and PTC7 have open drain outputs

| 64 LQFP | 48 QFP | 32 QFN | 32 LQFP | Pin Name | DEFAULT | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---------|--------|--------|---------|--------------------|------------------------------------|------------------------------------|--------------------|-----------|-----------------|----------------|------|-----------------|------|
| — | — | 7 | 7 | VDDA/ VREFH | VDDA/ VREFH | VDDA/ VREFH | | | | | | | |
| — | — | 8 | 8 | VREFL/ VSSA | VREFL/ VSSA | VREFL/ VSSA | | | | | | | |
| 1 | — | — | — | PTE0 | ADC1_SE12 | ADC1_SE12 | PTE0 | | UART1_TX | | | | |
| 2 | — | — | — | PTE1/ LLWU_P0 | ADC1_SE13 | ADC1_SE13 | PTE1/ LLWU_P0 | | UART1_RX | | | | |
| 3 | 1 | 1 | 1 | VDD | VDD | VDD | | | | | | | |
| 4 | 2 | 2 | 2 | VSS | VSS | VSS | | | | | | | |
| 5 | 3 | 3 | 3 | PTE16 | ADC0_SE1/ ADC0_DP1/ ADC1_SE0 | ADC0_SE1/ ADC0_DP1/ ADC1_SE0 | PTE16 | SPI0_PCS0 | UART1_TX | FTM_ CLKIN0 | | FTM0_FLT3 | |
| 6 | 4 | 4 | 4 | PTE17/ LLWU_P19 | ADC0_DM1/ ADC0_SE5/ ADC1_SE5 | ADC0_DM1/ ADC0_SE5/ ADC1_SE5 | PTE17/ LLWU_P19 | SPI0_SCK | UART1_RX | FTM_ CLKIN1 | | LPTMR0_ ALT3 | |
| 7 | 5 | 5 | 5 | PTE18/ LLWU_P20 | ADC0_SE6/ ADC1_SE1/ ADC1_DP1 | ADC0_SE6/ ADC1_SE1/ ADC1_DP1 | PTE18/ LLWU_P20 | SPI0_SOUT | UART1_ CTS_b | I2C0_SDA | | SPI0_SIN | |
| 8 | 6 | 6 | 6 | PTE19 | ADC0_SE7/ ADC1_SE7/ ADC1_DM1 | ADC0_SE7/ ADC1_SE7/ ADC1_DM1 | PTE19 | SPI0_SIN | UART1_ RTS_b | I2C0_SCL | | SPI0_SOUT | |
| 9 | 7 | — | — | PTE20 | ADC0_SE0/ ADC0_DP0 | ADC0_SE0/ ADC0_DP0 | PTE20 | | FTM1_CH0 | UART0_TX | | | |
| 10 | 8 | — | — | PTE21 | ADC0_SE4/ ADC0_DM0 | ADC0_SE4/ ADC0_DM0 | PTE21 | | FTM1_CH1 | UART0_RX | | | |
| 11 | — | — | — | PTE22 | ADC0_SE12 | ADC0_SE12 | PTE22 | | | | | | |
| 12 | — | — | — | PTE23 | ADC0_SE13 | ADC0_SE13 | PTE23 | | | | | | |
| 13 | 9 | — | — | VDDA | VDDA | VDDA | | | | | | | |

| 64 LQFP | 48 QFP | 32 QFN | 32 LQFP | Pin Name | DEFAULT | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|------------|-----------|-----------|------------|--------------------|--------------------------------------|--------------------------------------|--------------------|-----------------|-----------------|----------------|-----------------|-----------------|-----------------|
| 14 | 10 | — | — | VREFH | VREFH | VREFH | | | | | | | |
| 15 | 11 | — | — | VREFL | VREFL | VREFL | | | | | | | |
| 16 | 12 | — | — | VSSA | VSSA | VSSA | | | | | | | |
| 17 | 13 | — | — | PTE29 | CMP1_IN5/ CMP0_IN5 | CMP1_IN5/ CMP0_IN5 | PTE29 | | FTM0_CH2 | | FTM_ CLKIN0 | | |
| 18 | 14 | 9 | 9 | PTE30 | ADC1_SE4/ CMP1_IN4/ DAC0_OUT | ADC1_SE4/ CMP1_IN4/ DAC0_OUT | PTE30 | | FTM0_CH3 | | FTM_ CLKIN1 | | |
| 19 | — | — | — | PTE31 | ADC0_SE14/ CMP0_IN4 | ADC0_SE14/ CMP0_IN4 | PTE31 | | | | | | |
| 20 | 15 | 10 | 10 | PTE24 | DISABLED | | PTE24 | CAN0_TX | FTM0_CH0 | | I2C0_SCL | EWM_OUT_ b | |
| 21 | 16 | 11 | 11 | PTE25/ LLWU_P21 | DISABLED | | PTE25/ LLWU_P21 | CAN0_RX | FTM0_CH1 | | I2C0_SDA | EWM_IN | |
| 22 | 17 | 12 | 12 | PTA0 | SWD_CLK | SWD_CLK | PTA0 | UART0_ CTS_b | FTM0_CH5 | | EWM_IN | | SWD_CLK |
| 23 | 18 | 13 | 13 | PTA1 | DISABLED | | PTA1 | UART0_RX | FTM2_CH0 | CMP0_OUT | FTM2_QD_ PHA | FTM1_CH1 | FTM4_CH0 |
| 24 | 19 | 14 | 14 | PTA2 | DISABLED | | PTA2 | UART0_TX | FTM2_CH1 | CMP1_OUT | FTM2_QD_ PHB | FTM1_CH0 | FTM4_CH1 |
| 25 | 20 | 15 | 15 | PTA3 | SWD_DIO | SWD_DIO | PTA3 | UART0_ RTS_b | FTM0_CH0 | FTM2_FLT0 | EWM_OUT_ b | | SWD_DIO |
| 26 | 21 | 16 | 16 | PTA4/ LLWU_P3 | NMI_b | NMI_b | PTA4/ LLWU_P3 | | FTM0_CH1 | FTM4_FLT0 | FTM0_FLT3 | | NMI_b |
| 27 | — | — | — | PTA5 | DISABLED | | PTA5 | | FTM0_CH2 | FTM5_FLT0 | | | |
| 28 | — | — | — | PTA12 | DISABLED | | PTA12 | CAN0_TX | FTM1_CH0 | | | | FTM1_QD_ PHA |
| 29 | — | — | — | PTA13/ LLWU_P4 | DISABLED | | PTA13/ LLWU_P4 | CAN0_RX | FTM1_CH1 | | | | FTM1_QD_ PHB |
| 30 | 22 | — | — | VDD | VDD | VDD | | | | | | | |
| 31 | 23 | — | — | VSS | VSS | VSS | | | | | | | |
| 32 | 24 | 17 | 17 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | FTM0_FLT2 | FTM_ CLKIN0 | | FTM3_CH2 | |
| 33 | 25 | 18 | 18 | PTA19 | XTAL0 | XTAL0 | PTA19 | FTM0_FLT0 | FTM1_FLT0 | FTM_ CLKIN1 | | LPTMR0_ ALT1 | |
| 34 | 26 | 19 | 19 | PTA20 | RESET_b | | PTA20 | | | | | | RESET_b |
| 35 | 27 | 20 | 20 | PTB0/ LLWU_P5 | ADC0_SE8/ ADC1_SE8 | ADC0_SE8/ ADC1_SE8 | PTB0/ LLWU_P5 | I2C0_SCL | FTM1_CH0 | | | FTM1_QD_ PHA | UART0_RX |
| 36 | 28 | 21 | 21 | PTB1 | ADC0_SE9/ ADC1_SE9 | ADC0_SE9/ ADC1_SE9 | PTB1 | I2C0_SDA | FTM1_CH1 | FTM0_FLT2 | EWM_IN | FTM1_QD_ PHB | UART0_TX |
| 37 | 29 | — | — | PTB2 | ADC0_SE10/ ADC1_SE10/ ADC1_DM2 | ADC0_SE10/ ADC1_SE10/ ADC1_DM2 | PTB2 | I2C0_SCL | UART0_ RTS_b | FTM0_FLT1 | | FTM0_FLT3 | |
| 38 | 30 | — | — | PTB3 | ADC1_SE2/ ADC1_DP2 | ADC1_SE2/ ADC1_DP2 | PTB3 | I2C0_SDA | UART0_ CTS_b | | | FTM0_FLT0 | |

Pinout

| 64 LQFP | 48 QFP | 32 QFN | 32 LQFP | Pin Name | DEFAULT | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|------------|-----------|-----------|------------|--------------------|------------------------|------------------------|--------------------|-----------|-------------|-------------|----------|-----------|-----------|
| 39 | 31 | — | — | PTB16 | DISABLED | | PTB16 | | UART0_RX | FTM_CLKIN2 | CAN0_TX | EWM_IN | |
| 40 | 32 | — | — | PTB17 | DISABLED | | PTB17 | | UART0_TX | FTM_CLKIN1 | CAN0_RX | EWM_OUT_b | |
| 41 | — | — | — | PTB18 | DISABLED | | PTB18 | CAN0_TX | | FTM3_CH2 | | | |
| 42 | — | — | — | PTB19 | DISABLED | | PTB19 | CAN0_RX | | FTM3_CH3 | | | |
| 43 | 33 | — | — | PTC0 | ADC1_SE11 | ADC1_SE11 | PTC0 | SPI0_PCS4 | PDB_EXTRG0 | | CMP0_OUT | FTM0_FLT0 | SPI0_PCS0 |
| 44 | 34 | 22 | 22 | PTC1/ LLWU_P6 | ADC1_SE3 | ADC1_SE3 | PTC1/ LLWU_P6 | SPI0_PCS3 | UART1_RTS_b | FTM0_CH0 | FTM2_CH0 | | |
| 45 | 35 | 23 | 23 | PTC2 | ADC0_SE11/ CMP1_IN0 | ADC0_SE11/ CMP1_IN0 | PTC2 | SPI0_PCS2 | UART1_CTS_b | FTM0_CH1 | FTM2_CH1 | | |
| 46 | 36 | 24 | 24 | PTC3/ LLWU_P7 | CMP1_IN1 | CMP1_IN1 | PTC3/ LLWU_P7 | SPI0_PCS1 | UART1_RX | FTM0_CH2 | CLKOUT | FTM3_FLT0 | |
| 47 | — | — | — | VSS | VSS | VSS | | | | | | | |
| 48 | — | — | — | VDD | VDD | VDD | | | | | | | |
| 49 | 37 | 25 | 25 | PTC4/ LLWU_P8 | DISABLED | | PTC4/ LLWU_P8 | SPI0_PCS0 | UART1_TX | FTM0_CH3 | | CMP1_OUT | |
| 50 | 38 | 26 | 26 | PTC5/ LLWU_P9 | DISABLED | | PTC5/ LLWU_P9 | SPI0_SCK | LPTMR0_ALT2 | | | CMP0_OUT | FTM0_CH2 |
| 51 | 39 | 27 | 27 | PTC6/ LLWU_P10 | CMP0_IN0 | CMP0_IN0 | PTC6/ LLWU_P10 | SPI0_SOUT | PDB_EXTRG1 | | UART0_RX | | I2C0_SCL |
| 52 | 40 | 28 | 28 | PTC7 | CMP0_IN1 | CMP0_IN1 | PTC7 | SPI0_SIN | | | UART0_TX | | I2C0_SDA |
| 53 | — | — | — | PTC8 | ADC1_SE14/ CMP0_IN2 | ADC1_SE14/ CMP0_IN2 | PTC8 | | FTM3_CH4 | | | | |
| 54 | — | — | — | PTC9 | ADC1_SE15/ CMP0_IN3 | ADC1_SE15/ CMP0_IN3 | PTC9 | | FTM3_CH5 | | | | |
| 55 | — | — | — | PTC10 | ADC1_SE16 | ADC1_SE16 | PTC10 | | FTM5_CH0 | FTM5_QD_PHA | | | |
| 56 | — | — | — | PTC11/ LLWU_P11 | ADC1_SE17 | ADC1_SE17 | PTC11/ LLWU_P11 | | FTM5_CH1 | FTM5_QD_PHB | | | |
| 57 | 41 | — | — | PTD0/ LLWU_P12 | DISABLED | | PTD0/ LLWU_P12 | SPI0_PCS0 | UART0_CTS_b | FTM0_CH0 | UART1_RX | FTM3_CH0 | |
| 58 | 42 | — | — | PTD1 | ADC0_SE2 | ADC0_SE2 | PTD1 | SPI0_SCK | UART0_RTS_b | FTM0_CH1 | UART1_TX | FTM3_CH1 | |
| 59 | 43 | — | — | PTD2/ LLWU_P13 | DISABLED | | PTD2/ LLWU_P13 | SPI0_SOUT | UART0_RX | FTM0_CH2 | | FTM3_CH2 | I2C0_SCL |
| 60 | 44 | — | — | PTD3 | DISABLED | | PTD3 | SPI0_SIN | UART0_TX | FTM0_CH3 | | FTM3_CH3 | I2C0_SDA |
| 61 | 45 | 29 | 29 | PTD4/ LLWU_P14 | DISABLED | | PTD4/ LLWU_P14 | SPI0_PCS1 | UART0_RTS_b | FTM0_CH4 | FTM2_CH0 | EWM_IN | SPI0_PCS0 |
| 62 | 46 | 30 | 30 | PTD5 | ADC0_SE3 | ADC0_SE3 | PTD5 | SPI0_PCS2 | UART0_CTS_b | FTM0_CH5 | FTM2_CH1 | EWM_OUT_b | SPI0_SCK |
| 63 | 47 | 31 | 31 | PTD6/ LLWU_P15 | ADC1_SE6 | ADC1_SE6 | PTD6/ LLWU_P15 | FTM4_CH0 | UART0_RX | FTM0_CH0 | FTM1_CH0 | FTM0_FLT0 | SPI0_SOUT |
| 64 | 48 | 32 | 32 | PTD7 | DISABLED | | PTD7 | FTM4_CH1 | UART0_TX | FTM0_CH1 | FTM1_CH1 | FTM0_FLT1 | SPI0_SIN |

5.2 KV11 Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

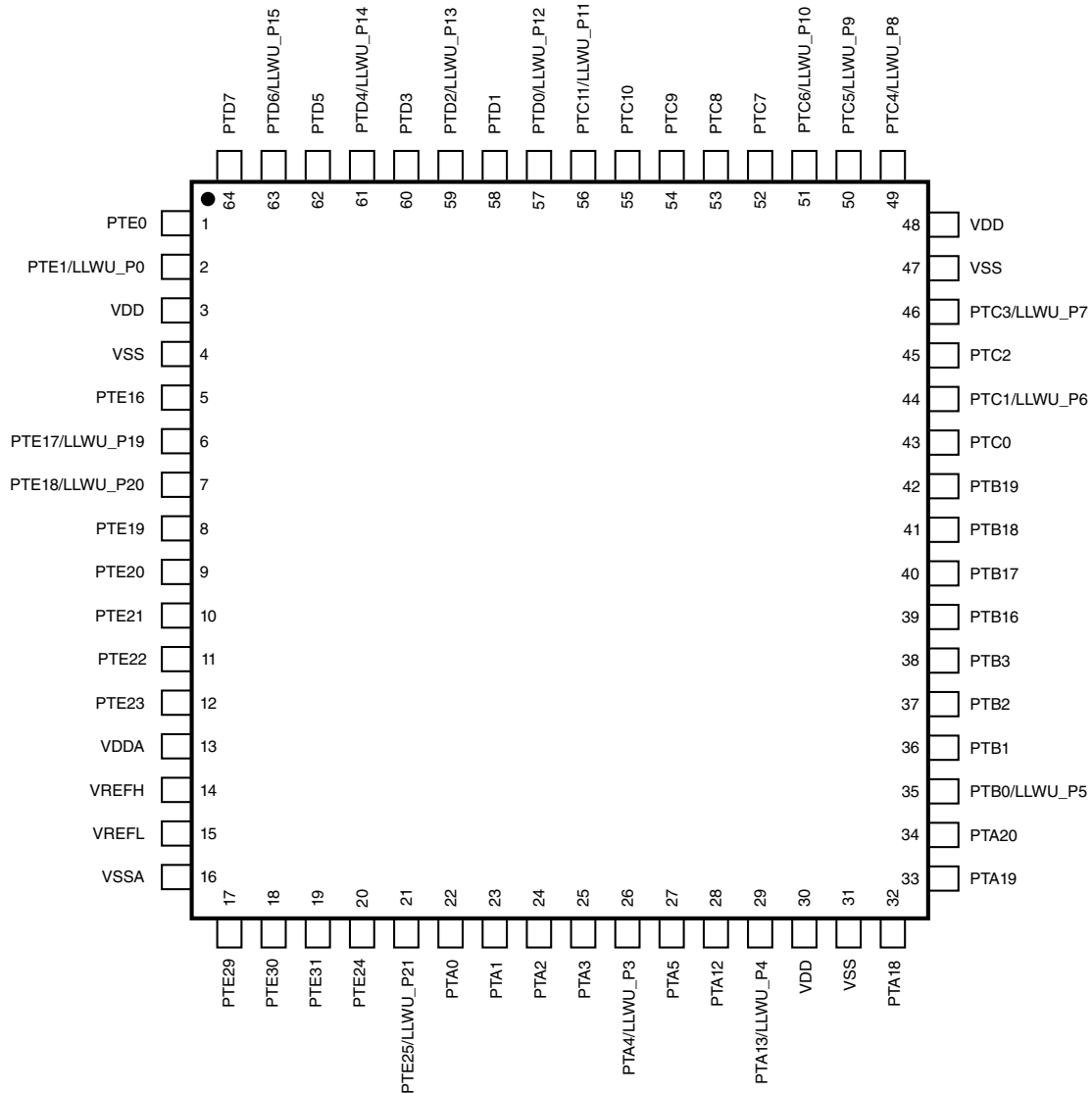


Figure 18. 64 LQFP Pinout Diagram

Pinout

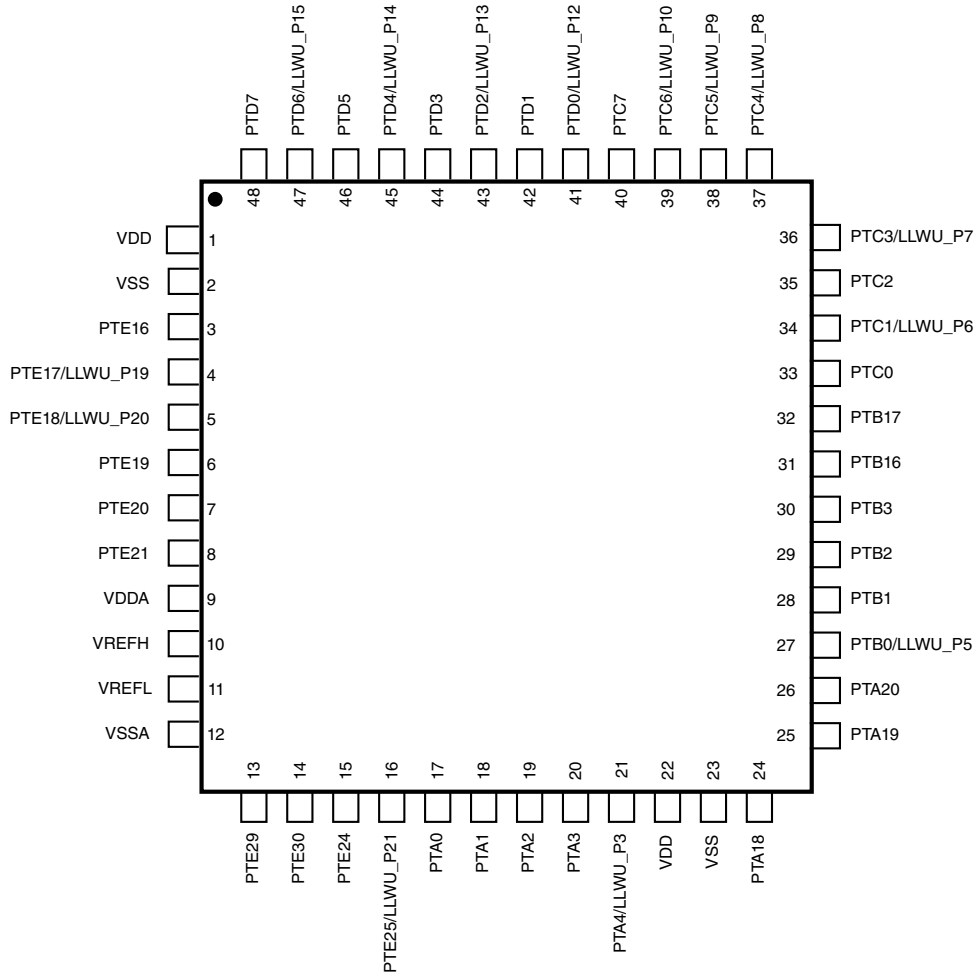


Figure 19. 48 QFP Pinout Diagram

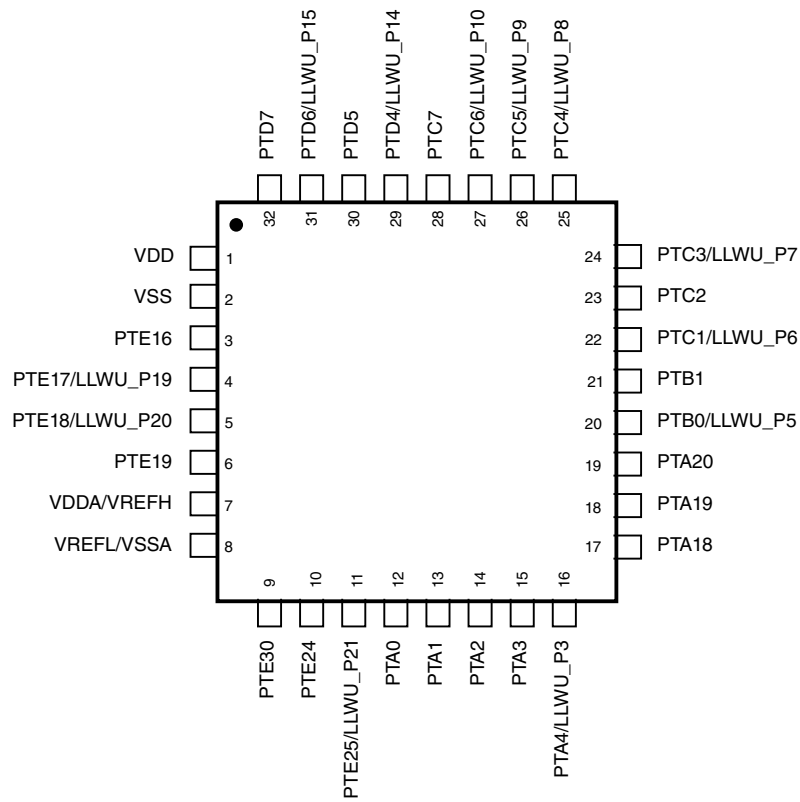


Figure 20. 32 LQFP Pinout Diagram

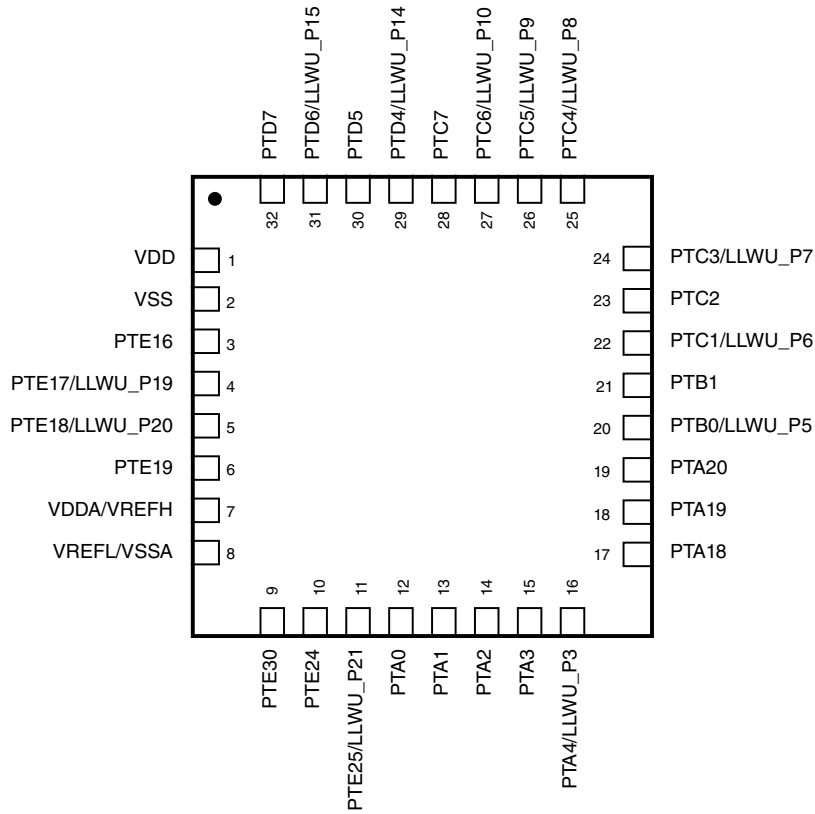


Figure 21. 32 QFN Pinout Diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the MKV11 device numbers.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KV## M FFF R T PP CC S N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

| Field | Description | Values |
|-------|-----------------------------|---|
| Q | Qualification status | <ul style="list-style-type: none"> M = Fully qualified, general market flow P = Prequalification |
| KV## | Kinetis family | <ul style="list-style-type: none"> KV10 and KV11 |
| M | Key attribute | <ul style="list-style-type: none"> Z = M0+ core |
| FFF | Program flash memory size | <ul style="list-style-type: none"> 128 = 128 KB |
| T | Temperature range (°C) | <ul style="list-style-type: none"> V = -40 to 105 |
| PP | Package identifier | <ul style="list-style-type: none"> LC = 32 LQFP (7 mm x 7 mm) FM = 32 QFN (5 mm x 5 mm) LF = 48 LQFP (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) |
| CCC | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> 7 = 75 MHz |
| S | Software type | <ul style="list-style-type: none"> (Blank) = Not software enabled |
| N | Packaging type | <ul style="list-style-type: none"> R = Tape and reel (Blank) = Trays |

7.4 Example

This is an example part number:

MKV11Z128VFM7

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | 0.9 | 1.1 | V |

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|--|------|------|------|
| I _{WP} | Digital I/O weak pullup/pulldown current | 10 | 130 | μA |

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|--------|------------------------------------|------|------|------|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

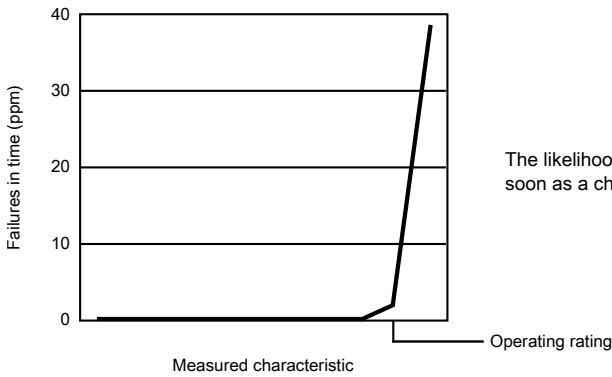
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

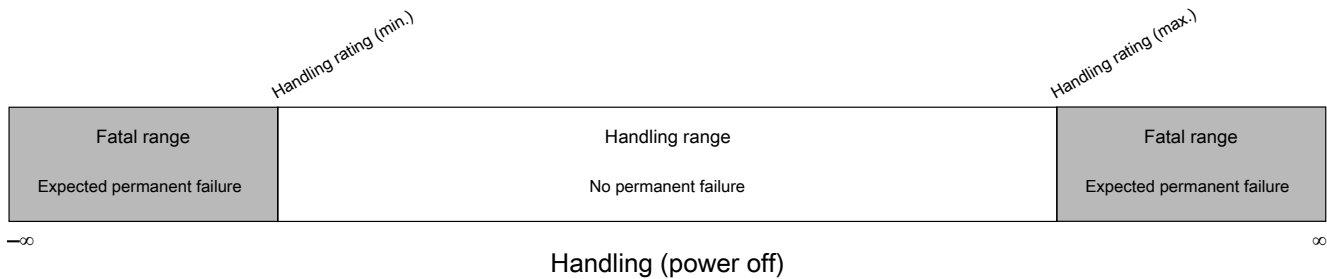
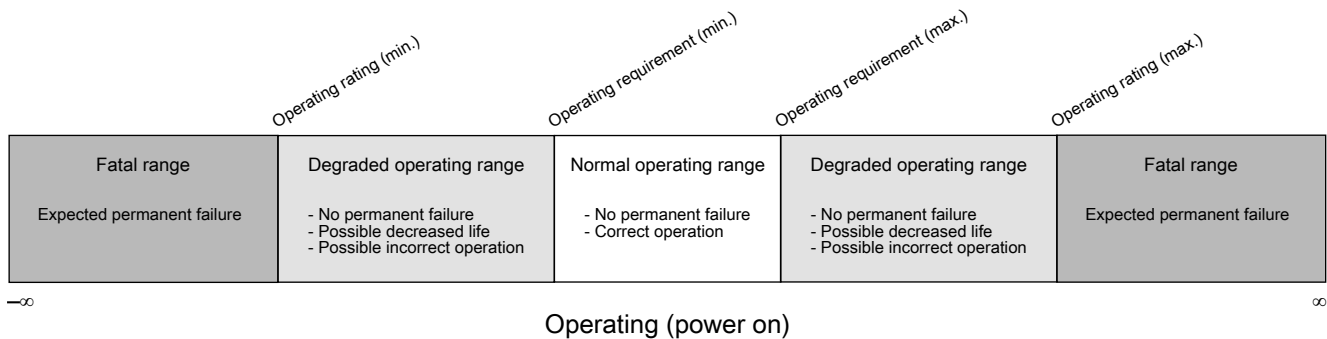
This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|-----------------|------------------------------|------|------|------|
| V _{DD} | 1.0 V core supply voltage | −0.3 | 1.2 | V |

8.5 Result of exceeding a rating



8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

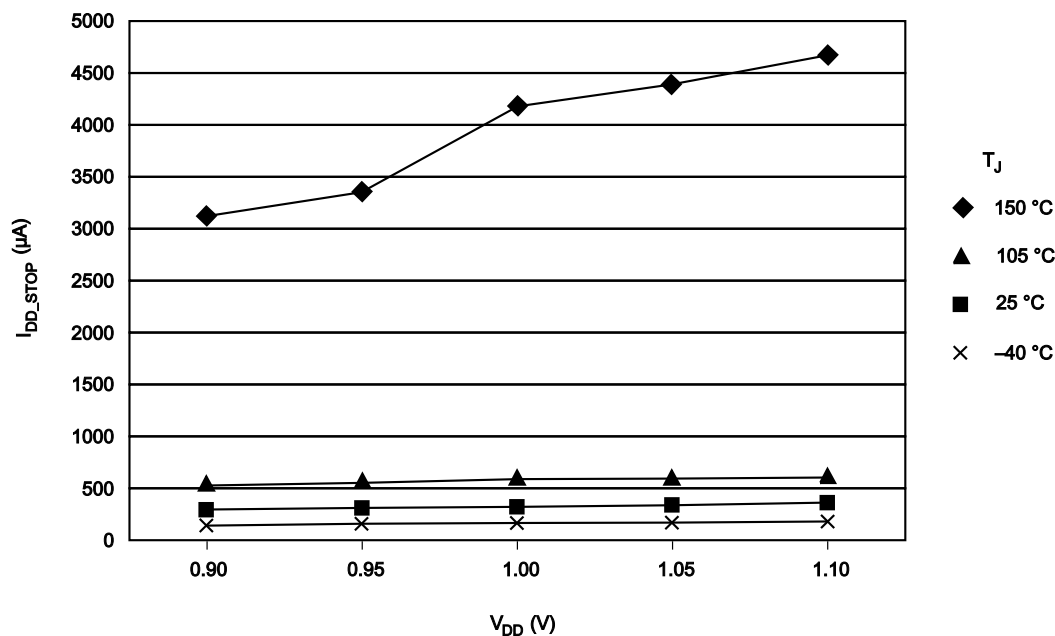
This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|----------|--|------|------|------|---------|
| I_{WP} | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | μA |

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

Revision history



8.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|-----------------|----------------------|-------|------|
| T _A | Ambient temperature | 25 | °C |
| V _{DD} | 3.3 V supply voltage | 3.3 | V |

9 Revision history

The following table provides a revision history for this document.

Table 30. Revision history

| Rev. No. | Date | Substantial Changes |
|----------|---------|---|
| 0 | 11/2014 | Initial Prelim release. |
| 1 | 02/2015 | Updated the following sections: <ul style="list-style-type: none"> • DSPI switching specifications (limited voltage range) • DSPI switching specifications (full voltage range) • KV11 Signal Multiplexing and Pin Assignments |

Table continues on the next page...

Table 30. Revision history (continued)

| Rev. No. | Date | Substantial Changes |
|----------|---------|---|
| 2 | 04/2015 | <p>Updated the following sections:</p> <ul style="list-style-type: none"> • Power mode transition operating behaviors • Power consumption operating behaviors • 16-bit ADC operating conditions • Fields <ul style="list-style-type: none"> • Updated the table "16-bit ADC electrical characteristics" with a footnote • Added the figure "Run mode supply current vs. core frequency" to the section "Diagram: Typical IDD_RUN operating behavior" |
| 3 | 06/2015 | <ul style="list-style-type: none"> • Added a footnote to the ambient temperature entry in the table "Thermal operating requirements" |
| 4 | 05/2017 | <ul style="list-style-type: none"> • Added KMS related information in front matter • Added the section "KMS Motor Suite" • Added "S" in the sections "Format" and "Fields" to specify software type in part number • Updated the section "Example" to add an example for KMS part number • Added the KMS supported part numbers in the table "Ordering information" • Updated the table "Related resources," to include references to KMS documents • Updated the figure "KV11 block diagram" • Added a note to the t_{POR} in the table "Power mode transition operating behaviors." • Changed freescale.com to nxp.com throughout |
| 5 | 07/2020 | <ul style="list-style-type: none"> • Removed KMS related information in front matter • Removed the section "KMS Motor Suite" • Updated ARM to Arm in front matter |
| 6 | 10/2020 | <ul style="list-style-type: none"> • Updated Related Resources Table in front matter section |

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Document Number KV11P64M75
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