UJA1161A

Self-supplied high-speed CAN transceiver with Standby mode

Rev. 1 — 23 August 2019 Product data sheet

1. General description

The UJA1161A is a 'self-supplied' high-speed CAN transceiver integrating an ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant HS-CAN transceiver and an internal 5 V CAN supply. The only supply input is a battery connection. The UJA1161A can be operated in a very-low-current Standby mode with bus wake-up capability.

This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

2. Features and benefits

2.1 General

- Self-supplied ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant high-speed CAN transceiver
- Hardware and software compatible with the UJA116x product family and with improved EMC performance
- Loop delay symmetry timing enables reliable communication at data rates up to 2 Mbit/s in the CAN FD fast phase
- Autonomous bus biasing according to ISO 11898-6
- Fully integrated 5 V supply (V_{BUF}) for the CAN transmitter/receiver
- VIO input allows for direct interfacing with 3.3 V to 5 V microcontrollers
- Bus connections are truly floating when power pin BAT is off

2.2 Designed for automotive applications

- ±8 kV ElectrStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins
- ±6 kV ESD protection, according to IEC TS 62228 on the CAN bus pins and on pin BAT
- CAN bus pins short-circuit proof to ±58 V
- Battery and CAN bus pins are protected against automotive transients according to with ISO 7637-3
- Very low quiescent current in Standby mode
- Leadless HVSON14 package (3 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Integrated supply voltage for the CAN transceiver (V_{BUF})

- 5 V nominal output; ±2 % accuracy
- Undervoltage detection at 90 % of nominal value
- Excellent response with a 4.7 μF ceramic output load capacitor

2.4 Power Management

- Standby mode featuring very low supply current
- Remote wake-up capability via standard CAN wake-up pattern

2.5 System control and diagnostic features

- Mode control via STBN pin
- Overtemperature shutdown
- Transmit data (TXD) dominant time-out function

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UJA1161ATK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

4. Block diagram

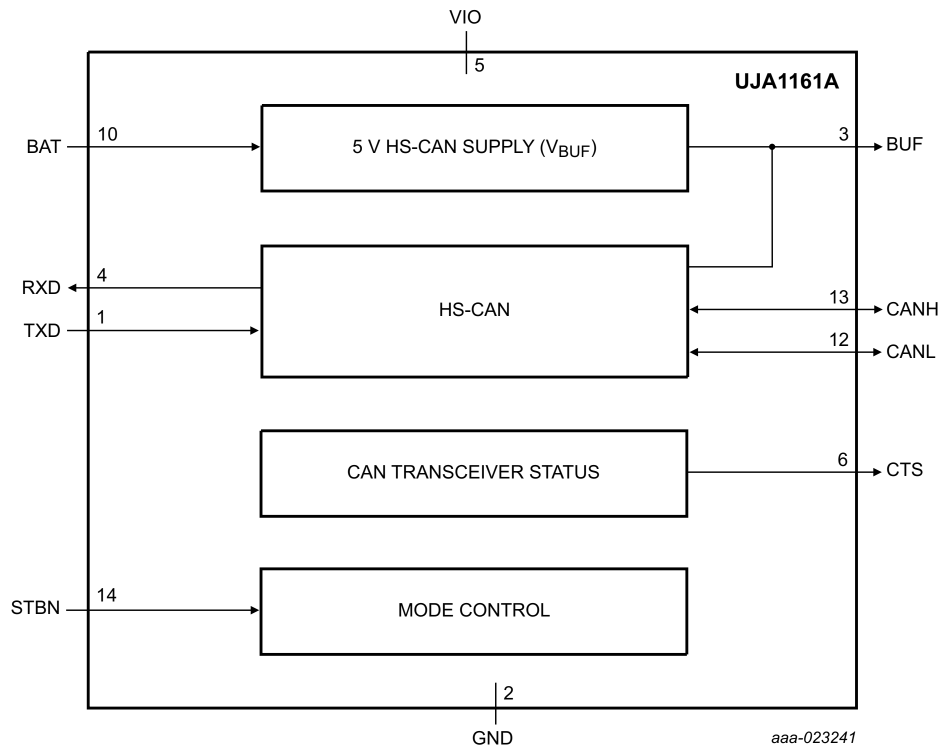


Fig 1. Block diagram of UJA1161A

5. Pinning information

5.1 Pinning

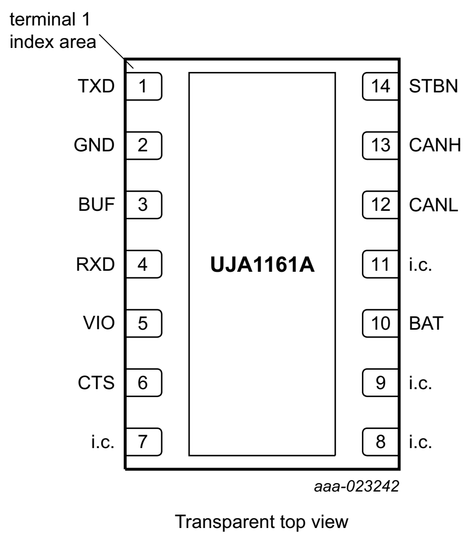


Fig 2. Pin configuration diagram

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground
BUF	3	5 V transceiver supply voltage
RXD	4	receive data output; reads out data from the bus lines
VIO	5	supply voltage for I/O level adaptor
CTS	6	CAN transceiver status output
i.c.	7	internally connected; should be left floating or connected to GND
i.c.	8	internally connected; should be left floating or connected to GND
i.c.	9	internally connected; should be left floating or connected to GND
BAT	10	battery supply voltage
i.c.	11	internally connected; should be left floating or connected to GND
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
STBN	14	standby control input (active LOW)

[1] The exposed die pad at the bottom of the package allows for better heat dissipation and grounding from the transceiver via the printed circuit board. For enhanced thermal and electrical performance, it is recommended to solder the exposed die pad to GND.

6. Functional description

The UJA1161A is a self-supplied high-speed CAN transceiver incorporating a 5 V CAN supply. A variety of fail-safe and diagnostic features offer enhanced system reliability.

6.1 System controller

The system controller is a state machine that manages register configuration and controls the internal functions of the UJA1161A. UJA1161A operating modes and state transitions are illustrated in Figure 3. These modes are discussed in more detail in the following sections.

6.1.1 Operating modes

The UJA1161A supports four operating modes: Normal, Standby, Overtemp and Off.

6.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, the UJA1161A is fully operational. Normal mode can be selected from Standby mode by setting pin STBN HIGH, provided $V_{IO} > V_{uvd(VIO)}$. The UJA1161A exits Normal mode:

- if the microcontroller selects Standby mode by setting pin STBN LOW
- if the UJA1161A detects an undervoltage on VIO, causing the UJA1161A to switch to Standby mode
- if the chip temperature rises above $T_{th(act)otp}$, causing the UJA1161A to switch to Overtemp mode
- if the battery supply voltage drops below $V_{th(det)poff}$, causing the UJA1161A to switch to Off mode

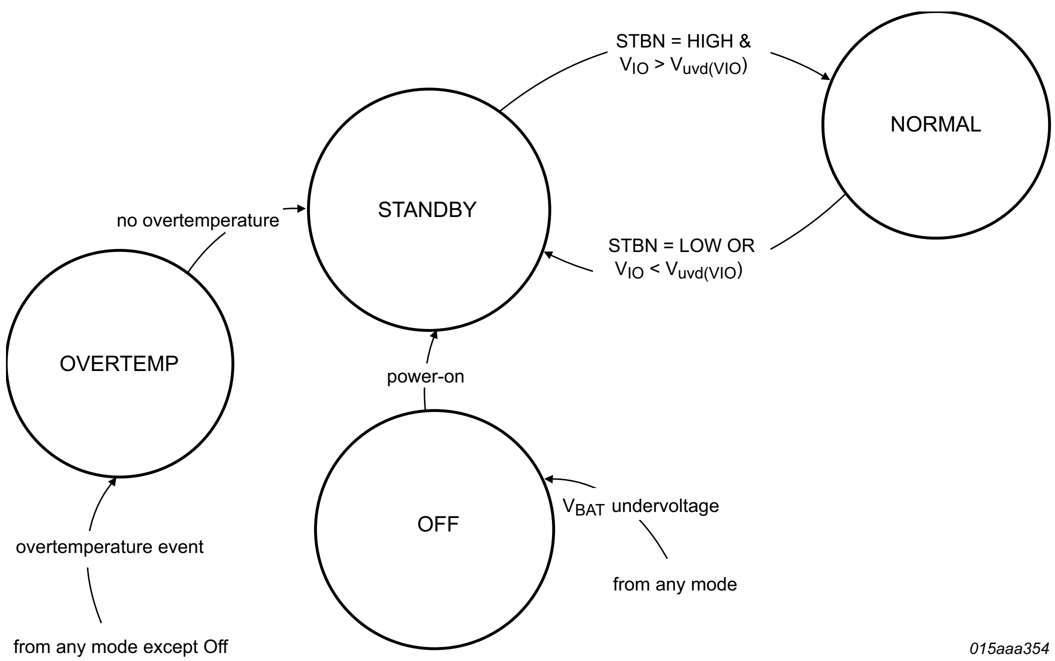


Fig 3. UJA1161A system controller state diagram

6.1.1.2 Standby mode

Standby mode is the power-saving mode of the UJA1161A, offering reduced current consumption. The transceiver is unable to transmit or receive data in Standby mode.

The receiver monitors bus activity for a wake-up request in Standby mode. The bus pins are biased at GND level (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up occurs via a standard wake-up pattern (see Section 6.3.2). Pin RXD is forced LOW when a bus wake-up event is detected.

The UJA1161A switches to Standby mode:

- from Normal mode if pin STBN goes LOW
- from Normal mode if an undervoltage is detected on VIO

6.1.1.3 Off mode

The UJA1161A switches to Off mode from any mode when $V_{BAT} < V_{th(det)poff}$. Only power-on detection is enabled; all other modules are inactive. The UJA1161A starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ (triggering an initialization process) and switches to Standby mode after $t_{startup}$. Pin RXD is driven LOW when the UJA1161A switches from Off mode to Standby mode, to indicate a power-on event has occurred.

In Off mode, the CAN pins disengage from the bus (zero load; high-ohmic).

6.1.1.4 Overtemp mode

Overtemp mode is provided to prevent the UJA1161A being damaged by excessive temperatures. The UJA1161A switches immediately to Overtemp mode from Normal or Standby mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. V_{BUF} is off in Overtemp mode.

The UJA1161A exits Overtemp mode:

- and switches to Standby mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

6.1.1.5 Hardware characterization for the UJA1161A operating modes

Table 3. Hardware characterization by functional block

Block	Operating mode			
	Off	Standby	Normal	Overtemp
V_{BUF}	off	on/off[1]	on	off
CAN	off	Offline	Active	off
RXD	V_{IO} level	V_{IO} level/LOW if wake-up detected	CAN bit stream	V_{IO} level/LOW if wake-up detected

[1] V_{BUF} is switched on in Standby mode if a CAN wake-up pattern is detected on the bus; if pin STBN does not go HIGH within $t_{to(silence)}$, V_{BUF} is switched off again. V_{BUF} is also switched on in Standby mode if STBN goes HIGH to select Normal mode.

6.1.2 Mode control via pin STBN

The UJA1161A can be switched between Normal and Standby modes via the STBN control input (see Figure 3). When STBN goes LOW, the UJA1161A switches to Standby mode. When STBN goes HIGH, the UJA1161A switches to Normal mode.

6.2 Power supplies

6.2.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device needs to be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the UJA1161A switches to Off mode, which means that the internal 5 V CAN supply and other internal logic (except for power-on detection) are shut down.

The UJA1161A switches from Off mode to Standby mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. A power-on event is indicated by a LOW level on pin RXD. RXD remains LOW from the moment UJA1161A exits Off mode until it switches to Normal mode.

6.2.2 CAN supply voltage (V_{BUF})

V_{BUF} provides the internal CAN transceiver with a 5 V supply. The output voltage on BUF is monitored. If V_{BUF} falls below the 90 % undervoltage threshold (90 % of the nominal V_{BUF} output voltage), the CAN transceiver switches to (or remains in) Offline mode.

6.3 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:2016 compliant. The CAN transmitter is supplied from V_{BUF}. The UJA1161A includes additional timing parameters on loop delay symmetry to ensure reliable communication in fast phase at data rates up to 2 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the UJA1161A is in Normal mode with V_{BUF} > 90 % threshold.

Autonomous biasing is active when the UJA1161A is in Standby mode with the CAN transceiver in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller. The transceiver ensures that the CAN bus is correctly biased to avoid disturbing ongoing communication between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

6.3.1 CAN operating modes

The integrated CAN transceiver supports three operating modes: Active, Offline and Offline Bias (see Figure 4). The CAN transceiver operating mode depends on the UJA1161A operating mode and the output voltage on BUF.

6.3.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

The CAN transceiver is in Active mode when:

- UJA1161A is in Normal mode (STBN = 1) AND $V_{BUF} > V_{uvd(BUF)}$ AND $V_{IO} > V_{uvd(VIO)}$

In CAN Active mode, the CAN bias voltage is derived from V_{BUF}. If V_{BUF} falls below $V_{uvd(BUF)}$, the UJA1161A exits CAN Active mode and enters CAN Offline Bias mode with autonomous CAN voltage biasing via pin BAT.

If pin TXD is LOW when the transceiver switches to CAN Active mode (UJA1161A in Normal mode; V_{BUF} and V_{IO} ok), the transmitter and receiver will remain disabled until TXD goes HIGH. This prevents network traffic being blocked for $t_{to(dom)TXD}$ (i.e. while the TXD dominant time-out timer is running; see Section 6.6.1) every time the transceiver enters Active mode, if the TXD pin is clamped permanently LOW.

6.3.1.2 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event. CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active mode when:

- theUJA1161A switches to Standby mode

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver will switch from CAN Active mode to CAN Offline Bias mode if:

- $V_{BUF} < V_{uvd(BUF)}$ OR $V_{IO} < V_{uvd(VIO)}$

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode when the UJA1161A is in Standby mode and no activity has been detected on the bus (no CAN edges) for $t > t_{to(silence)}$ OR
- when the UJA1161A switches from Off or Overtemp mode to Standby mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern is detected on the CAN bus OR
- the UJA1161A switches to Normal mode while $V_{BUF} < V_{uvd(BUF)}$ OR $V_{IO} < V_{uvd(VIO)}$

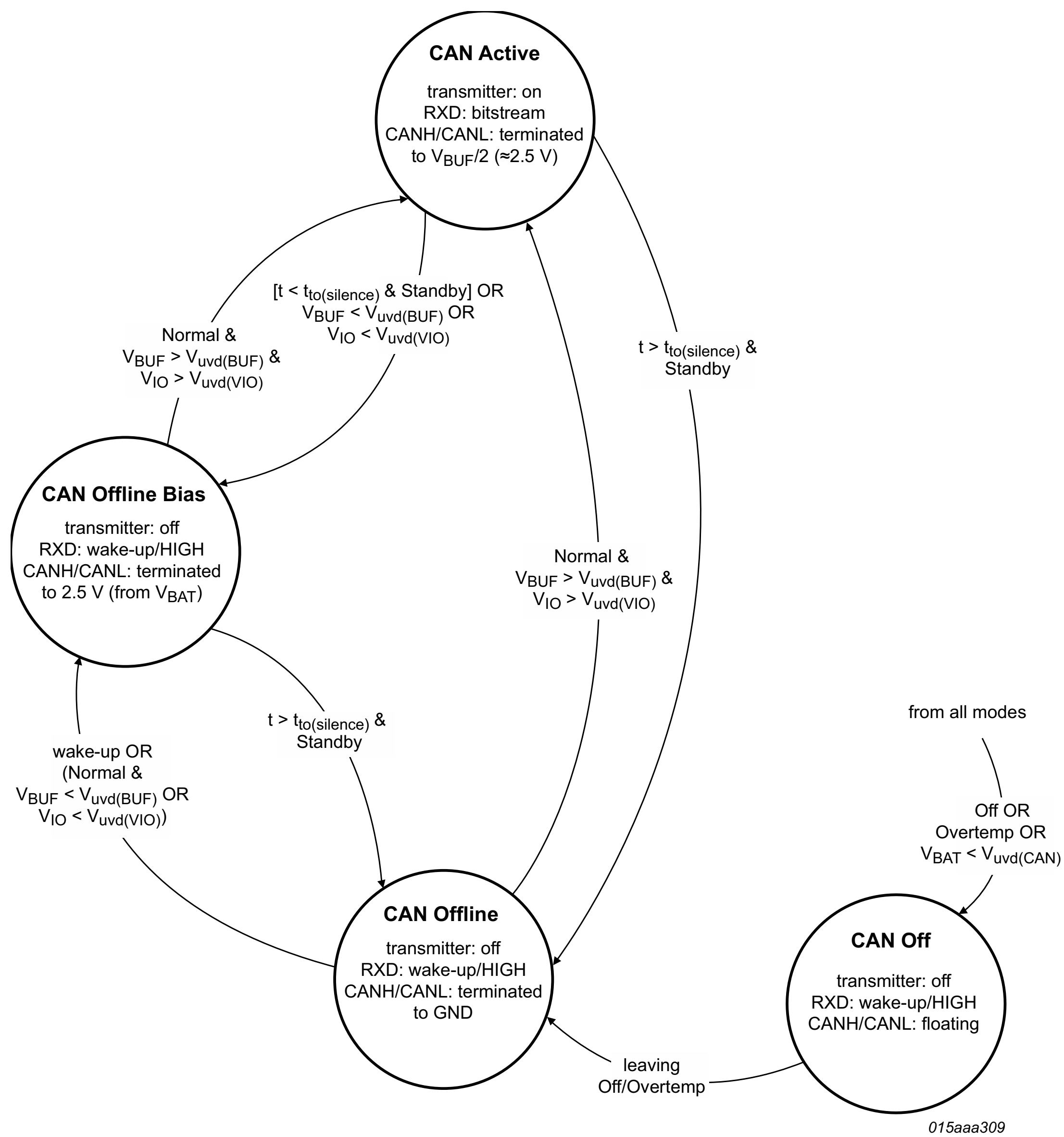


Fig 4. CAN transceiver state machine

6.3.1.3 CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the UJA1161A switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the UJA1161A is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the UJA1161A is lost.

6.3.2 CAN standard wake-up

The UJA1161A monitors the bus for a wake-up pattern when the CAN transceiver is in Offline mode.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up filter and trigger a wake-up event (see Figure 5; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

Pin RXD is driven LOW when a valid CAN wake-up pattern is detected on the bus.

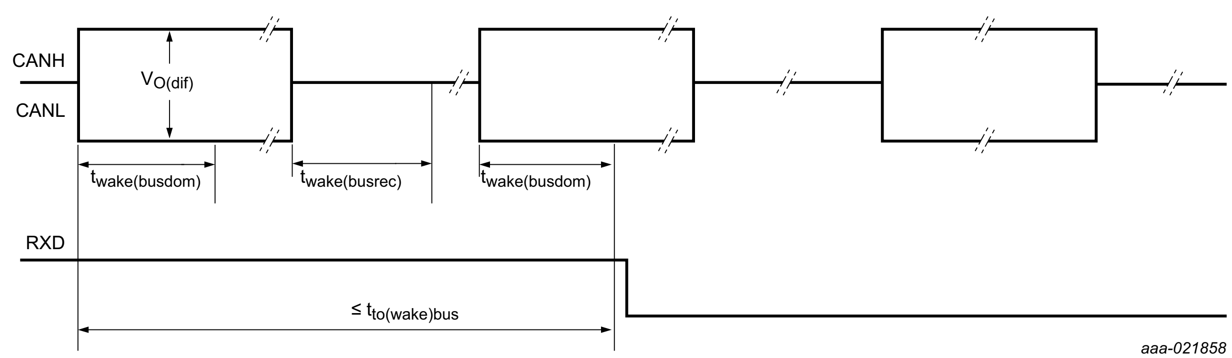


Fig 5. CAN wake-up timing

6.4 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels on TXD, RXD, STBN and CTS to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

6.5 CAN transceiver status pin (CTS)

Pin CTS is driven HIGH to indicate to microcontroller that the transceiver is fully enabled and data can be transmitted and received via the TXD/RXD pins.

Pin CTS is actively driven LOW:

- while the transceiver is starting up (e.g. during a transition from Standby to Normal mode) or

- if pin TXD is clamped LOW for t > $t_{to(dom)TXD}$ or
- if an undervoltage is detected on VIO or BUF

6.6 CAN fail-safe features

6.6.1 TXD dominant timeout

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network traffic). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 4.4 kbit/s.

6.6.2 Pull-up on TXD pin

Pin TXD has an internal pull-up (towards V_{IO}) to ensure a safe defined recessive driver state in case the pin is left floating.

6.6.3 Pull-down on STBN pin

Pin STBN has an internal pull-down (to GND) to ensure the UJA1161A switches to Standby mode if STBN is left floating.

6.6.4 Loss of power at pin BAT

A loss of power at pin BAT has no impact on the bus lines or on the microcontroller. No reverse currents flow from the bus.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x[2]	pins BUF[2], VIO		−0.2	+6	V
		pins TXD, RXD, STBN, CTS	[3]	−0.2	V_{IO} + 0.2	V
		pin BAT		−0.2	+40	V
		pins CANH and CANL with respect to any other pin		−58	+58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL			−40	+40	V
V_{trt}	transient voltage	on pins CANL, CANH, BAT	[4]			
		pulse 1		−100	-	V
		pulse 2a		-	75	V
		pulse 3a		−150	-	V
		pulse 3b		-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) discharge circuit	[5]			
		on pins CANH and CANL; pin BAT with capacitor		−6	+6	kV
		Human Body Model (HBM)				
		on any pin	[6]	−2	+2	kV
		on pin BAT	[7]	−4	+4	kV
		on pins CANH, CANL	[8]	−8	+8	kV
		Machine Model (MM)	[9]			
		on any pin		−100	+100	V
		Charged Device Model (CDM)	[10]			
		on corner pins		−750	+750	V
		on any other pin		−500	+500	V
T_{vj}	virtual junction temperature		[11]	−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] When the device is not powered up, I_{BUF} (max) = 25 mA.

[3] Maximum voltage should never exceed 6 V.

[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2.

[5] Verified by an external test house according to IEC TS 62228, Section 4.3.

[6] According to AEC-Q100-002.

[7] Pins stressed to reference group containing all grounds, emulating the application circuit (Figure 9). HBM pulse as specified in AEC-Q100-002 used.

[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 9). HBM pulse as specified in AEC-Q100-002 used.

[9] According to AEC-Q100-003.

[10] According to AEC-Q100-011.

[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	[1]	60	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

9. Static characteristics

Table 6. Static characteristics

T_{vj} = –40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} rising	4.2	-	4.55	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} rising	4.5	-	5	V
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	V_{BAT} falling	4.2	-	4.55	V
I_{BAT}	battery supply current	Normal mode; CAN Active mode				
		CAN recessive; V_{TXD} = V_{IO}	-	4	7.5	mA
		CAN dominant; V_{TXD} = 0 V	-	46	67	mA
		Standby mode; CAN Offline mode; –40 °C < T_{vj} < +50 °C; V_{BAT} = 7 V to 18 V	-	[2]	91	μA
		additional current in CAN Offline Bias mode; –40 °C < T_{vj} < 85 °C	-	38	55	μA
Voltage source; pin BUF						
V_O	output voltage	V_{BAT} = 5.5 V to 28 V	4.9	5	5.1	V
V_{uvd}	undervoltage detection voltage		4.5	-	4.75	V
$I_{O(sc)}$	short-circuit output current		–300	-	–150	mA
Supply; pin VIO						
V_{uvd}	undervoltage detection voltage		2.7	-	2.85	V
$I_{I(VIO)}$	input current on pin VIO	Standby/Normal mode; –40 °C < T_{vj} < 85 °C	-	7.1	11	μA
Standby mode control input; pin STBN						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V
R_{pd}	pull-down resistance		40	60	80	kΩ
CAN transmit data input; pin TXD						
$V_{th(sw)}$	switching threshold voltage		$0.25V_{IO}$	-	$0.75V_{IO}$	V

Table 6. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.05V_{BUF}$	-	-	V
R_{pu}	pull-up resistance		40	60	80	kΩ
CAN transmitter status; pin CTS						
I_{OH}	HIGH-level output current	V_{CTS} = V_{IO} − 0.4 V; transmitter on	-	-	−4	mA
I_{OL}	LOW-level output current	V_{CTS} = 0.4 V; transmitter off	4	-	-	mA
CAN receive data output; pin RXD						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	V_{IO} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
R_{pu}	pull-up resistance	CAN Offline mode	40	60	80	kΩ
High-speed CAN bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{TXD} = 0 V; ; t < $t_{to(dom)TXD}$; V_{BAT} > 5.5 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{BUF} − V_{CANH} − V_{CANL}; V_{BAT} > 5.5 V	−400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz; C_{SPLIT} = 4.7 nF [3] [4]	$0.9V_{BUF}$	-	$1.1V_{BUF}$	V
$V_{O(dif)}$	differential output voltage	CAN Active mode (dominant); V_{TXD} = 0 V; V_{BAT} > 5.5 V; t < $t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; R_L = no load; V_{BAT} > 5.5 V				
		CAN Active/Offline Bias mode; V_{TXD} = V_{IO}	−50	-	+50	mV
		CAN Offline mode	−0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	CAN Active mode; V_{TXD} = V_{IO}; V_{BAT} > 5.5 V; R_L = no load	2	$0.5V_{BUF}$	3	V
		CAN Offline mode; V_{BAT} > 5.5 V; R_L = no load	−0.1	-	+0.1	V
		CAN Offline Bias mode; R_L = no load	2	2.5	3	V

Table 6. Static characteristics *...continued*
T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

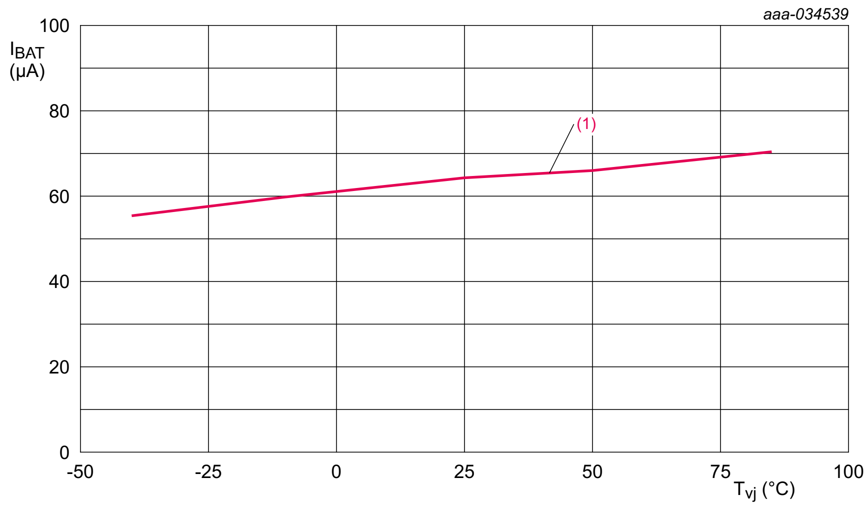
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{O(sc)dom}$	dominant short-circuit output current	CAN Active mode; V_{BAT} > 5.5 V; V_{TXD} = 0 V				
		pin CANH; V_{CANH} = −3 V to +27 V	−55	-	-	mA
		pin CANL; V_{CANL} = −15 V to 18 V	-	-	+55	mA
$I_{O(sc)rec}$	recessive short-circuit output current	V_{CANL} = V_{CANH} = −27 V to +32 V; V_{TXD} = V_{IO}	−3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active mode	0.5	0.7	0.9	V
		CAN Offline mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active mode	−4[3]	-	+0.5	V
		CAN Offline/Offline Bias modes	−4[3]	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active mode	0.9	-	9.0[3]	V
		CAN Offline/Offline Bias modes	1.15	-	9.0[3]	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active mode; −12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V	1	30	60	mV
R_i	input resistance	−2 V ≤ V_{CANL} ≤ +7 V; −2 V ≤ V_{CANH} ≤ +7 V	9	15	28	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	−1	-	+1	%
$R_{i(dif)}$	differential input resistance	−2 V ≤ V_{CANL} ≤ +7 V; −2 V ≤ V_{CANH} ≤ +7 V	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	10	pF
I_L	leakage current	V_{BAT} = V_{BUF} = 0 V or V_{BAT} = V_{BUF} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	−5	-	+5	μA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		167	177	187	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		127	137	147	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 6.

[3] Not tested in production; guaranteed by design.

[4] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 11.



(1) Standby Mode: CAN Offline mode, V_{BAT} = 12 V, I_{BUF} = 0 μA.

Fig 6. UJA1161A typical Standby quiescent current (μA)

10. Dynamic characteristics

Table 7. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage sources; pins BUF and VIO						
$t_{startup}$	start-up time	from V_{BAT} exceeding the power-on detection threshold until V_{BUF} > 90 % undervoltage threshold; C_{BUF} = 4.7 μF	-	2.8	4.7	ms
$t_{d(uvd)}$	undervoltage detection delay time		6	-	54	μs
Mode control: pin STBN						
$t_{fltr(stb)}$	standby filter time		2.5	-	13.5	μs
CAN transceiver timing; pins CANH, CANL, TXD and RXD						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	[2]	-	80	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	[2]	-	80	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	[2]	-	105	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	[2]	-	120	-	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	$t_{bit(TXD)}$ = 200 ns [3]	-	-	255	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	$t_{bit(TXD)}$ = 200 ns [3]	-	-	255	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns [3]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns [3]	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns [3]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns [3]	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	−65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	−45	-	+15	ns
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	1.8	μs
		second pulse for wake-up on pins CANH and CANL	0.5	-	1.8	μs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	1.8	μs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	1.8	μs
$t_{to(wake)bus}$	bus wake-up time-out time	between first and second dominant pulses; CAN Offline mode	0.8	-	10	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; V_{TXD} = 0 V	2.7	-	3.3	ms
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes	0.95	-	1.17	s
$t_{d(busact-bias)}$	delay time from bus active to bias		-	-	200	μs

Table 7. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup(CAN)}$	CAN start-up time	when switching to Active mode (CTS = HIGH)	-	-	220	μs
Mode transition						
$t_{d(act)norm}$	normal mode activation delay time	delay before CAN transceiver is activated after the UJA1161A enters Normal mode	-	-	320	μs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 7 and Figure 10.

[3] See Figure 8 and Figure 10.

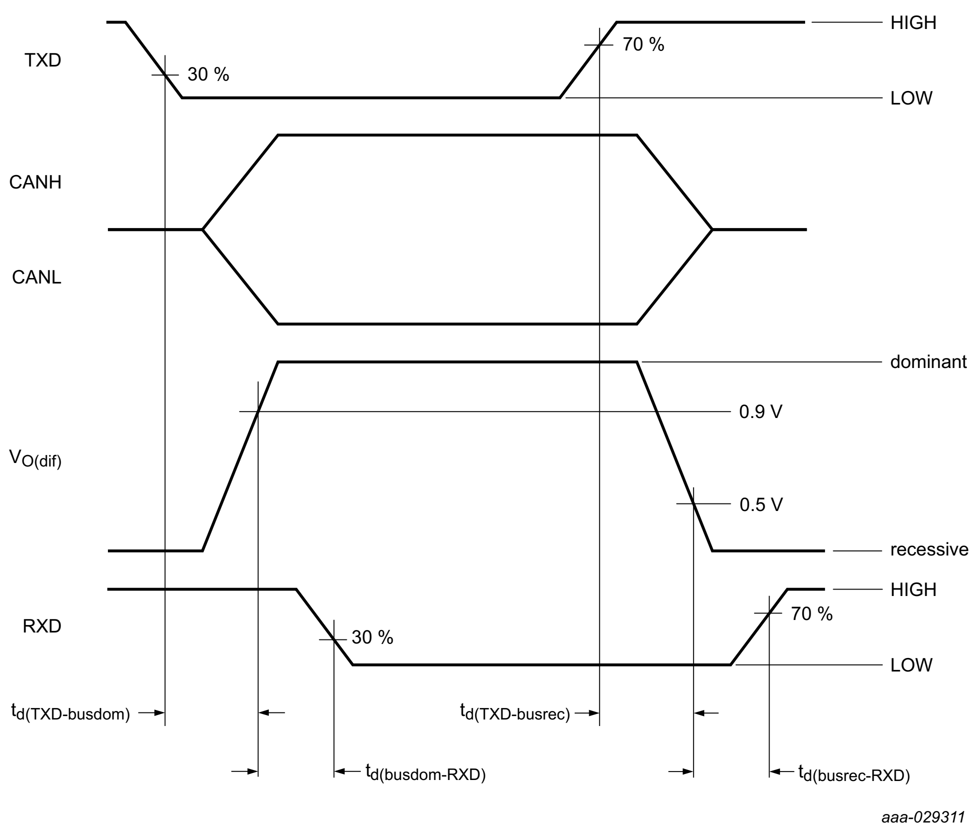


Fig 7. CAN transceiver timing diagram

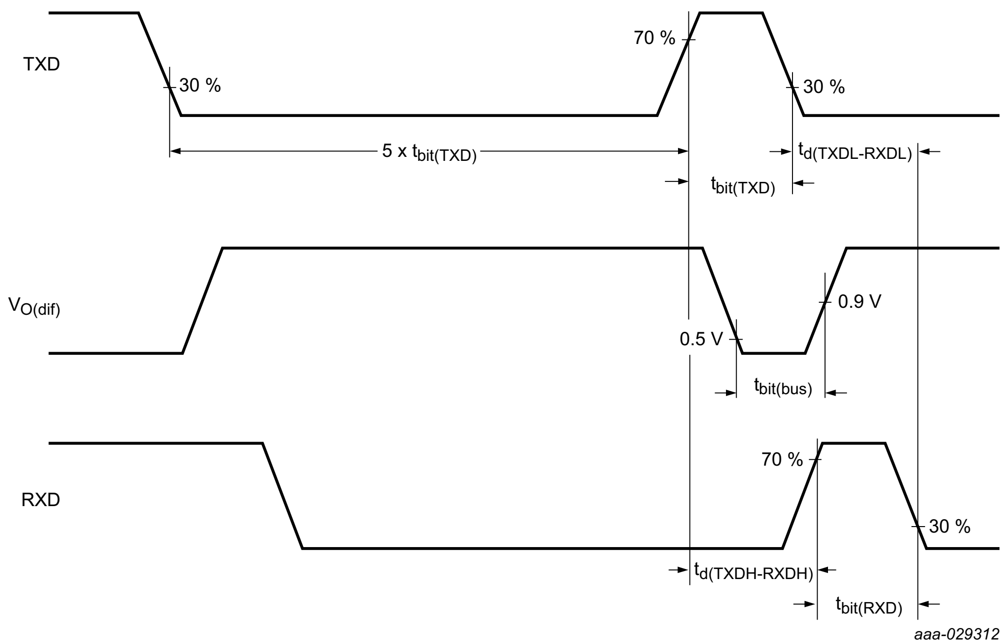
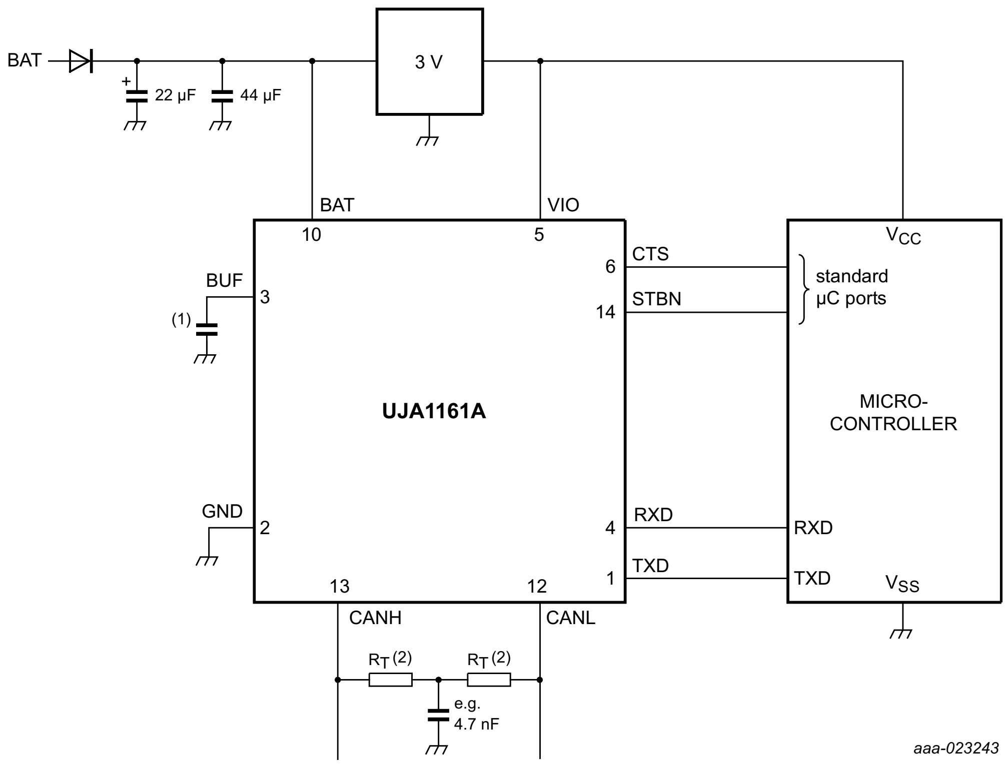


Fig 8. Loop delay symmetry timing diagram

11. Application information

11.1 Application diagram



(1) Actual capacitance value must be a least 1.76 µF with 5 V DC offset (recommended capacitor value is 6.8 µF).

(2) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 9. Typical application using the UJA1161A

12. Test information

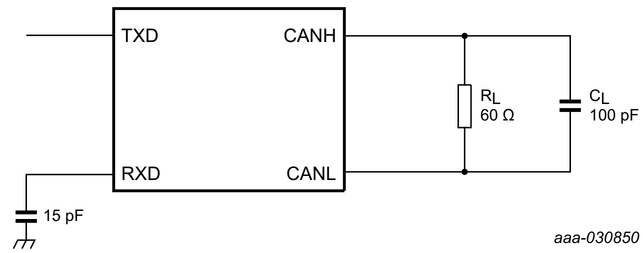


Fig 10. Timing test circuit for CAN transceiver

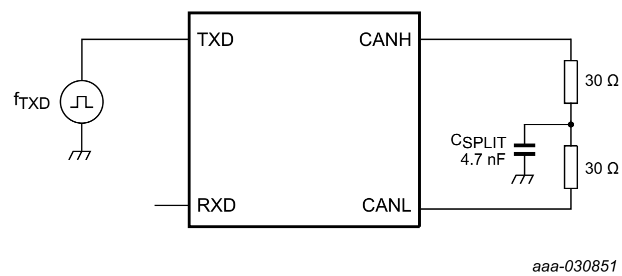


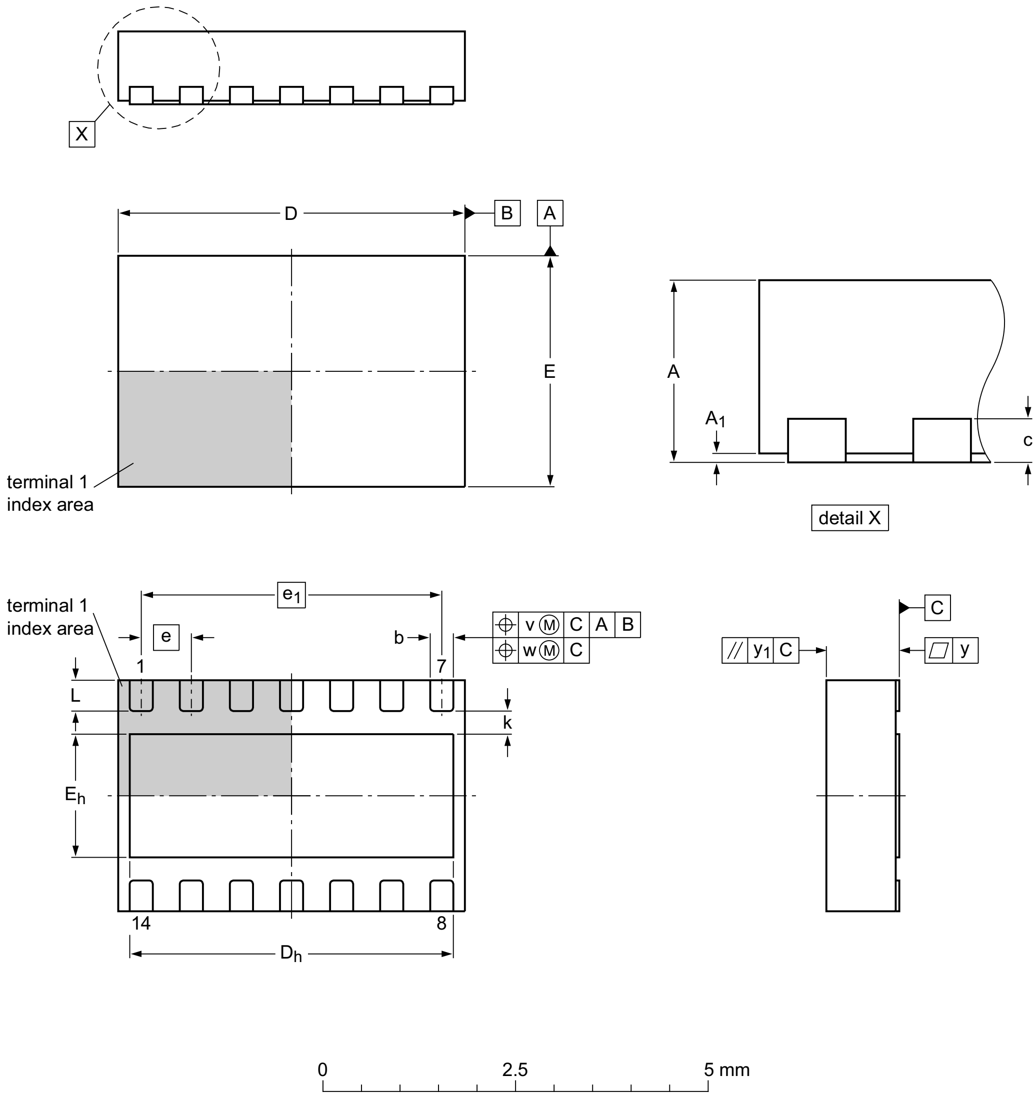
Fig 11. Test circuit for measuring transceiver driver symmetry

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13. Package outline

HVSON14: plastic, thermal enhanced very thin small outline package; no leads;
14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

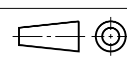
Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Fig 12. Package outline SOT1086-2 (HVSON14)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020D)

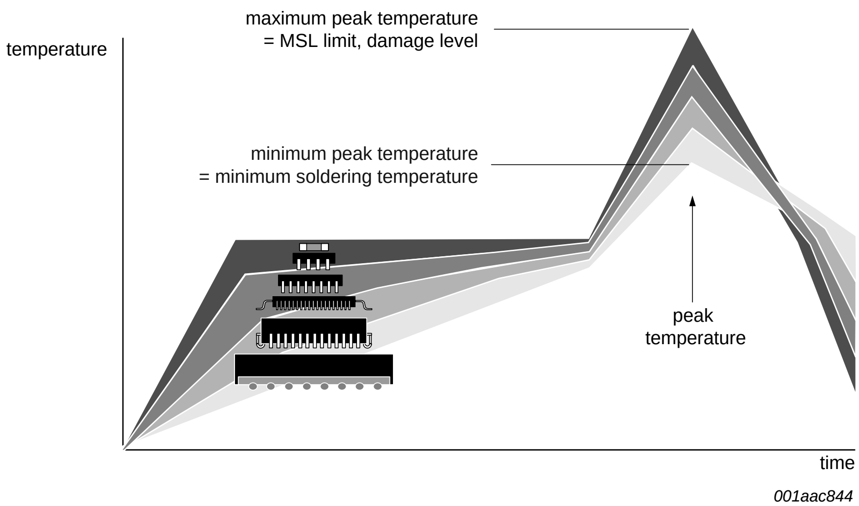
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16. Soldering of HVSON packages

Section 15 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 ‘Surface mount reflow soldering description”*
- *AN10366 “HVQFN application information”*

17. Appendix: ISO 11898-2:201x parameter cross-reference list

Table 10. ISO 11898-2:201x to NXP data sheet parameter conversion

ISO 11898-2:201x		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry

Table 10. ISO 11898-2:201x to NXP data sheet parameter conversion

ISO 11898-2:201x		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1]	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(busrec)}$[1]	bus recessive wake-up time
Wake-up timeout, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	delay time from bus active to bias

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

18. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UJA1161A v.1	20190823	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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21. Contents

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