LED Control IC
W2RG012RN

Optimal IC for LED Control

- An exponential function-based PWM gradation control for up to 256 gradations, enabling beautiful fade-in and fade-out.
- Dynamic drive of LEDs connected in a matrix form; individual control of up to 128 LED Lines.
- Serial bus connection permitting connection of up to 15 ICs on the same communication line.
- 24 constant current outputs contained in a small package of 7 x 7 mm.
- Built-in thermal shutdown.
- RoHS Compliant

Ordering Information

Description	Model
LED Control IC	**W2RG012RN**

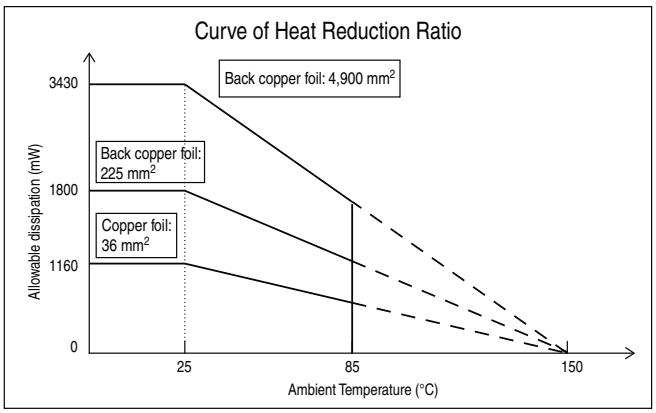
Specifications

Absolute Maximum Ratings

Item	Symbol	Rating	Applicable Terminal
Supply Voltage	V_{DD}	-0.3 to 7.0 V	V_{DD}
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3 ≤ 7.0 V	SDA, SCL, $\overline{RST}$, $\overline{CE}$, ADR1, ADR0, DIV, COM
Signal Output Voltage	V_{SOUT}	-0.3 to V_{DD} + 0.3 ≤ 7.0 V	SDO, OUTDC
Drive Output Voltage	V_{DOUT}	-0.3 to 20 V	OUT0R~7R, OUT0G~7G, OUT0B~7B, OUTS0~S3
Drive Output Current/pin (See note 1)	I_{DOUT}	80 mA	OUT0R~7R, OUT0G~7G, OUT0B~7B
Switch Output Current/pin	I_{DOUTS}	20 mA	OUTS0~S3
Allowable Power Dissipation (See note 2)	Pd1	3.43 W	- - -
	Pd2	1.80 W	- - -
	Pd3	1.16 W	- - -
Ambient Operating Temperature	T_{OPR}	-20 to 85 °C	- - -
Ambient Storage Temperature	T_{STG}	-40 to 150 °C	- - -

Note: **1.** Take the power consumption and allowable power dissipation rating into consideration.
2. Values when the product is mounted on a standard substrate (70 mm x 70 mm x1.6 mmt, FR-4).
When using the product at Ta = 25°C or higher, the values must be decreased using the constant of temperature decrease R_{td} [mW/°C].

Pd1: R_{td} = 27.4 mW/°C for a double-sided substrate with a back layer copper foil area of 4,900 mm^2
Pd2: R_{td} = 14.4 mW/°C for a double-sided substrate with a back layer copper foil area of 225 mm^2
Pd3: R_{td} = 9.28 mW/°C for a single-sided substrate with a copper foil area of 36 mm^2



Recommended Operating Conditions

Item	Symbol	Rating	Applicable Terminal
Supply Voltage	V_{DD}	3.0 to 5.5 V	V_{DD}
Input Voltage	V_{IN}	0 to V_{DD} V	SDA, SCL, $\overline{RST}$, $\overline{CE}$, ADR1, ADR0, DIV, COM
Signal Output Current	I_{SOUT}	-10 to 10 mA	SDO, OUTDC
Communication Clock Frequency (See note 1)	f_{SCL}	Max. 5 MHz	SCL

Note: 1. Take the timing characteristics into consideration.

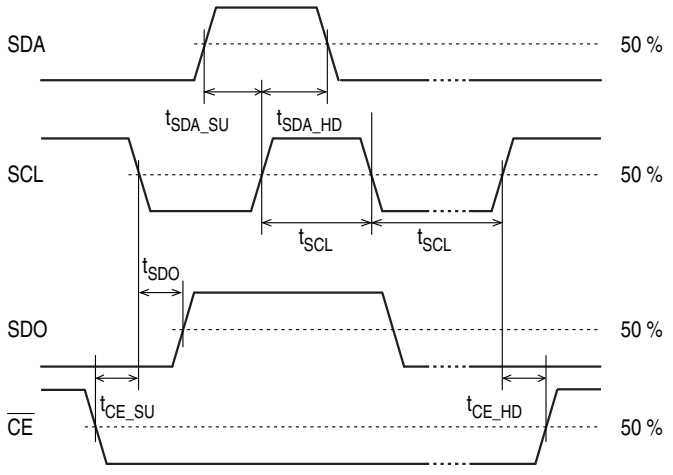
DC Electrical Characteristics (Ta = 25°C, V_{DD} = 5V)

Item	Symbol	Condition	Spec.			Unit	Applicable terminal
			Min.	Typ.	Max.		
High-level Input Voltage	V_{IH}	- - -	V_{DD} x 0.7	- - -	- - -	V	SDA, SCL, $\overline{RST}$, $\overline{CE}$
Low-level Input Voltage	V_{IL}	- - -	- - -	- - -	V_{DD} x 0.3	V	
A/D Input Voltage	V_{AD1}	"10" output	V_{DD} x 0.9	- - -	V_{DD} + 0.3	V	ADR1, ADR0, DIV, COM
	V_{AD2}	"11" output	V_{DD} x 0.6	- - -	V_{DD} x 0.7	V	
	V_{AD3}	"01" output	V_{DD} x 0.3	- - -	V_{DD} x 0.4	V	
	V_{AD4}	"00" output	-0.3	- - -	V_{DD} x 0.1	V	
High-level Signal Output Voltage	V_{SOH}	I_{SOUT} = -5 mA	V_{DD} - 0.5	- - -	- - -	V	SDO, OUTDC
Low-level Signal Output Voltage	V_{SOL}	I_{SOUT} = 5 mA	- - -	- - -	0.5	V	
ON Resistance1	R_{ON1}	- - -	- - -	6.3	10	Ω	OUT0R~7R OUT0G~7G OUT0B~7B
Inter-pin Current Accuracy	ΔIP	I_{DOUT} = 20 mA	-3	- - -	3	%	
Inter-device Current Accuracy	ΔID	I_{DOUT} = 20 mA	-6	- - -	6	%	
Drive Output Leak Current	I_{DL}	- - -	- - -	- - -	1	μA	
ON Resistance2	R_{ON2}	- - -	- - -	9	20	Ω	OUTS0~S3
Operating Current Consumption	I_{DD}	Total Output: I_{DOUT} = 20 mA	- - -	5	7	mA	V_{DD}

Timing Characteristics (Ta = -20 to 85 °C, V_{DD} = 3.0 to 5.5V)

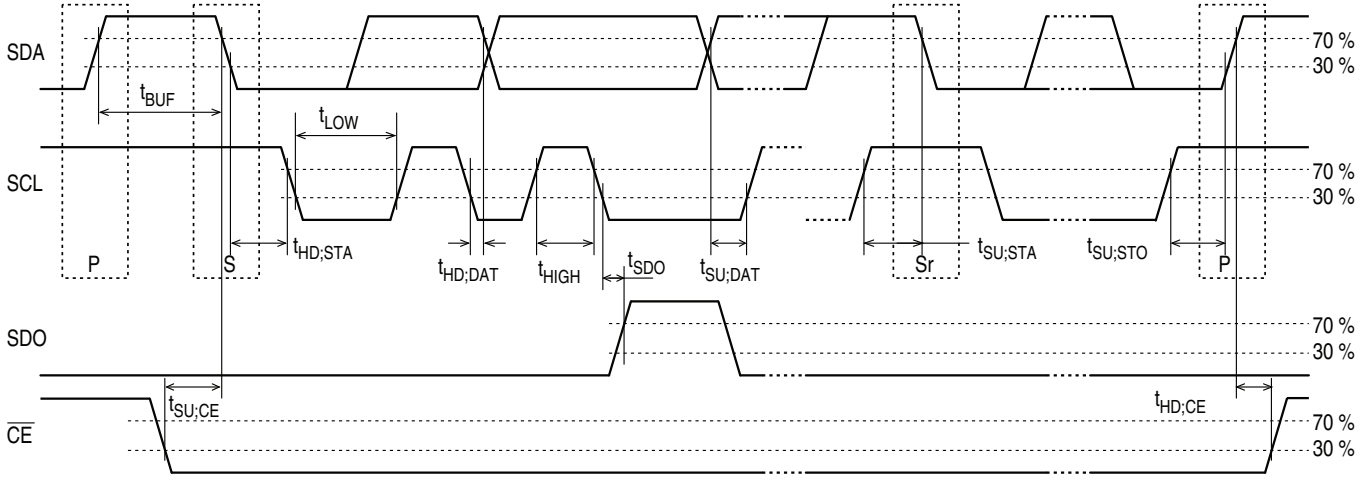
Serial Communication with Address

Item	Symbol	Condition	Spec.			Unit	Applicable terminal
			Min.	Typ.	Max.		
Communication Clock Pulse Width	t_{SCL}	- - -	100	- - -	- - -	ns	SCL
Data Setup Time	t_{SDA_SU}	- - -	90	- - -	- - -	ns	SCL,SDA
Data Hold Time	t_{SDA_HD}	- - -	90	- - -	- - -	ns	
$\overline{CE}$ Setup Time	t_{CE_SU}	- - -	50	- - -	- - -	ns	SCL, SDA, $\overline{CE}$
$\overline{CE}$ Hold Time	t_{CE_HD}	- - -	50	- - -	- - -	ns	
Data Output Time	t_{SDO}	Load capacity: 100 pF	- - -	- - -	80	ns	SCL, SDO



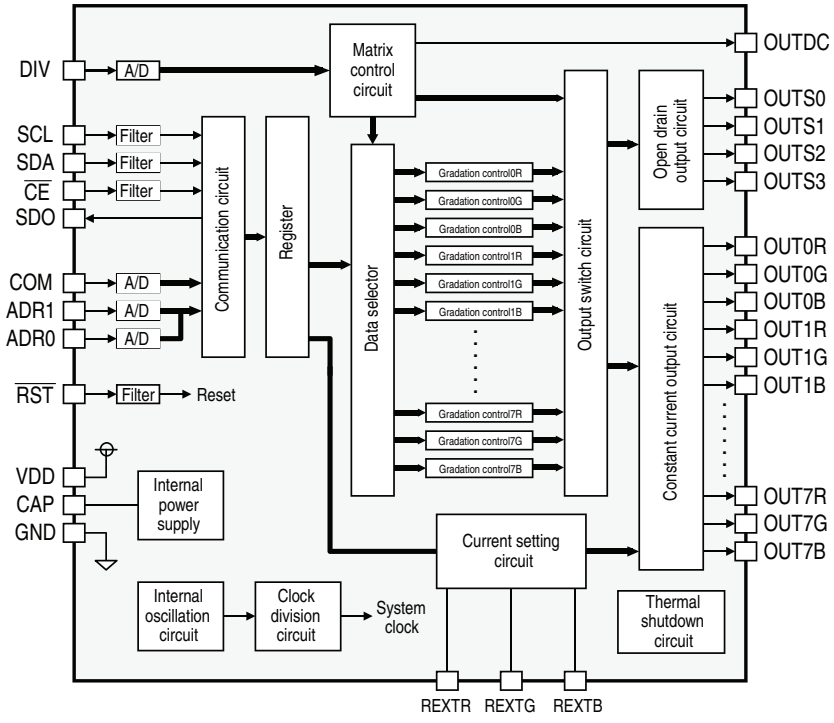
I²C-based Serial Communication

Item	Symbol	Condition	Spec.			Unit	Applicable terminal
			Min.	Typ.	Max.		
Clock "L" Period	t_{LOW}	- - -	50	- - -	- - -	ns	SCL
Clock "H" Period	t_{HIGH}	- - -	50	- - -	- - -	ns	
Bus Freeing Time	t_{BUF}	- - -	80	- - -	- - -	ns	SDA
Start Setup Time	$t_{SU;STA}$	- - -	50	- - -	- - -	ns	SCL,SDA
Start Hold Time	$t_{HD;STA}$	- - -	50	- - -	- - -	ns	
Stop Setup Time	$t_{SU;STO}$	- - -	50	- - -	- - -	ns	
Data Setup Time	$t_{SU;DAT}$	- - -	30	- - -	- - -	ns	
Data Hold Time	$t_{HD;DAT}$	- - -	0	- - -	- - -	ns	
$\overline{CE}$ Setup Time	$t_{SU;CE}$	- - -	50	- - -	- - -	ns	SCL, SDA, $\overline{CE}$
$\overline{CE}$ Hold Time	$t_{HD;CE}$	- - -	50	- - -	- - -	ns	
Data Output Time	t_{SDO}	Load capacity: 100 pF	- - -	- - -	80	ns	SCL, SDO



Engineering Data

Block Diagram



Terminal Designation

Terminal Number	Terminal Name	Description	I/O	Function
1	SDA	Serial data input	I	CMOS, filter
2	SCL	Serial clock input	I	
3	$\overline{CE}$	Chip enable input (See note 1)	I	
4	V_{DD}	Power source	P	
5	CAP	Capacitor (See note 2)	- - -	
6	GND	Ground	P	
7	ADR1	Device address 1	I	Resistance partial pressure input
8	ADR0	Device address 0	I	
9	DIV	Division mode	I	
10	COM	Communication mode	I	
11	REXTR	Current setting resistance R	- - -	
12	REXTG	Current setting resistance G	- - -	
13	REXTB	Current setting resistance B	- - -	
14	OUT0R	Output 0R	O	Constant Current
15	OUT0G	Output 0G	O	
16	OUT0B	Output 0B	O	
17	GND	Ground	P	
18	OUT1R	Output 1R	O	Constant Current
19	OUT1G	Output 1G	O	
20	OUT1B	Output 1B	O	
21	OUT2R	Output 2R	O	
22	OUT2G	Output 2G	O	
23	GND	Ground	P	
24	OUT2B	Output 2B	O	Constant Current
25	OUT3R	Output 3R	O	
26	OUT3G	Output 3G	O	
27	OUT3B	Output 3B	O	
28	OUT4R	Output 4R	O	
29	OUT4G	Output 4G	O	
30	OUT4B	Output 4B	O	
31	GND	Ground	P	
32	OUT5R	Output 5R	O	Constant Current
33	OUT5G	Output 5G	O	
34	OUT5B	Output 5B	O	
35	OUT6R	Output 6R	O	
36	OUT6G	Output 6G	O	
37	GND	Ground	P	
38	OUT6B	Output 6B/Output switch 4	O	Constant Current
39	OUT7R	Output 7R/Output switch 5	O	
40	OUT7G	Output 7G/Output switch 6	O	
41	OUT7B	Output 7B/Output switch 7	O	
42	OUTS0	Output switch 0	O	N-ch open drain
43	OUTS1	Output switch 1	O	
44	OUTS2	Output switch 2	O	
45	OUTS3	Output switch 3	O	
46	OUTDC	Synchronous control output	O	CMOS
47	SDO	Serial data output	O	
48	$\overline{RST}$	Reset (See note 3)	I	CMOS, filter, pull-up

Note: 1. When $\overline{CE}$ terminal is not used, keep it in L fixing condition. (This does not apply to CE-D8 mode.)

2. CAP terminal is connected to capacitor for power smoothing. Connect a 0.1 μF capacitor between the terminal and GND.

3. A 100 kΩ pullup resistance is built in the $\overline{RST}$ terminal. It is recommended that when the terminal is not used, a 0.1 μF capacitor be connected between the terminal and GND to ensure stable operation.

4. Leave unused output terminals open.

Operation

■ Functional Overview

LEDs in 24 systems are driven at a constant current or voltage. Also, LEDs connected in a matrix form can be lit dynamically (pulse lighting). For dynamic lighting, LEDs in 48 systems (divided into 2 parts), 96 systems (divided into 4 parts), or 128 systems (divided into 8 parts) can be gradation controlled individually.

Command Reception

An LED lighting command is received via serial communication. Regarding communication method, the product can adapt to three kinds of serial communication with address, and I^2C-based serial communication. LED lighting data for up to 128 units can be transmitted continuously. As only a single operation is required for designation of a start signal or a device address, the overall volume of communication can be reduced.

Gradation Control

A 256-gradation can be used for lighting. Each gradation is allocated to a duty ratio based on the exponential function, to enable lighting design suited to human visual sensation.

Matrix Control

The product is adapted to connection of 24x1, 24x2, 24x4 and 16x8 matrix. Also, lighting errors at switching can be controlled by controlling switch timing for dynamic lighting.

Power-saving Control

For driving, power consumption for LED lighting is controlled to 75%/50%25% of the normal level. Collective switching via communication command can be executed, permitting easy switching between normal and power-saving operations. Either current control or duty ratio control can be selected as control method. For current control, the output current is changed to a 75%/50%/25% level, with the current set with current setting terminal REXTR/REXTG/REXTB as reference. For duty ratio control, the output duty ratio is changed to a 75%/50%/25% level, with the duty ratio allocated to a gradation as reference.

Number of Control Systems

Up to 15 devices can be connected through address designation. This permits the control of LEDs in up to 1,920 systems. Additional devices can be connected by switching the $\overline{CE}$ terminal.

■ Description of Terminals

Setting By Inputting Resistance Partial Pressure

Device address setting terminal (ADR1/ADR0), division mode setting terminal (DIV), and communication mode setting terminal (COM) are level input terminals with an A/D converter built in internal IC. One of 4 voltage levels (GND, V_{DD} x 1/3, V_{DD} x 2/3, and V_{DD}) is set by inputting resistance partial pressure.

Device Address Setting

The device address is set by inputting resistance partial pressure to device address setting terminal (ADR1/ADR0). The address is chosen from among 15 addresses from “0000” to “1110”. “1111” cannot be designated to any device, as it is used for collective designation to all devices in communication. The relationship between device address and ADR terminal voltage is shown in the table below.

Device Address	ADR1	ADR0
0000	GND	GND
0001	GND	V_{DD} x 1/3
0010	GND	V_{DD}
0011	GND	V_{DD} x 2/3
0100	V_{DD} x 1/3	GND
0101	V_{DD} x 1/3	V_{DD} x 1/3
0110	V_{DD} x 1/3	V_{DD}
0111	V_{DD} x 1/3	V_{DD} x 2/3
1000	V_{DD}	GND
1001	V_{DD}	V_{DD} x 1/3
1010	V_{DD}	V_{DD}
1011	V_{DD}	V_{DD} x 2/3
1100	V_{DD} x 2/3	GND
1101	V_{DD} x 2/3	V_{DD} x 1/3
1110	V_{DD} x 2/3	V_{DD}
1111 (reserved)	V_{DD} x 2/3	V_{DD} x 2/3

Selection of Division Mode

The matrix configuration for connected LEDs is set by inputting resistance partial pressure to devision mode setting terminal (DIV). The relationship between matrix configuration and DIV terminal voltage is shown in the table below.

Matrix configuration	DIV
24 x 1	GND
24 x2	V_{DD} x 1/3
24 x 4	V_{DD}
16 x 8	V_{DD} x 2/3

Selection of Division Mode (continued)

The function of output terminal varies according to matrix configuration. The relationship between matrix configuration and terminal function is shown in the table below.

Output terminal	Matrix Configuration			
	24 x 1	24 x 2	24 x 4	16 x 8
OUT0R	OUT0R			
OUT0G	OUT0G			
OUT0B	OUT0B			
OUT1R	OUT1R			
OUT1G	OUT1G			
OUT1B	OUT1B			
OUT2R	OUT2R			
OUT2G	OUT2G			
OUT2B	OUT2B			
OUT3R	OUT3R			
OUT3G	OUT3G			
OUT3B	OUT3B			
OUT4R	OUT4R			
OUT4G	OUT4G			
OUT4B	OUT4B			
OUT5R	OUT5R			
OUT5G	OUT5G			(Not used)
OUT5B	OUT5B			(Not used)
OUT6R	OUT6R			(Not used)
OUT6G	OUT6G			(Not used)
OUT6B	OUT6B			OUTS4
OUT7R	OUT7R			OUTS5
OUT7G	OUT7G			OUTS6
OUT7B	OUT7B			OUTS7
OUTS0	OUTS0			
OUTS1	(Not used)	OUTS1		
OUTS2	(Not used)	(Not used)	OUTS2	
OUTS3	(Not used)	(Not used)	OUTS3	

Selection of Communication mode

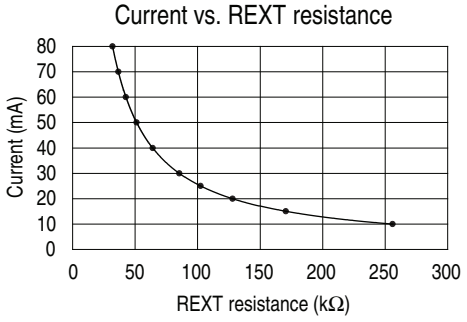
The communication mode is set by inputting resistance partial pressure to communication mode setting terminal (COM). The relationship between communication mode and COM terminal voltage is shown in the table below.

Communication mode	COM
Serial communication with address (SP-D8)	GND
Serial communication with address (SP-D7)	V_{DD} x 1/3
I²C-based serial communication (I²C)	V_{DD}
Serial communication with address (CE-D8)	V_{DD} x 2/3

Setting of Drive Current

Constant Current Drive

Current can be set individually for 3 groups (R/G/B). Current is set by connecting current setting resistance terminal (REXTR/REXTG/REXTB) to GND through external REXT resistance (See note 1). The relationship between current and REXT resistance is shown below.



Current (mA)	REXT resistance (kΩ)
10	256
15	171
20	128
25	102
30	85.3
40	64.0
50	51.2
60	42.7
70	36.6
80	32.0

Formula for Current Setting

I_{DOUT} (mA) = 2,560/REXT resistance (kΩ)

Recommended Operating Conditions

I_{DOUT}: 10 ~ 80 mA (momentary value).

Note: **1.** The current that is set is a momentary value. When LEDs are composed into a matrix, the effective value is calculated by dividing the original value by the matrix's division number. For example, when current is set at 60 mA in a 24x4 configuration, the effective value is 15 mA (= 60 mA/4).
2. The effective value is: I_{DOUT}/division number.

Constant Voltage Drive

Current can be set individually for output terminals in 24 systems (OUT0R ~ 7R,/ OUT0G ~ 7G/OUT0B ~ 7B). To set current individually, resistance is put in series relative to the LED to be lit. Current setting resistance terminal (REXTR/REXTG/REXTB) is connected to REXT resistance with which current becomes higher than the operating current. The relationship between current and series resistance/REXT resistance is shown below.

Formula for Current Setting

I_{DOUT} (mA) = Supply voltage (V) / (Series resistance (Ω) + On resistance 6.3 Ω) < 2,560 / REXT resistance (kΩ)

Reset

When the input to reset terminal ($\overline{RST}$) is L, all internal circuits are reset. Each buffer passes into the initial condition; the constant current output terminal and the open drain output terminal into open output; and CMOS output terminal into L output. When the input is changed from L to H, operation is resumed from the initial condition.

■ Communication Specifications

This IC can adapt to 4 communication modes. The communication mode is set with communication mode setting terminal (COM).

Serial Communication with Address (SP-D8 Mode)

Communication is started with a 9-bit start signal. Communication stability is enhanced by inserting a separator into data at intervals of 8 bits.

Serial Communication with Address (SP-D7 Mode)

Communication is started with an 8-bit start signal. Communication stability is enhanced by inserting a separator into data at intervals of 7 bits.

Serial Communication with Address (CE-D8 Mode)

The start and termination of communication is controlled with chip enabled signals. This communication mode is adapted to general-purpose serial parallel interface.

I²C Mode Communication (I²C Mode)

This communication mode conforms to general-purpose I²C communication protocol.

The name and communication format of each communication mode are shown below.

Name of communication mode	Abbreviation	Start Signal	Stop Signal	Separator	Data Width	Response
Serial communication with address (SP-D8 mode)	SP-D8	“1 1111 1111 0”	“1 1111 1111”	0: continuation 1: termination	8	ACK (NACK)
Serial communication with address (SP-D7 mode)	SP-D7	“1111 1111 0”	“1111 1111”	0: continuation 1: termination	7	ACK (NACK)
Serial communication with address (CE-D8 mode)	CE-D8	$\overline{CE}$ fall	$\overline{CE}$ rise	(None)	8	SYN
I²C-based serial communication (I²C mode)	I²C	I²C standard-based	I²C standard-based	I²C standard-based	8	ACK (NACK)

Start Signal: Communication is initialized, whether in wait or communication, into the device selection data wait condition.

Stop Signal: Communication is terminated, and passes into the start signal wait condition. In SP-D8/SP-D7, procedures to terminate communication (transmitting “1” to separator/transmitting a stop signal) can be omitted by transmitting a start signal after transmitting gradation data.

Separator: This bit is inserted into transmitted data. In SP-D8/SP-D7, communication is terminated by transmitting “1” to separator, and passes into the stop/start signal wait condition. In I²C, separator is allotted to ACK response.

Data Width: Data width refers to the bit width of transmitted data. In SP-D7, data that can be designated are restricted (no word length designation, designation of 128 gradations).

Response: Response refers to the type of response. This IC outputs data to SDO terminal at the fall of SCL signal. In SP-D8/SP-D7/I²C, received data are checked, and a result is returned (ACK or NACK). In CE-D8, a synchronization signal indicating in-communication status is output (SYN). Received data are not checked.

Chip Enable

This IC has chip enable terminal ($\overline{CE}$). If L is input as signal to the chip enable terminal, the chip becomes effective.

Serial Communication with Address (SP-D8, SP-D7), I²C-based Serial Communication

Communication data are received only when the chip is effective. If the chip becomes ineffective during communication, the IC interior passes into the wait condition, and received communication data are ignored.

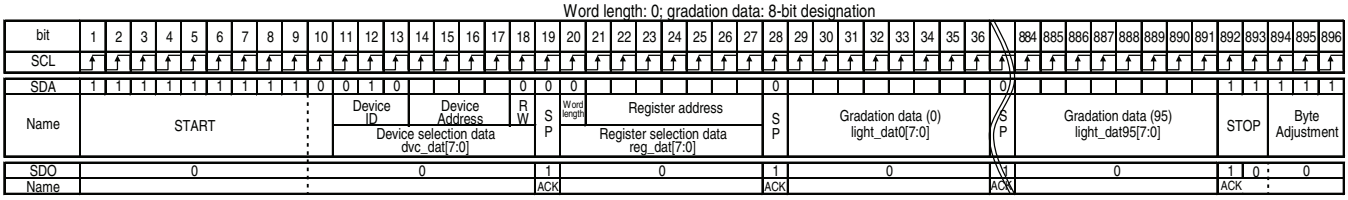
Serial Communication with Address (CE-D8)

The change of a chip enabled input signal means the start or termination of communication. If the chip passes from an effective condition (L input) into an ineffective condition (H input), judgment is made that the communication has terminated, and the IC interior returns to the initial condition.

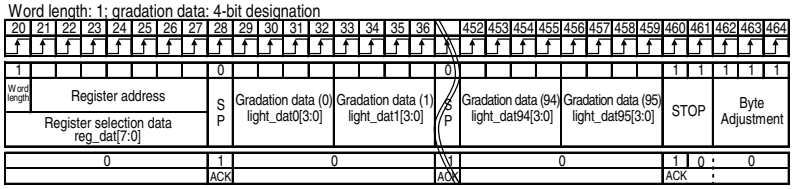
Communication Format

Serial Communication with Address (SP-D8 Mode)

Word length: 0; gradation data: 8-bit designation

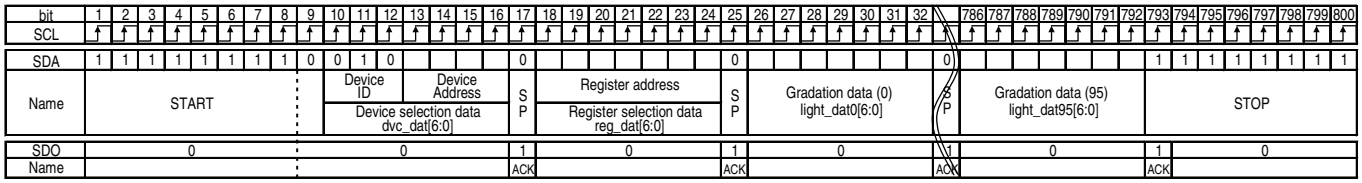


Word length: 1; gradation data: 4-bit designation



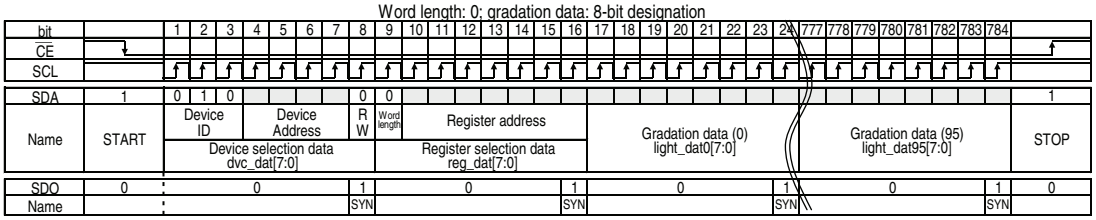
Byte adjustment: When transmitting data with 8 bits as unit, "1" is designated to remaining bits after STOP.

Serial Communication with Address (SP-D7 Mode)

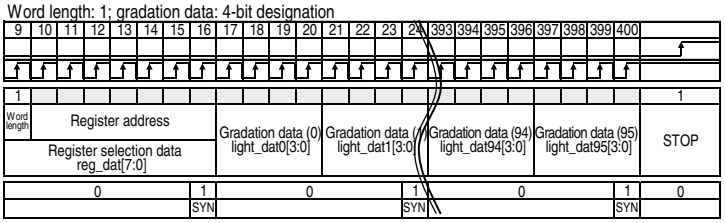


Serial Communication with Address (CE-D8 Mode)

Word length: 0; gradation data: 8-bit designation

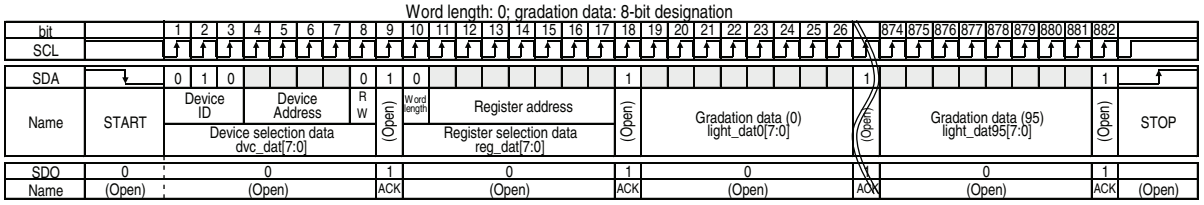


Word length: 1; gradation data: 4-bit designation

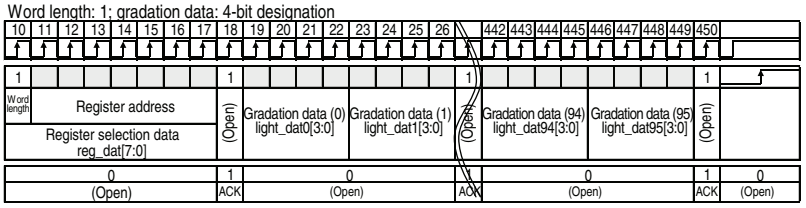


I²C-based Serial Communication (I²C Mode)

Word length: 0; gradation data: 8-bit designation



Word length: 1; gradation data: 4-bit designation



■ Command System

Device Designation

If the device ID and device address match IC settings, received data are retrieved. Device ID is fixed as “010”. The same command can be transmitted to all devices by designating “1111” as device address. The relationship between device address and device address terminal is shown in the table below.

Communication mode	Device selection data dvc_dat (7:0)							
	7	6	5	4	3	2	1	0
	Device ID			Device Address				RW
Standard	0	1	0	ADR1(1:0)		ADR0(1:0)		0
SP-D7								- - -

Register Designation

Communication mode	Register Selection data reg_dat (7:0)							
	7	6	5	4	3	2	1	0
Standard	Word Length	Register Address						
SP-D7	- - -							

Word length designation	Word length
0	8bit
1	4bit

Word Length

The data unit of gradation data is designated.

Register Address (Designation of lighting position)

The address of gradation register is designated. The upper limit of address that can be designated, and the number of gradation that can be transferred continuously, vary according to division mode setting and word length designation.

Register address (Special address)

All gradation registers can be designated collectively by designating 0x7F (127).
The power saving register can be designated by designating 0x78 (120)

Gradation Data

Communication mode	Gradation data light_dat(7:0)							
	7	6	5	4	3	2	1	0
Standard (8-bit)	Gradation Data							
Standard (4-bit)	Gradation Data N				Gradation Data N+1			
SP-D7	Gradation Data							- - -

Gradation Designation

Gradation data are designated using 8 bits (256 gradations), 7 bits (128 gradations), or 4 bits (16 gradations).

Power-saving Mode

When the power-saving data register is designated by register address-bits, the lowest 4 bits are treated as power-saving data.

Communication mode	Gradation data light_dat(7:0)							
	7	6	5	4	3	2	1	0
Standard	0	0	0	0	Power-saving data (current control)		Power-saving data (duty ratio control)	
SP-D7	- - -	0	0	0				

Power-saving Data	Output current or output duty ratio
00	100%
01	75%
10	50%
11	25%

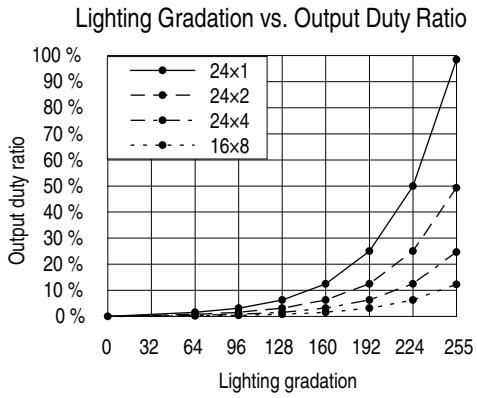
■ Gradation Control

Designation of Gradation

Gradation is designated using a data length of 8 bits (256 gradations), 7 bits (128 gradations), or 4 bits (16 gradations). The 8-bit or 4-bit mode can be selected using a word length bit in a communication command. In case of the 4-bit mode, the overall data length for communication can be shortened, though only a small number of gradations can be designated. In case of SP-D7 mode in serial communication with address, the word length is fixed at 7 bits, i.e., it is not designated.

Communication mode	Word length	Gradation number
Serial communication with address (SP-D8)	8-bit mode	256
	4-bit mode	16
Serial communication with address (SP-D7)	- - -	128
Serial communication with address (CE-D8)	8-bit mode	256
	4-bit mode	16
I^2C-based serial communication (I^2C)	8-bit mode	256
	4-bit mode	16

The relationship between lighting gradation and output duty ratio is shown below;



Lighting Gradation vs. Output Duty Ratio
(Representative Values Only)

Lighting gradation (8-bit)	Lighting gradation (7-bit)	Lighting gradation (4-bit)	Matrix configuration			
			24x1	24x2	24x4	16x8
0	0	0	(Light-out)	(Light-out)	(Light-out)	(Light-out)
15	7	- - -	0.37%	0.18%	0.09%	0.05%
31	15	1	0.76%	0.38%	0.19%	0.09%
47	23	2	1.15%	0.57%	0.29%	0.14%
63	31	3	1.54%	0.77%	0.38%	0.19%
79	39	4	2.29%	1.15%	0.57%	0.29%
95	47	5	3.08%	1.54%	0.77%	0.38%
111	55	6	4.59%	2.29%	1.15%	0.57%
127	63	7	6.15%	3.08%	1.54%	0.77&
143	71	8	9.18%	4.59%	2.29%	1.15%
159	79	9	12.30%	6.15%	3.08%	1.54%
175	87	10	18.36%	9.18%	4.59%	2.29%
191	95	11	24.61%	12.30%	6.15%	3.08%
207	103	12	36.72%	18.36%	9.18%	4.59%
223	111	13	49.22%	24.61%	12.30%	6.15%
239	119	14	73.44%	36.72%	18.36%	9.18%
255	127	15	98.44%	49.22%	24.61%	12.30%

Lighting Gradation vs. Output Duty Ratio (All Gradations)

Gradation (8-bit)	Gradation (7-bit)	Gradation (4-bit)	Matrix configuration			
			24x1	24x2	24x4	16x8
0	0	0	(Light-out)	(Light-out)	(Light-out)	(Light-out)
1	- - -	- - -	0.02	0.01	0.01	0.00
2	- - -	- - -	0.05	0.02	0.01	0.01
3	1	- - -	0.07	0.04	0.02	0.01
4	- - -	- - -	0.10	0.05	0.02	0.01
5	2	- - -	0.12	0.06	0.03	0.02
6	- - -	- - -	0.15	0.07	0.04	0.02
7	3	- - -	0.17	0.09	0.04	0.02
8	- - -	- - -	0.20	0.10	0.05	0.02
9	4	- - -	0.22	0.11	0.05	0.03
10	- - -	- - -	0.24	0.12	0.06	0.03
11	5	- - -	0.27	0.13	0.07	0.03
12	- - -	- - -	0.29	0.15	0.07	0.04
13	6	- - -	0.32	0.16	0.08	0.04
14	- - -	- - -	0.34	0.17	0.09	0.04
15	**7**	**- - -**	**0.37**	**0.18**	**0.09**	**0.05**
16	- - -	- - -	0.39	0.20	0.10	0.05
17	8	- - -	0.42	0.21	0.10	0.05
18	- - -	- - -	0.44	0.22	0.11	0.05
19	9	- - -	0.46	0.23	0.12	0.06
20	- - -	- - -	0.49	0.24	0.12	0.06
21	10	- - -	0.51	0.26	0.13	0.06
22	- - -	- - -	0.54	0.27	0.13	0.07
23	11	- - -	0.56	0.28	0.14	0.07
24	- - -	- - -	0.59	0.29	0.15	0.07
25	12	- - -	0.61	0.31	0.15	0.08
26	- - -	- - -	0.63	0.32	0.16	0.08
27	13	- - -	0.66	0.33	0.16	0.08
28	- - -	- - -	0.68	0.34	0.17	0.09
29	14	- - -	0.71	0.35	0.18	0.09
30	- - -	- - -	0.73	0.37	0.18	0.09
31	**15**	**1**	**0.76**	**0.38**	**0.19**	**0.09**
32	- - -	- - -	0.78	0.39	0.20	0.10
33	16	- - -	0.81	0.40	0.20	0.10
34	- - -	- - -	0.83	0.42	0.21	0.10
35	17	- - -	0.85	0.43	0.21	0.11
36	- - -	- - -	0.88	0.44	0.22	0.11
37	18	- - -	0.90	0.45	0.23	0.11
38	- - -	- - -	0.93	0.46	0.23	0.12
39	19	- - -	0.95	0.48	0.24	0.12
40	- - -	- - -	0.98	0.49	0.24	0.12
41	20	- - -	1.00	0.50	0.25	0.13
42	- - -	- - -	1.03	0.51	0.26	0.13
43	21	- - -	1.05	0.52	0.26	0.13
44	- - -	- - -	1.07	0.54	0.27	0.13
45	22	- - -	1.10	0.55	0.27	0.14
46	- - -	- - -	1.12	0.56	0.28	0.14
47	**23**	**2**	**1.15**	**0.57**	**0.29**	**0.14**
48	- - -	- - -	1.17	0.59	0.29	0.15
49	24	- - -	1.20	0.60	0.30	0.15
50	- - -	- - -	1.22	0.61	0.31	0.15
51	25	- - -	1.25	0.62	0.31	0.16
52	- - -	- - -	1.27	0.63	0.32	0.16
53	26	- - -	1.29	0.65	0.32	0.16
54	- - -	- - -	1.32	0.66	0.33	0.16
55	27	- - -	1.34	0.67	0.34	0.17
56	- - -	- - -	1.37	0.68	0.34	0.17
57	28	- - -	1.39	0.70	0.35	0.17
58	- - -	- - -	1.42	0.71	0.35	0.18
59	29	- - -	1.44	0.72	0.36	0.18
60	- - -	- - -	1.46	0.73	0.37	0.18
61	30	- - -	1.49	0.74	0.37	0.19
62	- - -	- - -	1.51	0.76	0.38	0.19
63	**31**	**3**	**1.54**	**0.77**	**0.38**	**0.19**

Gradation (8-bit)	Gradation (7-bit)	Gradation (4-bit)	Matrix configuration			
			24x1	24x2	24x4	16x8
64	- - -	- - -	1.56	0.78	0.39	0.20
65	32	- - -	1.61	0.81	0.40	0.20
66	- - -	- - -	1.66	0.83	0.42	0.21
67	33	- - -	1.71	0.85	0.43	0.21
68	- - -	- - -	1.76	0.88	0.44	0.22
69	34	- - -	1.81	0.90	0.45	0.23
70	- - -	- - -	1.86	0.93	0.46	0.23
71	35	- - -	1.90	0.95	0.48	0.24
72	- - -	- - -	1.95	0.98	0.49	0.24
73	36	- - -	2.00	1.00	0.50	0.25
74	- - -	- - -	2.05	1.03	0.51	0.26
75	37	- - -	2.10	1.05	0.52	0.26
76	- - -	- - -	2.15	1.07	0.54	0.27
77	38	- - -	2.20	1.10	0.55	0.27
78	- - -	- - -	2.25	1.12	0.56	0.28
79	**39**	**4**	**2.29**	**1.15**	**0.57**	**0.29**
80	- - -	- - -	2.34	1.17	0.59	0.29
81	40	- - -	2.39	1.20	0.60	0.30
82	- - -	- - -	2.44	1.22	0.61	0.31
83	41	- - -	2.49	1.25	0.62	0.31
84	- - -	- - -	2.54	1.27	0.63	0.32
85	42	- - -	2.59	1.29	0.65	0.32
86	- - -	- - -	2.64	1.32	0.66	0.33
87	43	- - -	2.69	1.34	0.67	0.34
88	- - -	- - -	2.73	1.37	0.68	0.34
89	44	- - -	2.78	1.39	0.70	0.35
90	- - -	- - -	2.83	1.42	0.71	0.35
91	45	- - -	2.88	1.44	0.72	0.36
92	- - -	- - -	2.93	1.46	0.73	0.37
93	46	- - -	2.98	1.49	0.74	0.37
94	- - -	- - -	3.03	1.51	0.76	0.38
95	**47**	**5**	**3.08**	**1.54**	**0.77**	**0.38**
96	- - -	- - -	3.13	1.56	0.78	0.39
97	48	- - -	3.22	1.61	0.81	0.40
98	- - -	- - -	3.32	1.66	0.83	0.42
99	49	- - -	3.42	1.71	0.85	0.43
100	- - -	- - -	3.52	1.76	0.88	0.44
101	50	- - -	3.61	1.81	0.90	0.45
102	- - -	- - -	3.71	1.86	0.93	0.46
103	51	- - -	3.81	1.90	0.95	0.48
104	- - -	- - -	3.91	1.95	0.98	0.49
105	52	- - -	4.00	2.00	1.00	0.50
106	- - -	- - -	4.10	2.05	1.03	0.51
107	53	- - -	4.20	2.10	1.05	0.52
108	- - -	- - -	4.30	2.15	1.07	0.54
109	54	- - -	4.39	2.20	1.10	0.55
110	- - -	- - -	4.49	2.25	1.12	0.56
111	**55**	**6**	**4.59**	**2.29**	**1.15**	**0.57**
112	- - -	- - -	4.69	2.34	1.17	0.59
113	56	- - -	4.79	2.39	1.20	0.60
114	- - -	- - -	4.88	2.44	1.22	0.61
115	57	- - -	4.98	2.49	1.25	0.62
116	- - -	- - -	5.08	2.54	1.27	0.63
117	58	- - -	5.18	2.59	1.29	0.65
118	- - -	- - -	5.27	2.64	1.32	0.66
119	59	- - -	5.37	2.69	1.34	0.67
120	- - -	- - -	5.47	2.73	1.37	0.68
121	60	- - -	5.57	2.78	1.39	0.70
122	- - -	- - -	5.66	2.83	1.42	0.71
123	61	- - -	5.76	2.88	1.44	0.72
124	- - -	- - -	5.86	2.93	1.46	0.73
125	62	- - -	5.96	2.98	1.49	0.74
126	- - -	- - -	6.05	3.03	1.51	0.76
127	**63**	**7**	**6.15**	**3.08**	**1.54**	**0.77**

Lighting Gradation vs. Output Duty Ratio (All Gradations - continued)

Gradation (8-bit)	Gradation (7-bit)	Gradation (4-bit)	Matrix configuration			
			24x1	24x2	24x4	16x8
128	- - -	- - -	6.25	3.13	1.56	0.78
129	64	- - -	6.45	3.22	1.61	0.81
130	- - -	- - -	6.64	3.32	1.66	0.83
131	65	- - -	6.84	3.42	1.71	0.85
132	- - -	- - -	7.03	3.52	1.76	0.88
133	66	- - -	7.23	3.61	1.81	0.90
134	- - -	- - -	7.42	3.71	1.86	0.93
135	67	- - -	7.62	3.81	1.90	0.95
136	- - -	- - -	7.81	3.91	1.95	0.98
137	68	- - -	8.01	4.00	2.00	1.00
138	- - -	- - -	8.20	4.10	2.05	1.03
139	69	- - -	8.40	4.20	2.10	1.05
140	- - -	- - -	8.59	4.30	2.15	1.07
141	70	- - -	8.79	4.39	2.20	1.10
142	- - -	- - -	8.98	4.49	2.25	1.12
143	**71**	**8**	**9.18**	**4.59**	**2.29**	**1.15**
144	- - -	- - -	9.38	4.69	2.34	1.17
145	72	- - -	9.57	4.79	2.39	1.20
146	- - -	- - -	9.77	4.88	2.44	1.22
147	73	- - -	9.96	4.98	2.49	1.25
148	- - -	- - -	10.16	5.08	2.54	1.27
149	74	- - -	10.35	5.18	2.59	1.29
150	- - -	- - -	10.55	5.27	2.64	1.32
151	75	- - -	10.74	5.37	2.69	1.34
152	- - -	- - -	10.94	5.47	2.73	1.37
153	76	- - -	11.13	5.57	2.78	1.39
154	- - -	- - -	11.33	5.66	2.83	1.42
155	77	- - -	11.52	5.76	2.88	1.44
156	- - -	- - -	11.72	5.86	2.93	1.46
157	78	- - -	11.91	5.96	2.98	1.49
158	- - -	- - -	12.11	6.05	3.03	1.51
159	**79**	**9**	**12.30**	**6.15**	**3.08**	**1.54**
160	- - -	- - -	12.50	6.25	3.13	1.56
161	80	- - -	12.89	6.45	3.22	1.61
162	- - -	- - -	13.28	6.64	3.32	1.66
163	81	- - -	13.67	6.84	3.42	1.71
164	- - -	- - -	14.06	7.03	3.52	1.76
165	82	- - -	14.45	7.23	3.61	1.81
166	- - -	- - -	14.84	7.42	3.71	1.86
167	83	- - -	15.23	7.62	3.81	1.90
168	- - -	- - -	15.63	7.81	3.91	1.95
169	84	- - -	16.02	8.01	4.00	2.00
170	- - -	- - -	16.41	8.20	4.10	2.05
171	85	- - -	16.80	8.40	4.20	2.10
172	- - -	- - -	17.19	8.59	4.30	2.15
173	86	- - -	17.58	8.79	4.39	2.20
174	- - -	- - -	17.97	8.98	4.49	2.25
175	**87**	**10**	**18.36**	**9.18**	**4.59**	**2.29**
176	- - -	- - -	18.75	9.38	4.69	2.34
177	88	- - -	19.14	9.57	4.79	2.39
178	- - -	- - -	19.53	9.77	4.88	2.44
179	89	- - -	19.92	9.96	4.98	2.49
180	- - -	- - -	20.31	10.16	5.08	2.54
181	90	- - -	20.70	10.35	5.18	2.59
182	- - -	- - -	21.09	10.55	5.27	2.64
183	91	- - -	21.48	10.74	5.37	2.69
184	- - -	- - -	21.88	10.94	5.47	2.73
185	92	- - -	22.27	11.13	5.57	2.78
186	- - -	- - -	22.66	11.33	5.66	2.83
187	93	- - -	23.05	11.52	5.76	2.88
188	- - -	- - -	23.44	11.72	5.86	2.93
189	94	- - -	23.83	11.91	5.96	2.98
190	- - -	- - -	24.22	12.11	6.05	3.03
191	**95**	**11**	**24.61**	**12.30**	**6.15**	**3.08**

Gradation (8-bit)	Gradation (7-bit)	Gradation (4-bit)	Matrix configuration			
			24x1	24x2	24x4	16x8
192	- - -	- - -	25.00	12.50	6.25	3.13
193	96	- - -	25.78	12.89	6.45	3.22
194	- - -	- - -	26.56	13.28	6.64	3.32
195	97	- - -	27.34	13.67	6.84	3.42
196	- - -	- - -	28.13	14.06	7.03	3.52
197	98	- - -	28.91	14.45	7.23	3.61
198	- - -	- - -	29.69	14.84	7.42	3.71
199	99	- - -	30.47	15.23	7.62	3.81
200	- - -	- - -	31.25	15.63	7.81	3.91
201	100	- - -	32.03	16.02	8.01	4.00
202	- - -	- - -	32.81	16.41	8.20	4.10
203	101	- - -	33.59	16.80	8.40	4.20
204	- - -	- - -	34.38	17.19	8.59	4.30
205	102	- - -	35.16	17.58	8.79	4.39
206	- - -	- - -	35.94	17.97	8.98	4.49
207	**103**	**12**	**36.72**	**18.36**	**9.18**	**4.59**
208	- - -	- - -	37.50	18.75	9.38	4.69
209	104	- - -	38.28	19.14	9.57	4.79
210	- - -	- - -	39.06	19.53	9.77	4.88
211	105	- - -	39.84	19.92	9.96	4.98
212	- - -	- - -	40.63	20.31	10.16	5.08
213	106	- - -	41.41	20.70	10.35	5.18
214	- - -	- - -	42.19	21.09	10.55	5.27
215	107	- - -	42.97	21.48	10.74	5.37
216	- - -	- - -	43.75	21.88	10.94	5.47
217	108	- - -	44.53	22.27	11.13	5.57
218	- - -	- - -	45.31	22.66	11.33	5.66
219	109	- - -	46.09	23.05	11.52	5.76
220	- - -	- - -	46.88	23.44	11.72	5.86
221	110	- - -	47.66	23.83	11.91	5.96
222	- - -	- - -	48.44	24.22	12.11	6.05
223	**111**	**13**	**49.22**	**24.61**	**12.30**	**6.15**
224	- - -	- - -	50.00	25.00	12.50	6.25
225	112	- - -	51.56	25.78	12.89	6.45
226	- - -	- - -	53.13	26.56	13.28	6.64
227	113	- - -	54.69	27.34	13.67	6.84
228	- - -	- - -	56.25	28.13	14.06	7.03
229	114	- - -	57.81	28.91	14.45	7.23
230	- - -	- - -	59.38	29.69	14.84	7.42
231	115	- - -	60.94	30.47	15.23	7.62
232	- - -	- - -	62.50	31.25	15.63	7.81
233	116	- - -	64.06	32.03	16.02	8.01
234	- - -	- - -	65.63	32.81	16.41	8.20
235	117	- - -	67.19	33.59	16.80	8.40
236	- - -	- - -	68.75	34.38	17.19	8.59
237	118	- - -	70.31	35.16	17.58	8.79
238	- - -	- - -	71.88	35.94	17.97	8.98
239	**119**	**14**	**73.44**	**36.72**	**18.36**	**9.18**
240	- - -	- - -	75.00	37.50	18.75	9.38
241	120	- - -	76.56	38.28	19.14	9.57
242	- - -	- - -	78.13	39.06	19.53	9.77
243	121	- - -	79.69	39.84	19.92	9.96
244	- - -	- - -	81.25	40.63	20.31	10.16
245	122	- - -	82.81	41.41	20.70	10.35
246	- - -	- - -	84.38	42.19	21.09	10.55
247	123	- - -	85.94	42.97	21.48	10.74
248	- - -	- - -	87.50	43.75	21.88	10.94
249	124	- - -	89.06	44.53	22.27	11.13
250	- - -	- - -	90.63	45.31	22.66	11.33
251	125	- - -	92.19	46.09	23.05	11.52
252	- - -	- - -	93.75	46.88	23.44	11.72
253	126	- - -	95.31	47.66	23.83	11.91
254	- - -	- - -	96.88	48.44	24.22	12.11
255	**127**	**15**	**98.44**	**49.22**	**24.61**	**12.30**

Designation of Lighting Position

The lighting position is designated with a register address in a communication command. The relationship between register address and lighting position in each matrix configuration is shown in the table below.

Register Address	Matrix Configuration				
	24x1	24x2	24x4	16x8	
				Even-number row	Odd-number row
0x00 (0)	(0, 0)	(0, 0)	(0, 0)	(0, 0)	(1, 0)
0x01 (1)	(1 ,0)	(1, 0)	(1, 0)	(2, 0)	(3, 0)
0x02 (2)	(2, 0)	(2, 0)	(2, 0)	(4, 0)	(5, 0)
0x03 (3)	(3, 0)	(3, 0)	(3, 0)	(6, 0)	(7, 0)
0x04 (4)	(4, 0)	(4, 0)	(4, 0)	(8, 0)	(9, 0)
0x05 (5)	(5, 0)	(5, 0)	(5, 0)	(10, 0)	(11, 0)
0x06 (6)	(6, 0)	(6, 0)	(6, 0)	(12, 0)	(13, 0)
0x07 (7)	(7, 0)	(7, 0)	(7, 0)	(14, 0)	(15, 0)
0x08 (8)	(8, 0)	(8, 0)	(8, 0)	(0, 1)	(1, 1)
0x09 (9)	(9, 0)	(9, 0)	(9, 0)	(2, 1)	(3, 1)
0x0A (10)	(10, 0)	(10, 0)	(10, 0)	(4, 1)	(5, 1)
0x0B (11)	(11, 0)	(11, 0)	(11, 0)	(6, 1)	(7, 1)
0x0C (12)	(12, 0)	(12, 0)	(12, 0)	(8, 1)	(9, 1)
0x0D (13)	(13, 0)	(13, 0)	(13, 0)	(10, 1)	(11, 1)
0x0E (14)	(14, 0)	(14, 0)	(14, 0)	(12, 1)	(13, 1)
0x0F (15)	(15, 0)	(15, 0)	(15, 0)	(14, 1)	(15, 1)
0x10 (16)	(16, 0)	(16, 0)	(16, 0)	(0, 2)	(1, 2)
0x11 (17)	(17, 0)	(17, 0)	(17, 0)	(2, 2)	(3, 2)
0x12 (18)	(18, 0)	(18, 0)	(18, 0)	(4, 2)	(5, 2)
0x13 (19)	(19, 0)	(19, 0)	(19, 0)	(6, 2)	(7, 2)
0x14 (20)	(20, 0)	(20, 0)	(20, 0)	(8, 2)	(9, 2)
0x15 (21)	(21, 0)	(21, 0)	(21, 0)	(10, 2)	(11, 2)
0x16 (22)	(22, 0)	(22, 0)	(22, 0)	(12, 2)	(13, 2)
0x17 (23)	(23, 0)	(23, 0)	(23, 0)	(14, 2)	(15, 2)
0x18 (24)	- - -	(0, 1)	(0, 1)	(0, 3)	(1, 3)
0x19 (25)	- - -	(1, 1)	(1, 1)	(2, 3)	(3, 3)
0x1A (26)	- - -	(2, 1)	(2, 1)	(4, 3)	(5, 3)
0x1B (27)	- - -	(3, 1)	(3, 1)	(6, 3)	(7, 3)
0x1C (28)	- - -	(4, 1)	(4, 1)	(8, 3)	(9, 3)
0x1D (29)	- - -	(5, 1)	(5, 1)	(10, 3)	(11, 3)
0x1E (30)	- - -	(6, 1)	(6, 1)	(12, 3)	(13, 3)
0x1F (31)	- - -	(7, 1)	(7, 1)	(14, 3)	(15, 3)
0x20 (32)	- - -	(8, 1)	(8, 1)	(0, 4)	(1, 4)
0x21 (33)	- - -	(9, 1)	(9, 1)	(2, 4)	(3, 4)
0x22 (34)	- - -	(10, 1)	(10, 1)	(4, 4)	(5, 4)
0x23 (35)	- - -	(11, 1)	(11, 1)	(6, 4)	(7, 4)
0x24 (36)	- - -	(12, 1)	(12, 1)	(8, 4)	(9, 4)
0x25 (37)	- - -	(13, 1)	(13, 1)	(10, 4)	(11, 4)
0x26 (38)	- - -	(14, 1)	(14, 1)	(12, 4)	(13, 4)
0x27 (39)	- - -	(15, 1)	(15, 1)	(14, 4)	(15, 4)
0x28 (40)	- - -	(16, 1)	(16, 1)	(0, 5)	(1, 5)
0x29 (41)	- - -	(17, 1)	(17, 1)	(2, 5)	(3, 5)
0x2A (42)	- - -	(18, 1)	(18, 1)	(4, 5)	(5, 5)
0x2B (43)	- - -	(19, 1)	(19, 1)	(6, 5)	(7, 5)
0x2C (44)	- - -	(20, 1)	(20, 1)	(8, 5)	(9, 5)
0x2D (45)	- - -	(21, 1)	(21, 1)	(10, 5)	(11, 5)
0x2E (46)	- - -	(22, 1)	(22, 1)	(12, 5)	(13, 5)
0x2F (47)	- - -	(23, 1)	(23, 1)	(14, 5)	(15, 5)

Register Address	Matrix Configuration				
	24x1	24x2	24x4	16x8	
				Even-number row	Odd-number row
0x30 (48)	- - -	- - -	(0, 2)	(0, 6)	(1, 6)
0x31 (49)	- - -	- - -	(1, 2)	(2, 6)	(3, 6)
0x32 (50)	- - -	- - -	(2, 2)	(4, 6)	(5, 6)
0x33 (51)	- - -	- - -	(3, 2)	(6, 6)	(7, 6)
0x34 (52)	- - -	- - -	(4, 2)	(8, 6)	(9, 6)
0x35 (53)	- - -	- - -	(5, 2)	(10, 6)	(11, 6)
0x36 (54)	- - -	- - -	(6, 2)	(12, 6)	(13, 6)
0x37 (55)	- - -	- - -	(7, 2)	(14, 6)	(15, 6)
0x38 (56)	- - -	- - -	(8, 2)	(0, 7)	(1, 7)
0x39 (57)	- - -	- - -	(9, 2)	(2, 7)	(3, 7)
0x3A (58)	- - -	- - -	(10, 2)	(4, 7)	(5, 7)
0x3B (59)	- - -	- - -	(11, 2)	(6, 7)	(7, 7)
0x3C (60)	- - -	- - -	(12, 2)	(8, 7)	(9, 7)
0x3D (61)	- - -	- - -	(13, 2)	(10, 7)	(11, 7)
0x3E (62)	- - -	- - -	(14, 2)	(12, 7)	(13, 7)
0x3F (63)	- - -	- - -	(15, 2)	(14, 7)	(15, 7)
0x40 (64)	- - -	- - -	(16, 2)	- - -	- - -
0x41 (65)	- - -	- - -	(17, 2)	- - -	- - -
0x42 (66)	- - -	- - -	(18, 2)	- - -	- - -
0x43 (67)	- - -	- - -	(19, 2)	- - -	- - -
0x44 (68)	- - -	- - -	(20, 2)	- - -	- - -
0x45 (69)	- - -	- - -	(21, 2)	- - -	- - -
0x46 (70)	- - -	- - -	(22, 2)	- - -	- - -
0x47 (71)	- - -	- - -	(23, 2)	- - -	- - -
0x48 (72)	- - -	- - -	(0, 3)	- - -	- - -
0x49 (73)	- - -	- - -	(1, 3)	- - -	- - -
0x4A (74)	- - -	- - -	(2, 3)	- - -	- - -
0x4B (75)	- - -	- - -	(3, 3)	- - -	- - -
0x4C (76)	- - -	- - -	(4, 3)	- - -	- - -
0x4D (77)	- - -	- - -	(5, 3)	- - -	- - -
0x4E (78)	- - -	- - -	(6, 3)	- - -	- - -
0x4F (79)	- - -	- - -	(7, 3)	- - -	- - -
0x50 (80)	- - -	- - -	(8, 3)	- - -	- - -
0x51 (81)	- - -	- - -	(9, 3)	- - -	- - -
0x52 (82)	- - -	- - -	(10, 3)	- - -	- - -
0x53 (83)	- - -	- - -	(11, 3)	- - -	- - -
0x54 (84)	- - -	- - -	(12, 3)	- - -	- - -
0x55 (85)	- - -	- - -	(13, 3)	- - -	- - -
0x56 (86)	- - -	- - -	(14, 3)	- - -	- - -
0x57 (87)	- - -	- - -	(15, 3)	- - -	- - -
0x58 (88)	- - -	- - -	(16, 3)	- - -	- - -
0x59 (89)	- - -	- - -	(17, 3)	- - -	- - -
0x5A (90)	- - -	- - -	(18, 3)	- - -	- - -
0x5B (91)	- - -	- - -	(19, 3)	- - -	- - -
0x5C (92)	- - -	- - -	(20, 3)	- - -	- - -
0x5D (93)	- - -	- - -	(21, 3)	- - -	- - -
0x5E (94)	- - -	- - -	(22, 3)	- - -	- - -
0x5F (95)	- - -	- - -	(23, 3)	- - -	- - -

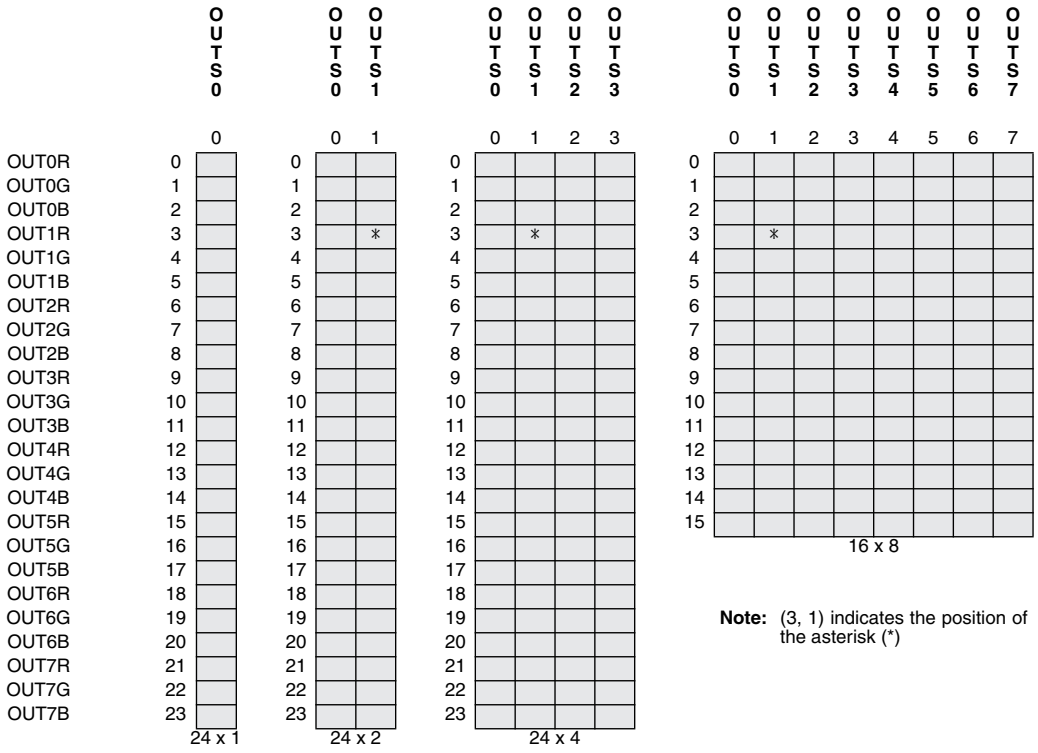
Gradation data can be transmitted continuously (continuous transfer). In this case, gradation data are stored sequentially, with the register address designated at first at the top. Gradation data cannot be transmitted to a register address that is not found in matrix configurations (wrong address). Communication is terminated if a wrong address is designated, or if a wrong address is reached in continuous transfer of gradation data.

Note: When a 16x8-mode matrix configuration is used, an LED shown in an odd-number row in the table above cannot be designated as the first address. Gradation data can be transmitted only via continuous transfer to a register address in an odd-number row.

■ Matrix Configuration

An LED Matrix configuration can be chosen from among 24x1, 24x2, 24x4 and 16x8 configurations, using division mode setting terminal DIV.

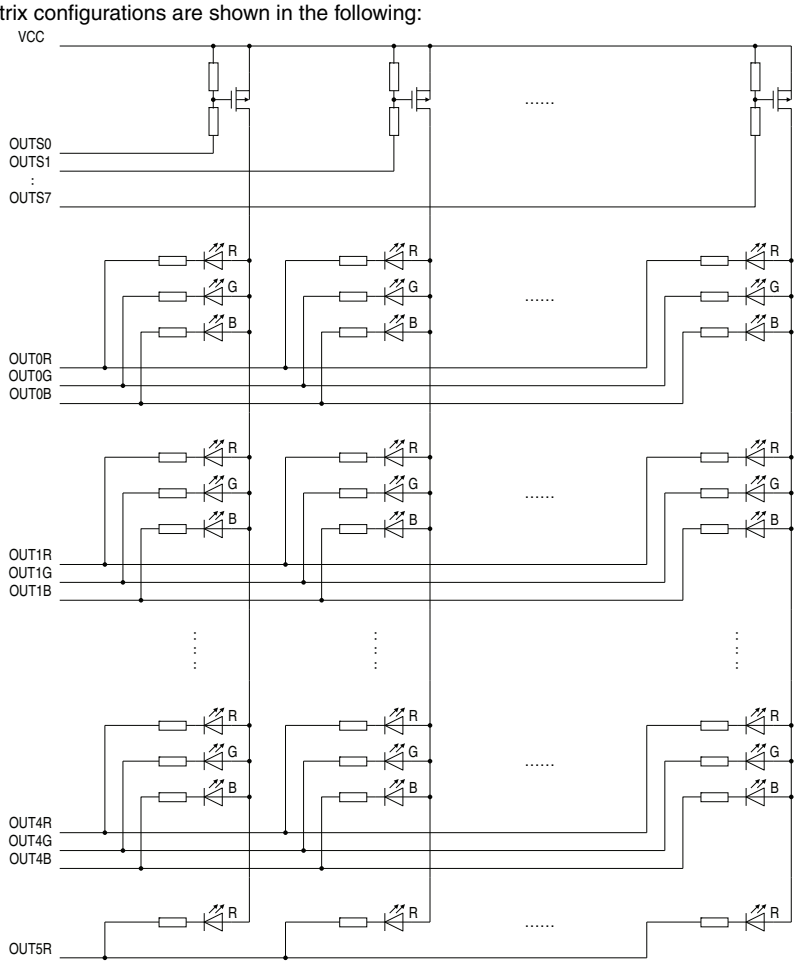
Indication of Lighting Position



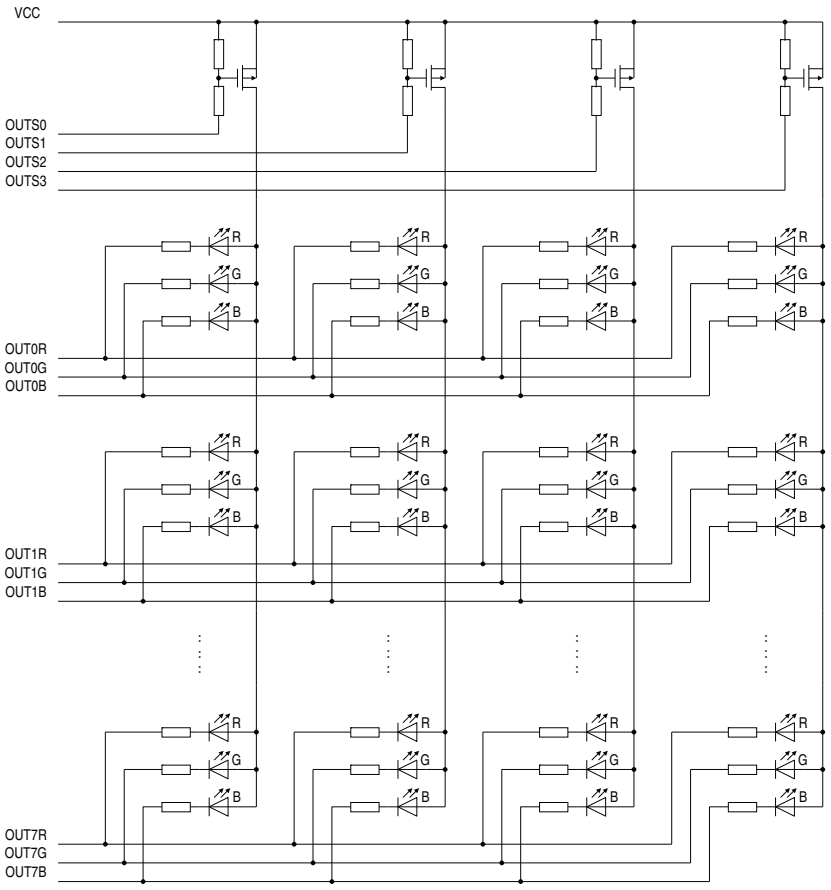
Note: (3, 1) indicates the position of the asterisk (*)

Examples of circuits in different matrix configurations are shown in the following:

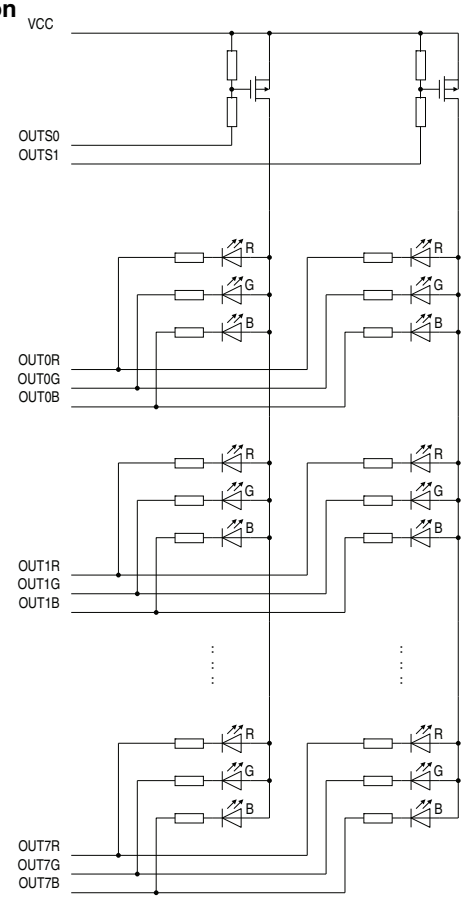
16 x 8 Configuration



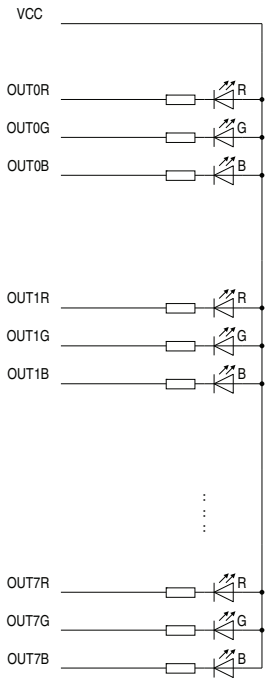
24 x 4 Configuration



24 x 2 Configuration



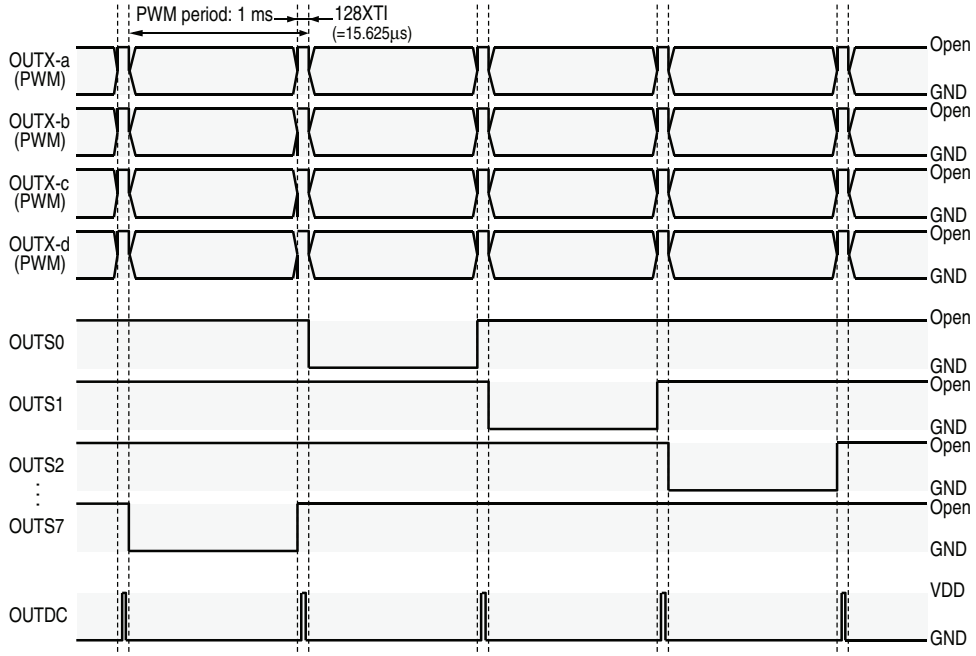
24 x 1 Configuration



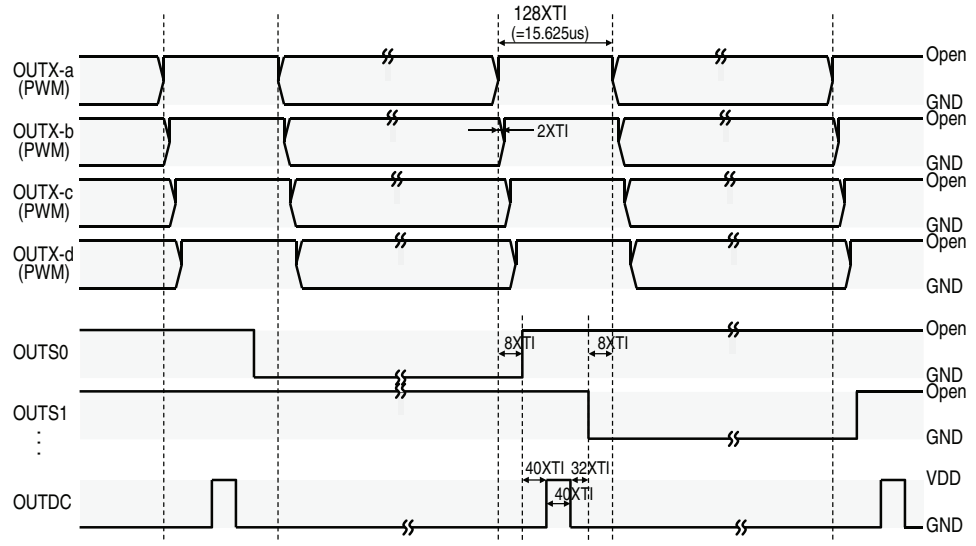
■ Control Waveform

The matrix is controlled by switching between ON and OFF of drive output terminals (OUT0R - 7B) and switch output terminals (OUTS0 - 7).

Control Waveform (Overall)



Control Waveform (at Switching)



Note: XTI = 8.192 MHz = 122.07 ns. The indication of duration in these figures is for 16x8 configuration. The duration is twice the indicated value for 24x4 configuration; 4 times for 24x2 configuration; and 8 times for 24x1 configuration.

Drive Output Group

Adjoining drive output terminals (OUT0R - 7B) have different change timings. This difference is designed to reduce noise caused by the simultaneous change of drive output. There are 4 change timings, by which drive outputs are grouped as follows:

Drive output terminal	Drive output group			
	OUTX-a	OUTX-b	OUTX-c	OUTX-d
OUT0R	○			
OUT0G		○		
OUT0B			○	
OUT1R				○
OUT1G	○			
OUT1B		○		
OUT2R			○	
OUT2G				○
OUT2B	○			
OUT3R		○		
OUT3G			○	
OUT3B				○
OUT4R	○			
OUT4G		○		
OUT4B			○	
OUT5R				○
OUT5G	○(*)			
OUT5B		○(*)		
OUT6R			○(*)	
OUT6G				○(*)
OUT6B	○(*)			
OUT7R		○(*)		
OUT7G			○(*)	
OUT7B				○(*)

Note: *This does not apply when the division mode is set as 16x8 configuration, in which case the following operations are executed:
OUT5G - 6G: Not used.
OUT6B - OUT7B: Functions as OUTS4 - 7

Synchronous Control Output

Synchronous control output terminal (OUTDC) outputs control signals synchronized with lighting switch. These signals are used to drive external circuits at lighting switch.

■ Power-saving Control

Power saving data is set, via communications as 100%, 75%, 50% or 25%. Current or duty ratio control is used as control method. Power saving data can be set separately via either of these methods.

Current Control

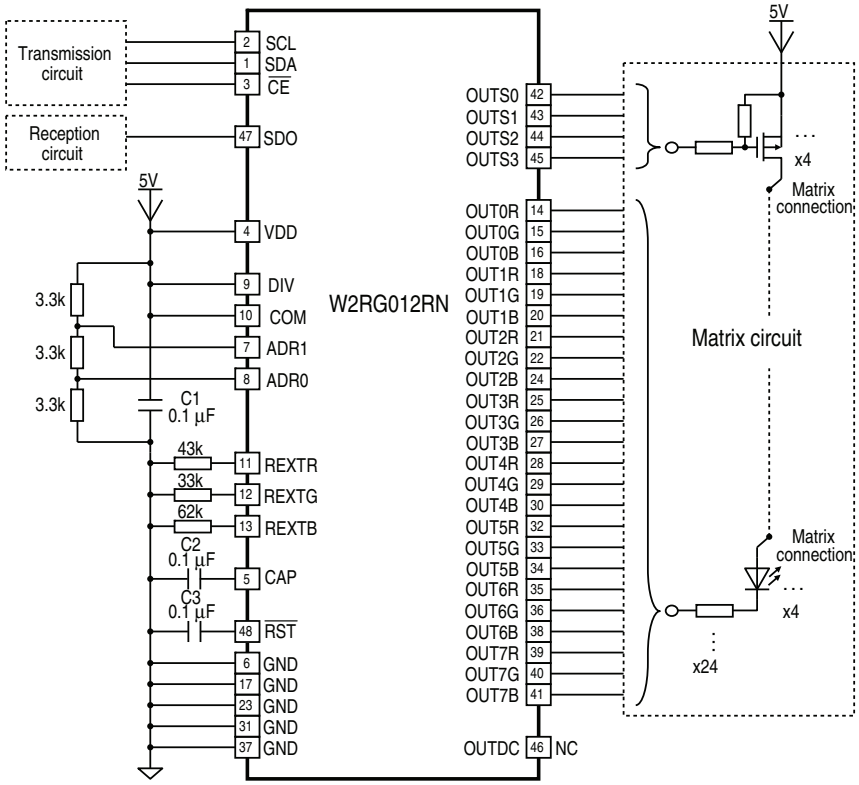
Output currents are changed collectively according to a designated ratio to a current set with current setting terminal REXTR/REXTG/REXTB.

Note: The hue of a full-color LED in normal operation may be different from that in power-saving operation, due to differences in current characteristics among R/G/B.

Duty Ratio Control

Output duty ratios are changed collectively according to a designated ratio to a duty ratio designated to a particular gradation.

■ Application Example

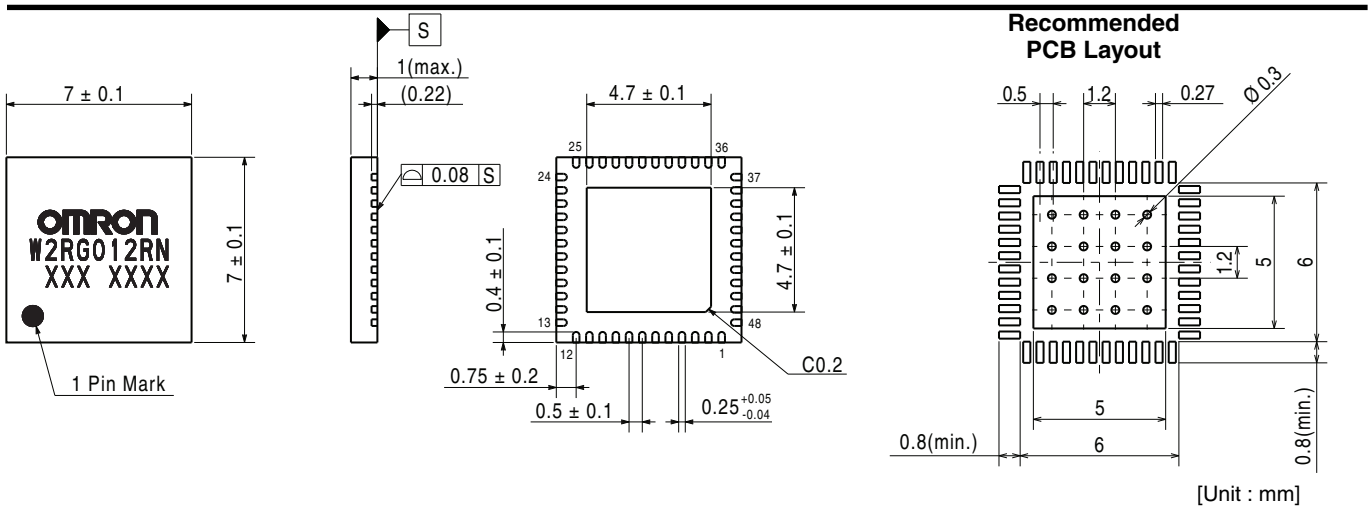


Setting Example

DIV:		24x4 configuration
COM:		I²C communication
ADR:		device address “1101”
Constant current setting	R:	59.5 mA (14.9 mA)
	G:	77.6 mA (19.4 mA)
	B:	41.3 mA (10.3 mA)

Note: Effective values are shown in parentheses.

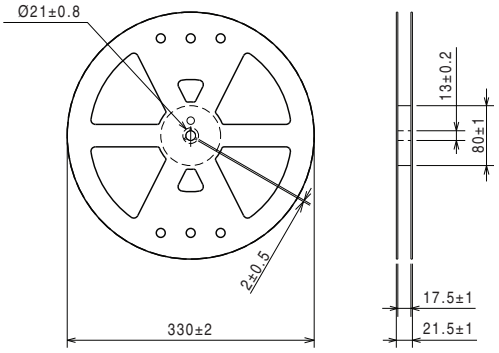
Dimensions



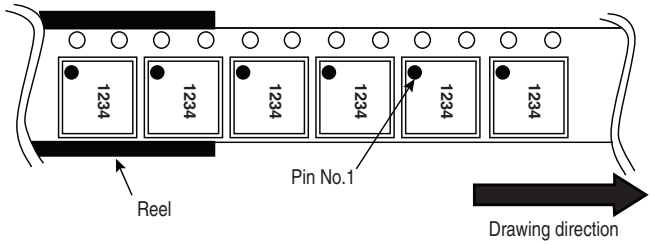
Tape Packaging

Packaging style: Embossed taping
Packaging quantity: 1,500 pcs/reel

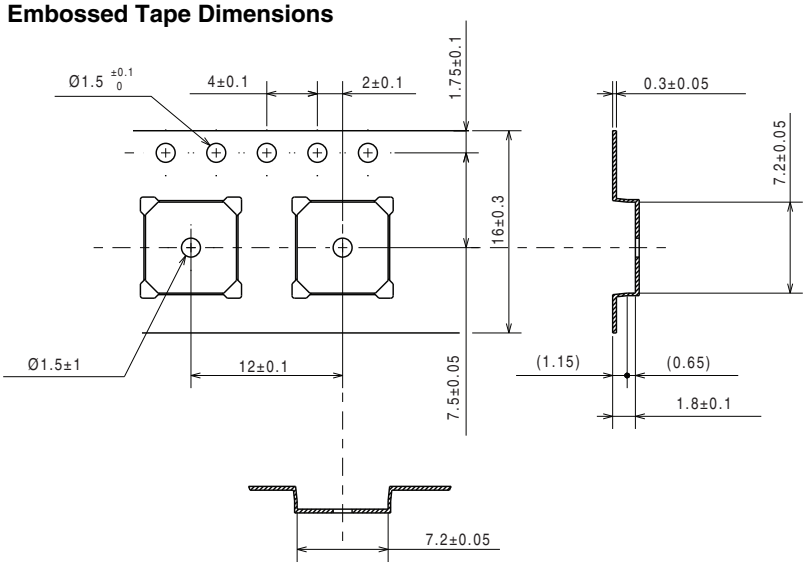
Reel Dimensions



Direction of Insertion



Embossed Tape Dimensions



Precautions for Use

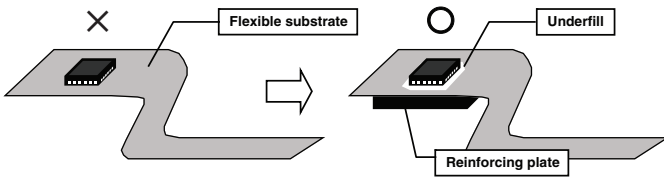
■ Correct Use

- The absolute maximum rating is the limit value which should not be exceeded even momentarily. Exceeding this value can cause deterioration of the characteristics or complete failure of the IC.
- Check the operation at the communication frequency to be used before using the device.
- Sufficiently take into consideration the static electricity, chattering and voltage of the input to be connected when determining each input circuit.
- Although the device contains an ESD protection circuit, static electricity that exceeds the function may damage the device. When handling the device, exercise due caution by, for example, grounding the body of the handler.
- Execute thermal design providing for a sufficient margin, by considering allowable dissipation in the actual operating condition. If a high voltage is applied to IC (e.g. due to a small number of driven series LEDs), heating of the IC can be controlled by inserting a resistance to disperse power dissipation.
- A thermal shutdown circuit is built in this IC. If chip temperature has risen abnormally, this circuit works to open output terminals. The original condition is restored when chip temperature has decreased to a normal level. As this circuit is provided as protection in the event of emergency, do not use it on a regular basis.
- Due to potential damage, do not use product that has been dropped or that has come into contact with water.

■ Cautions on Mounting

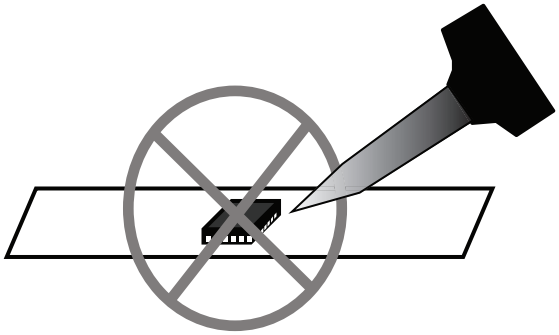
Mounting on a Flexible Substrate

When mounting the product on a flexible substrate, a reed may be detached after mounting due to stress transmitted through the substrate. Therefore, it is recommended to use, for mounting, a reinforced substrate or an underfill, etc.



Reworking with a Soldering Iron

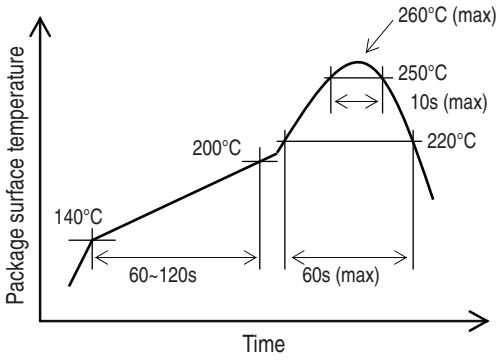
The user is strictly admonished against the use of soldering iron for rework. Such a use may cause mold cracking or open terminals.



■ Recommended Reflow Conditions

Allowable Temperature Profile Conditions

Product mounting method should be by Reflow and we recommend the following temperature profile. Reflow no more than twice.



Storage Conditions before Mounting

Moisture absorption by the plastic package will increase the possibility of faults, such as cracks; therefore, take enough care for storage.

	Storage Conditions	Period
Before moisture-proof package is opened	5 to 30°C, 40 to 70%RH	1 Year
After moisture-proof package is opened	5 to 30°C, 40 to 70%RH	168 hours

Recommended Drying Conditions

If the allowable storage period after opening a moisture-proof package has been exceeded, dry the products under the following conditions before mounting them:

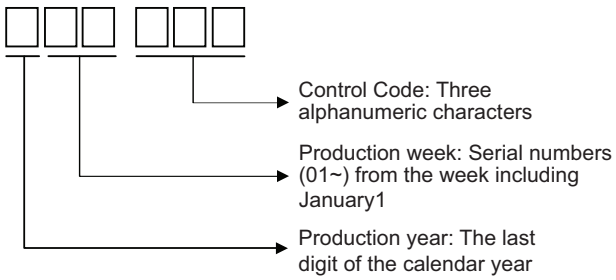
Temperature	Time	Frequency
60°C	72 hours	Once or twice

■ RoHS Directive Compliance

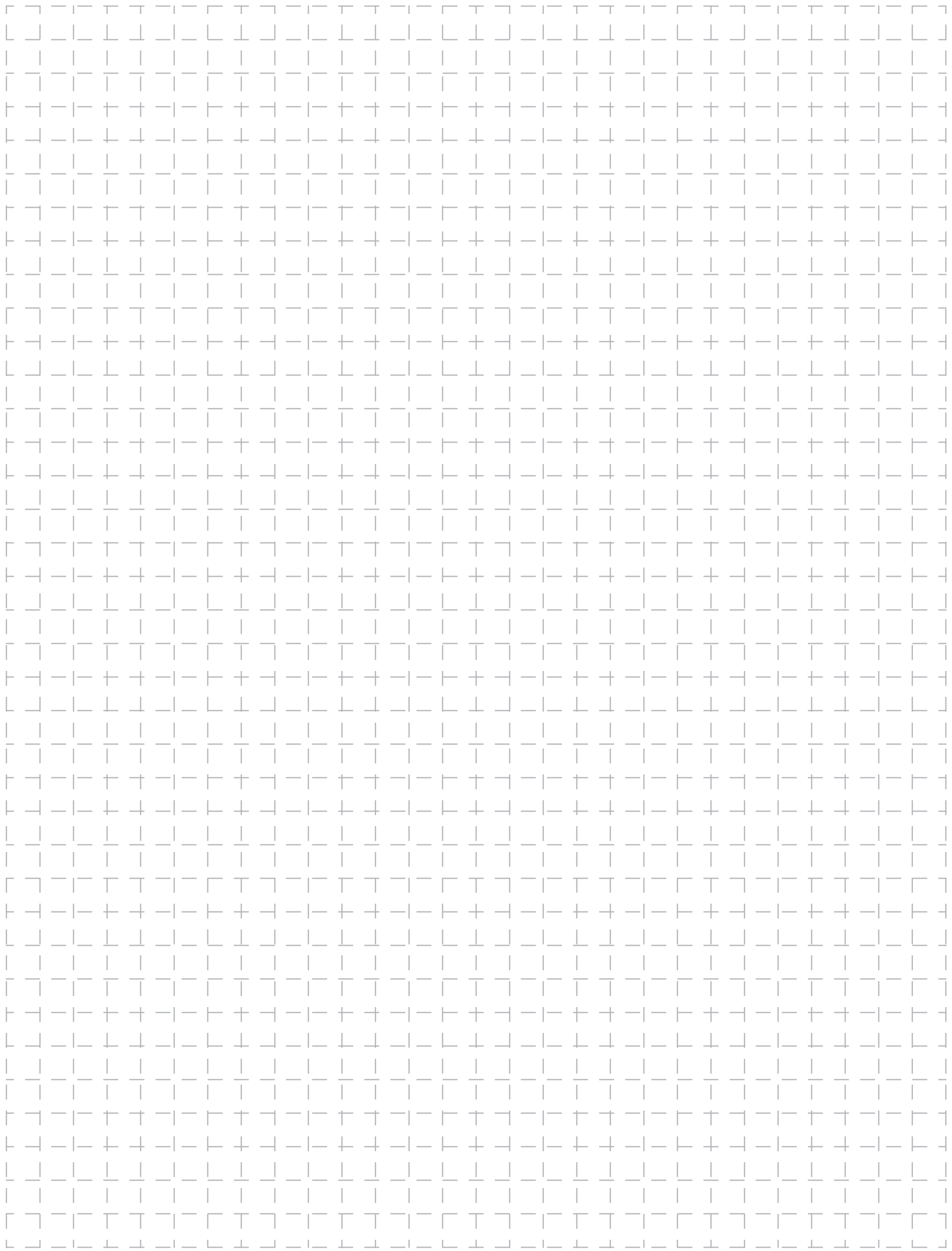
Models that are indicated as being RoHS compliant do not exceed the threshold value for the following six substances.

Lead:	1,000 ppm max.
Mercury:	1,000 ppm max.
Cadmium:	100 ppm max.
Hexavalent chromium:	1,000 ppm max.
PBB:	1,000 ppm max.
PBDE:	1,000 ppm max.

■ Lot Code Indication



MEMO



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