AXM0F243

SoC Ultra-Low Power RF-Microcontroller for RF Carrier Frequencies in the Range 27 - 1050 MHz

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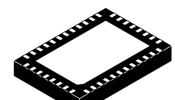


1 40

QFN40 7x5, 0.5P
CASE 485EG

ORDERING INFORMATION

See detailed ordering and shipping information in Table 58 of this data sheet.

OVERVIEW

Features

System−on−Chip (SoC) Ultra−low Power Advanced Narrow−band RF−microcontroller for Wireless Communication Applications

- QFN40 Package
- Supply Range 1.8 V − 3.6 V
- −40°C to 85°C
- Deep Sleep Mode with Operational Analog and 2.5 μA Digital System Current
- Radio RX−mode
  6.5 mA @ 169 MHz
  9.5 mA @ 868 MHz and 433 MHz
- Radio TX−mode at 868 MHz
  7.6 mA @ 0 dBm
  21 mA @ 10 dBm
  55 mA @ 15 dBm
- This is a Pb−Free Device

32−bit MCU Subsystem

- 48−MHz ARM Cortex−M0+ CPU
- Up to 64 KB of Flash with Read Accelerator
- Up to 8 KB of SRAM

Programmable Analog

- Two opamps with reconfigurable high−drive external and high−bandwidth internal drive and Comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low−power mode.
- 12−bit 1−Msps SAR ADC with differential and single−ended modes
- Single−slope 10−bit ADC function
- Two current DACs (IDACs) for general−purpose applications on any pin
- Two low−power comparators that operate in Deep Sleep low−power mode

Programmable Digital

- Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs

Low−Power 1.8 V to 3.6 V Operation

- Deep Sleep mode with operational analog and 2.5 μA digital system current

Serial Communication

- Two independent run−time reconfigurable Serial Communication Blocks (SCBs) with re−configurable I^2C, SPI, or UART functionality

Timing and Pulse−Width Modulation

- Five 16−bit timer/counter/pulse−width modulator (TCPWM) blocks
- Center−aligned, Edge, and Pseudo−random modes
- Comparator−based triggering of Kill signals for motor drive and other high−reliability digital logic applications

Up to 20 Programmable GPIO Pins

- Any GPIO pin can be analog, or digital
- Drive modes, strengths, and slew rates are programmable

High Performance Narrow−band RF Transceiver compatible to AX5043 (FSK/MSK/4−FSK/GFSK/GMSK/ASK/AFSK/FM/PSK)

- Receiver
  - Carrier Frequencies from 27 to 1050 MHz
  - Data Rates from 0.1 kbps to 125 kbps
  - Optional Forward Error Correction (FEC)
  - Sensitivity without FEC
    −135 dBm @ 0.1 kbps, 868 MHz, FSK
    −126 dBm @ 1 kbps, 868 MHz, FSK
    −117 dBm @ 10 kbps, 868 MHz, FSK
    −107 dBm @ 100 kbps, 868 MHz, FSK
    −105 dBm @ 125 kbps, 868 MHz, FSK

    −138 dBm @ 0.1 kbps, 868 MHz, PSK
    −130 dBm @ 1 kbps, 868 MHz, PSK
    −120 dBm @ 10 kbps, 868 MHz, PSK
    −109 dBm @ 100 kbps, 868 MHz, PSK
    −108 dBm @ 125 kbps, 868 MHz, PSK
  - Sensitivity with FEC
    −137 dBm @ 0.1 kbps, 868 MHz, FSK
    −122 dBm @ 5 kbps, 868 MHz, FSK
    −111 dBm @ 50 kbps, 868 MHz, FSK
  - High Selectivity Receiver with up to 47 dB Adjacent Channel Rejection
  - 0 dBm Maximum Input Power
  - ±10% Data−rate Error Tolerance
  - Support for Antenna Diversity with External Antenna Switch
  - Short Preamble Modes allow the Receiver to work with as little as 16 Preamble Bits
  - Fast State Switching Times
    200 μs TX → RX Switching Time
    62 μs RX → TX Switching Time
- Transmitter
  - Carrier Frequencies from 27 to 1050 MHz
  - Data−rates from 0.1 kbps to 125 kbps
  - High Efficiency, High Linearity Integrated Power Amplifier
  - Maximum Output Power
    16 dBm @ 868 MHz
    16 dBm @ 433 MHz
    16 dBm @ 169 MHz
  - Power Level programmable in 0.5 dB Steps
  - GFSK Shaping with BT=0.3 or BT=0.5
  - Unrestricted Power Ramp Shaping
- RF Frequency Generation
  - Configurable for Usage in 27 MHz −1050 MHz Bands
  - RF Carrier Frequency and FSK Deviation Programmable in 1 Hz Steps
  - Ultra Fast Settling RF Frequency Synthesizer for Low−power Consumption
  - Fully Integrated RF Frequency Synthesizer with VCO Auto−ranging and Band−width Boost Modes for Fast Locking
  - Configurable for either Fully Integrated VCO, Internal VCO with External Inductor or Fully External VCO
  - Configurable for either Fully Integrated or External Synthesizer Loop Filter for a Large Range of Bandwidths
  - Channel Hopping up to 2000 hops/s
  - Automatic Frequency Control (AFC)
- Flexible Antenna Interface
  - Integrated RX/TX Switching with Differential Antenna Pins
  - Mode with Differential RX Pins and Single−ended TX Pin for Usage with External PAs and for Maximum PA Efficiency at Low Output Power
- Wakeup−on−Radio
  - 640 Hz or 10 kHz Lowest Power Wake−up Timer
  - Wake−up Time Interval programmable between 98 μs and 102 s
- Sophisticated Radio Controller
  - Antenna Diversity and RX/TX Switch Control
  - Fully Automatic Packet Reception and Transmission without Micro−controller Intervention
  - Supports HDLC, Raw, Wireless M−Bus Frames and Arbitrary Defined Frames
  - Automatic Channel Noise Level Tracking
  - μs Resolution Timestamps for Exact Timing (eg. for Frequency Hopping Systems)
  - 256 Byte Micro−programmable FIFO, optionally supports Packet Sizes > 256 Bytes
  - Three Matching Units for Preamble Byte, Sync−word and Address
  - Ability to store RSSI, Frequency Offset and Data−rate Offset with the Packet Data
  - Multiple Receiver Parameter Sets allow the use of more aggressive Receiver Parameters during Preamble, dramatically shortening the Required Preamble Length at no Sensitivity Degradation
- Advanced Crystal Oscillator (RF Reference Oscillator)
  - Fast Start−up and Lowest Power Steady−state XTAL Oscillator for a Wide Range of Crystals
  - Integrated Tuning Capacitors
  - Possibility of Applying an External Clock Reference (TCXO)

Applications

27 − 1050 MHz Licensed and Unlicensed Radio Systems

- Internet of Things
- Automatic meter reading (AMR)
- Security applications
- Building automation
- Wireless networks
- Messaging Paging
- Compatible with: Wireless M−Bus, POCSAG, FLEX, KNX, Sigfox, Z−Wave, enocean
- Regulatory Regimes: EN 300 220 V2.3.1 including the Narrow−band 12.5 kHz, 20 kHz and 25 kHz Definitions; EN 300 422; FCC Part 15.247; FCC Part 15.249; FCC Part 90 6.25 kHz, 12.5 kHz and 25 kHz

BLOCK DIAGRAM

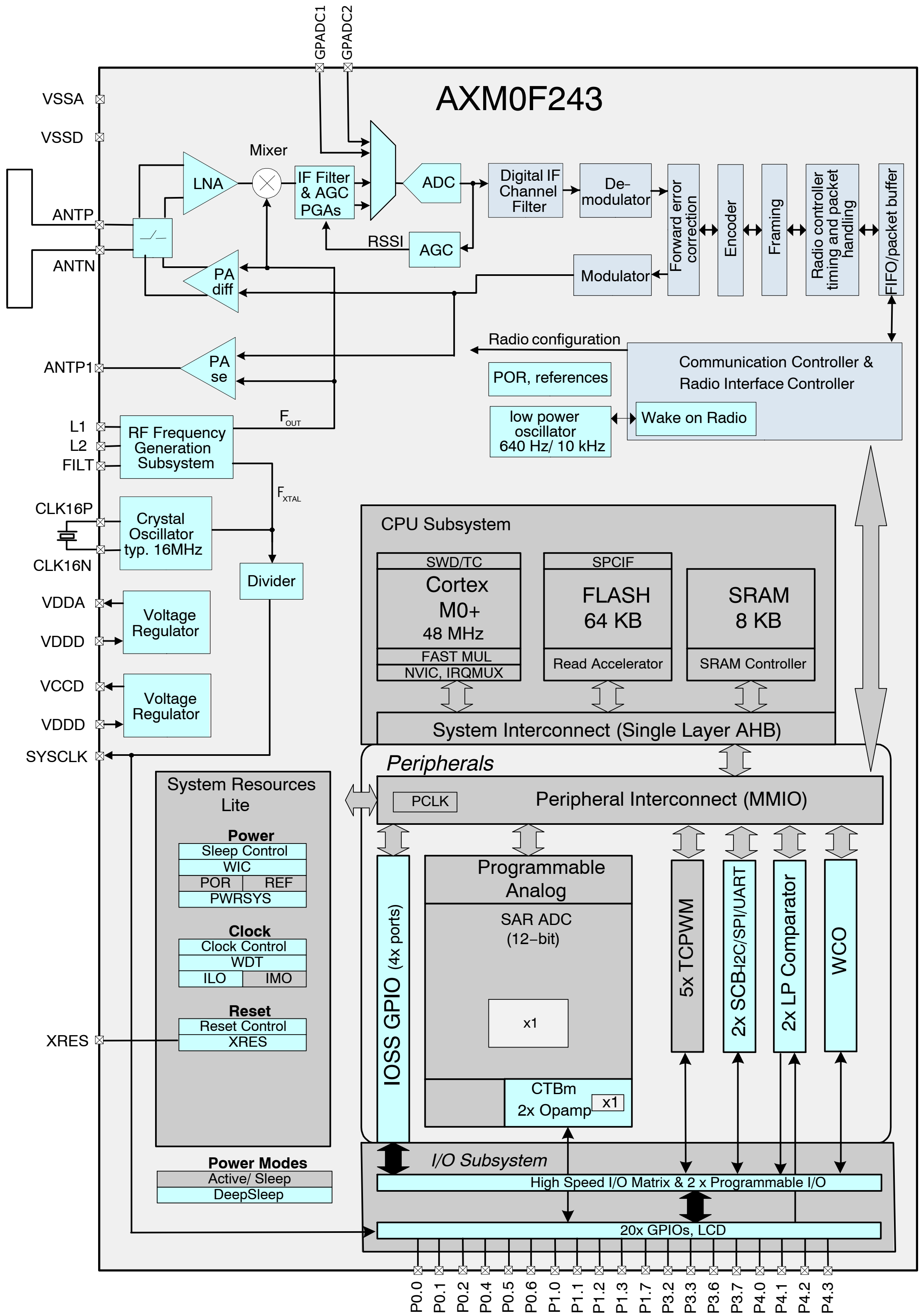


Figure 1. Functional Block Diagram of the AXM0F243

Table 1. PIN FUNCTION DESCRIPTION

Symbol	Pin(s)	Type	Description
VDDA	1	P	Analog power output, decouple to neighboring VSSA
VSSA	2	P	Ground, decouple to neighboring VDDA
ANTP	3	A	Differential antenna input/output
ANTN	4	A	Differential antenna input/output
ANTP1	5	A	Single−ended antenna output
VSSA	6	P	Ground, decouple to neighboring VDDA
VDDA	7	P	Analog power output, decouple to neighboring VSSA
VSSA	8	P	Ground
FILT	9	A	Optional synthesizer filter
L2	10	A	Optional synthesizer inductor
L1	11	A	Optional synthesizer inductor
VSSD	12	P	Ground
SYSCLK	13	I/O/PU	Default functionality: system clock output
P3.2	14	I/O/PU/PD/A	General purpose IO
P3.3	15	I/O/PU/PD/A	General purpose IO
P3.6	16	I/O/PU/PD/A	General purpose IO
P3.7	17	I/O/PU/PD/A	General purpose IO
P4.0	18	I/O/PU/PD/A	General purpose IO
P4.1	19	I/O/PU/PD/A	General purpose IO
P4.2	20	I/O/PU/PD/A	General purpose IO
P4.3	21	I/O/PU/PD/A	General purpose IO
P0.0	22	I/O/PU/PD/A	General purpose IO
P0.1	23	I/O/PU/PD/A	General purpose IO
P0.2	24	I/O/PU/PD/A	General purpose IO
P0.4	25	I/O/PU/PD/A	General purpose IO
P0.5	26	I/O/PU/PD/A	General purpose IO
P0.6	27	I/O/PU/PD/A	General purpose IO
XRES	28	I/PU	Reset pin
VCCD	29	P	Regulated digital supply, decouple to ground
VDDD	30	P	Unregulated power supply
P1.0	31	I/O/PU/PD/A	General purpose IO
P1.1	32	I/O/PU/PD/A	General purpose IO
P1.2	33	I/O/PU/PD/A	General purpose IO
P1.3	34	I/O/PU/PD/A	General purpose IO
P1.7	35	I/O/PU/PD/A	General purpose IO
VDDD	36	P	Unregulated power supply
GPADC1	37	A	GPADC input, must be connected to GND if not used
GPADC2	38	A	GPADC input, must be connected to GND if not used
CLK16N	39	A	Crystal oscillator input/output (RF reference oscillator)
CLK16P	40	A	Crystal oscillator input/output (RF reference oscillator)
GND	Center pad	P	Ground on center pad of QFN, must be connected

A = analog input
I = digital input signal
O = digital output signal
PU = pull−up
N = not to be connected
P = power or ground
PD = pull−down

Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for instance, be an analog I/O or a digital peripheral function. The pin assignments are shown in the following table.

Table 2. ALTERNATE PIN FUNCTIONS

Pin	HSIOM_PORT_SEL[x].SELy (*5)					
	Active				DeepSleep	
	ACTIVE #0	ACTIVE #1	ACTIVE #2	ACTIVE #3	Deep Sleep #2	Deep Sleep #3
P0.0		scb[2].uart_cts:0	pass.dsi_sar_data_valid:0	tcpwm.tr_in[0]	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1		scb[2].uart_rts:0	pass.tr_sar_out	tcpwm.tr_in[1]	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2			pass.dsi_sar_sample_done			scb[0].spi_select3:0
P0.4		scb[1].uart_rx:0	pass.dsi_sar_data[0]:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5		scb[1].uart_tx:0	pass.dsi_sar_data[1]:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6	srss.ext_clk	scb[1].uart_cts:0		scb[2].uart_tx:1		scb[1].spi_clk:1
P1.0	tcpwm.line[2]:1	scb[0].uart_rx:1			scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	tcpwm.line_compl[2]:1	scb[0].uart_tx:1			scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	tcpwm.line[3]:1	scb[0].uart_cts:1	pass.dsi_sar_data[3]:0	tcpwm.tr_in[2]	scb[2].i2c_scl:1	scb[0].spi_clk:1
P1.3	tcpwm.line_compl[3]:1	scb[0].uart_rts:1	pass.dsi_sar_data[4]:0	tcpwm.tr_in[3]	scb[2].i2c_sda:1	scb[0].spi_select0:1
P1.7						scb[2].spi_clk
P3.2	tcpwm.line[1]:0	scb[1].uart_cts:1			cpuss.swd_data	scb[1].spi_clk:0
P3.3	tcpwm.line_compl[1]:0	scb[1].uart_rts:1			cpuss.swd_clk	scb[1].spi_select0:0
P3.6	tcpwm.line[3]:0		pass.dsi_ctb_cmp0			scb[1].spi_select3:0
P3.7	tcpwm.line_compl[3]:0		pass.dsi_ctb_cmp1		lpcomp.comp[1]:1	scb[2].spi_miso
P4.0		scb[0].uart_rx:0	pass.dsi_sar_data[9]:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1		scb[0].uart_tx:0			scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2		scb[0].uart_cts:0	pass.dsi_sar_data[10]:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3		scb[0].uart_rts:0	pass.dsi_sar_data[11]:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

PINOUT DRAWING

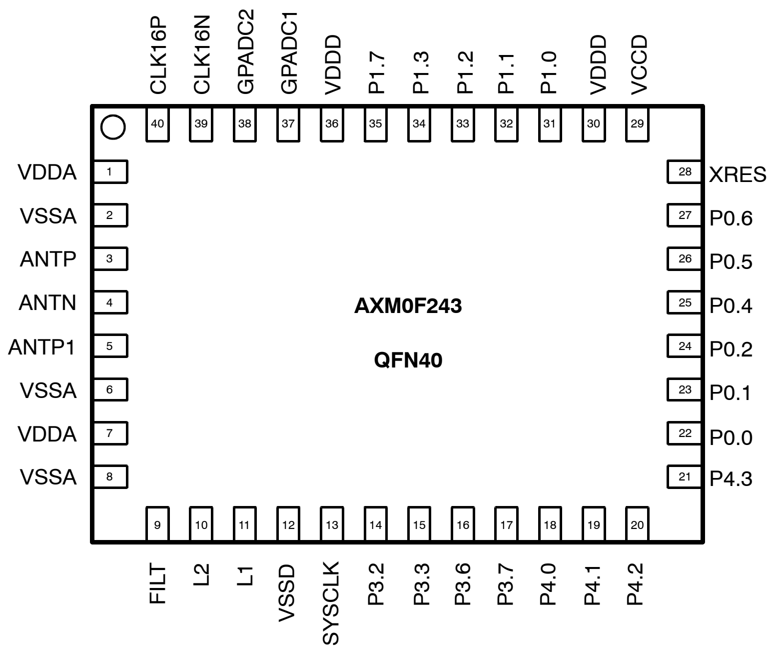


Figure 2. Pinout Drawing (Top View)

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Description	Condition	Min	Max	Units
VDDD	Supply voltage		−0.5	5.5	V
IDD	Supply current			200	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input	ANTP and ANTN pins in RX mode		10	dBm
I_{I1}	DC current into pin SYSCLK		−10	10	mA
I_{I2}	DC current into GPIO		−25	25	mA
I_{I3}	DC current into pins ANTP, ANTN, ANTP1		−100	100	mA
V_{ia}	Input voltage ANTP, ANTN, ANTP1 pins		−0.5	5.5	V
	Input voltage GPIO pins		−0.5	VDDD + 0.5	V
V_{es}	Electrostatic handling	HBM	−2000	2000	V
Lu	GPIO pin current for latch−up		−140	140	mA
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−65	150	°C
T_j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 4. SUPPLIES

Sym	Description	Condition	Min	Typ	Max	Units
T_{AMB}	Operational ambient temperature		−40	27	85	°C
VDDD	I/O and voltage regulator supply voltage		1.8	3.0	3.6	V
IDDsleep1	Sleep mode I^2C wakeup, WDT and Comparators on	6 MHz. Max is at 85°C and 3.6 V		1.7		mA
IDDsleep2	Sleep mode I^2C wakeup, WDT and Comparators on	12 MHz. Max is at 85°C and 3.6 V		2.2		mA
IDDdeep-sleep	Deep Sleep current I^2C wakeup and WDT on	Max is at 85°C and 3.6 V		2.5		μA
IDD6	CPU at 6 MHz, execute from flash	Max is at 85°C and 3.6 V		1.8		mA
IDD24	CPU at 24 MHz, execute from flash	Max is at 85°C and 3.6 V		3.0		mA
IDD48	CPU at 48 MHz, execute from flash	Max is at 85°C and 3.6 V		5.4		mA
IDDxres	Supply current while XRES asserted			2		mA
I_{RX}	Current consumption RX RF frequency generation subsystem: Internal VCO and internal loop−fiter	868 MHz, datarate 6 kbps		9.5		mA
		169 MHz, datarate 6 kbps		6.5		
		868 MHz, datarate 100 kbps		11		
		169 MHz, datarate 100 kbps		7.5		
$I_{TX-DIFF}$	Current consumption TX differential	868 MHz, 15 dBm, CW, Note 2 RF frequency generation subsystem: Internal VCO and internal loop−filter Antenna configuration: Differential PA, internal RX/TX switch		55		mA

2. Measured with optimized matching networks.

Table 4. SUPPLIES

Sym	Description	Condition	Min	Typ	Max	Units
I_{TX_SE}	Current consumption TX single ended	868 MHz, 0 dBm, FSK, Note 2 RF frequency generation subsystem: Internal VCO and internal loop−filter Antenna configuration: Single ended PA, external RX/TX switching		7.6		mA
I_{WOR}	Typical wake−on−radio duty cycle current	1 s, 100 kbps		6		μA

2. Measured with optimized matching networks.

For information on current consumption in complex modes of operation tailored to your application, see the software AX−RadioLab.

Both AXM0F243 power amplifiers run from the regulated VDDA supply and not directly from the battery. This has the advantage that the current and output power do not vary much over supply voltage and temperature.

Table 5. AC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
F_{CPU}	CPU frequency	DC	–	48	MHz	
T_{SLEEP} [3]	CPU Wakeup from Sleep mode	–	0	–	μs	
$T_{DEEPSLEEP}$ [3]	CPU Wakeup from Deep Sleep mode	–	35	–		

3. Guaranteed by characterization.

GPIO

Table 6. GPIO DC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
V_{IH} [4]	Input voltage high threshold	0.7 x V_{DDD}	–	–	V	CMOS Input
V_{IL}	Input voltage low threshold	–	–	0.3 x V_{DDD}		CMOS Input
V_{IH} [4]	LVTTL input, V_{DDD} < 2.7 V	0.7 x V_{DDD}	–	–		–
V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 x V_{DDD}		–
V_{IH} [4]	LVTTL input, $V_{DDD} \geq 2.7$ V	2.0	–	–		–
V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8		–
V_{OH}	Output voltage high level	$V_{DDD} - 0.6$	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
V_{OH}	Output voltage high level	$V_{DDD} - 0.5$	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
R_{PULLUP}	Pull–up resistor	3.5	5.6	8.5	kΩ	–
$R_{PULLDOWN}$	Pull–down resistor	3.5	5.6	8.5		–
I_{IL}	Input leakage current (absolute value)	–	–	1	μA	25°C, V_{DDD} = 3.0 V
C_{IN}	Input capacitance	–	–	7	pF	–
V_{HYSTTL} [5]	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
$V_{HYSCMOS}$ [5]	Input hysteresis CMOS	0.05 x V_{DDD}	–	–		
I_{TOT_GPIO} [5]	Maximum total source or sink chip current	–	–	200	mA	–

4. V_{IH} must not exceed V_{DDD} + 0.2 V
5. Guaranteed by characterization.

Table 7. GPIO AC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF
T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 3.6 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT2}$	GPIO F_{OUT}; 1.8 V ≤ V_{DDD} ≤ 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 3.6 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
$F_{GPIOUT4}$	GPIO F_{OUT}; 1.8 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
F_{GPIOIN}	GPIO input operating frequency; 1.8 V ≤ V_{DDD} ≤ 3.6 V	–	–	48		90/10% V_{IO}

*Guaranteed by characterization.

XRES

Table 8. XRES DC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
V_{IH}	Input voltage high threshold	0.7 x V_{DDD}	–	–	V	CMOS Input
V_{IL}	Input voltage low threshold	–	–	0.3 x V_{DDD}		CMOS Input
R_{PULLUP}	Pull−up resistor	–	60	–	kΩ	
C_{IN}	Input capacitance	–	–	7	pF	
$V_{HYSXRES}$ [6]	Input voltage hysteresis	–	100	–	mV	

Table 9. XRES AC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
$T_{RESETWIDTH}$ [6]	Reset pulse width	1	–	–	μs	
$T_{RESETWAKE}$ [6]	Wake−up time from reset release	–	–	2.7	ms	

6. Guaranteed by characterization.

Table 10. SYSCLK DC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
V_{IL}	Input voltage low threshold	–	–	0.8	V	at 3.3 V VDDD
V_{IH}	Input voltage high threshold	2.0	–	–	V	at 3.3 V VDDD
R_{PULLUP}	Pull−up resistor	–	65	–	kΩ	
V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 4 mA at 3 V VDDD
V_{OH}	Output voltage high level	2.4	–	–	V	I_{OH} = 4 mA at 3 V VDDD

Analog Peripherals

Table 11. CTBm OPAMP SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{DD}	Opamp block current, External load					
I_{DD_HI}	power=hi	–	1100	–	μA	–
I_{DD_MED}	power=med	–	550	–		–
I_{DD_LOW}	power=lo	–	150	–		–
G_{BW}	Load = 20 pF, 0.1 mA VDDD = 2.7 V					
G_{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to VDDD−0.2 V
G_{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to VDDD−0.2 V
G_{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to VDDD−0.2 V
I_{OUT_MAX}	VDDD = 2.7 V, 500 mV from rail					
$I_{OUT\_MAX\_HI}$	power=hi	10	–	–	mA	Output is 0.5 V VDDD−0.5 V
$I_{OUT\_MAX\_MID}$	power=mid	10	–	–		Output is 0.5 V VDDD−0.5 V
$I_{OUT\_MAX\_LO}$	power=lo	–	5	–		Output is 0.5 V VDDD−0.5 V
I_{OUT}	VDDD = 1.8 V, 500 mV from rail					

Table 11. CTBm OPAMP SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
IOUT_MAX_HI	power=hi	4	–	–		Output is 0.5 V VDDD−0.5 V
IOUT_MAX_MID	power=mid	4	–	–	mA	Output is 0.5 V VDDD−0.5 V
IOUT_MAX_LO	power=lo	–	2	–		Output is 0.5 V VDDD−0.5 V
IDD_Int	Opamp block current Internal Load					
IDD_HI_Int	power=hi	–	1500	–	µA	–
IDD_MED_Int	power=med	–	700	–		–
IDD_LOW_Int	power=lo	–	–	–		–
GBW	VDDD = 2.7 V	–	–	–		–
GBW_HI_Int	power=hi	8	–	–	MHz	Output is 0.25 V to VDDD−0.25 V
	General opamp specs for both internal and external modes					
VIN	Charge−pump on, VDDD = 2.7 V	−0.05	–	VDDD−0.2	V	–
VCM	Charge−pump on, VDDD = 2.7 V	−0.05	–	VDDD−0.2		–
VOUT	VDDD = 2.7 V					
VOUT_1	power=hi, Iload=10 mA	0.5	–	VDDD −0.5	V	–
VOUT_2	power=hi, Iload=1 mA	0.2	–	VDDD −0.2		–
VOUT_3	power=med, Iload=1 mA	0.2	–	VDDD −0.2		–
VOUT_4	power=lo, Iload=0.1 mA	0.2	–	VDDD −0.2		–
VOS_TR	Offset voltage, trimmed	−1.0	±0.5	1.0	mV	High mode, input 0 V to VDDD−0.2 V
VOS_TR	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to VDDD−0.2 V
VOS_TR	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to VDDD−0.2 V
VOS_DR_TR	Offset voltage drift, trimmed	−10	±3	10	µV/C	High mode
VOS_DR_TR	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
VOS_DR_TR	Offset voltage drift, trimmed	–	±10	–		Low mode
CMRR	DC	70	80	–	dB	Input is 0 V to VDDD−0.2 V, Output is 0.2 V to VDDD−0.2 V
PSRR	At 1 kHz, 10−mV ripple	70	85	–		V_{DDD} = 3.6 V, high−power mode, input is 0.2 V to VDDD−0.2 V

Table 11. CTBm OPAMP SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Noise						
VN2	Input−referred, 1 kHz, power=Hi	–	72	–	nV/rtHz	3
VN3	Input−referred, 10 kHz, power=Hi	–	28	–		Input and output are at 0.2 V to VDDD−0.2 V
VN4	Input−referred, 100 kHz, power=Hi	–	15	–		Input and output are at 0.2 V to VDDD−0.2 V
C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SLEW_RATE	Cload = 50 pF, Power = High, VDDD = 2.7 V	6	–	–	V/μs	–
T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	μs	–
OL_GAIN	Open Loop Gain	–	90	–	dB	
COMP_MODE	Comparator mode; 50 mV drive, T_{rise}=T_{fall} (approx.)					
TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to VDDD−0.2 V
TPD2	Response time; power=med	–	500	–		Input is 0.2 V to VDDD−0.2 V
TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to VDDD−0.2 V
VHYST_OP	Hysteresis	–	10	–	mV	–
WUP_CTB	Wake−up time from Enabled to Usable	–	–	25	μs	–
Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
$I_{DD\_HI\_M1}$	Mode 1, High current	–	1400	–	μA	25°C
$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	700	–		25°C
$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	200	–		25°C
$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–		25°C
$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–		25°C
$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–		25°C

Table 11. CTBm OPAMP SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
GBW_HI_M1	Mode 1, High current	–	4	–	MHz	20−pF load, no DC load 0.2 V to VDDD−0.2 V
GBW_MED_M1	Mode 1, Medium current	–	2	–		20−pF load, no DC load 0.2 V to VDDD−0.2 V
GBW_LOW_M1	Mode 1, Low current	–	0.5	–		20−pF load, no DC load 0.2 V to VDDD−0.2 V
GBW_HI_M2	Mode 2, High current	–	0.5	–		20−pF load, no DC load 0.2 V to VDDD−0.2 V
GBW_MED_M2	Mode 2, Medium current	–	0.2	–		20−pF load, no DC load 0.2 V to VDDD−0.2 V
GBW_Low_M2	Mode 2, Low current	–	0.1	–		20−pF load, no DC load 0.2 V to VDDD−0.2 V
VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25°C, 0.2 V to VDDD−0.2 V
VOS_MED_M1	Mode 1, Medium current	–	5	–		With trim 25°C, 0.2 V to VDDD−0.2 V
VOS_LOW_M2	Mode 1, Low current	–	5	–		With trim 25°C, 0.2 V to VDDD−0.2 V
VOS_HI_M2	Mode 2, High current	–	5	–		With trim 25°C, 0.2V to VDDD−0.2 V
VOS_MED_M2	Mode 2, Medium current	–	5	–		With trim 25°C, 0.2 V to VDDD−0.2 V
VOS_LOW_M2	Mode 2, Low current	–	5	–		With trim 25°C, 0.2 V to VDDD−0.2 V
IOUT_HI_M!	Mode 1, High current	–	10	–	mA	Output is 0.5 V to VDDD−0.5 V
IOUT_MED_M1	Mode 1, Medium current	–	10	–		Output is 0.5 V to VDDD−0.5 V
IOUT_LOW_M1	Mode 1, Low current	–	4	–		Output is 0.5 V to VDDD−0.5 V
IOUT_HI_M2	Mode 2, High current	–	1	–		
IOU_MED_M2	Mode 2, Medium current	–	1	–		
IOU_LOW_M2	Mode 2, Low current	–	0.5	–		

Table 12. COMPARATOR DC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
VOFFSET1	Input offset voltage, Factory trim	–	–	±10	mV	
VOFFSET2	Input offset voltage, Custom trim	–	–	±4		
VHYST	Hysteresis when enabled	–	10	35		
VICM1	Input common mode voltage in normal mode	0	–	V_{DDD}−0.1	V	Modes 1 and 2
VICM2	Input common mode voltage in low power mode	0	–	V_{DDD}		
VICM3	Input common mode voltage in ultra low power mode	0	–	V_{DDD}−1.15		$V_{DDD} \geq$ 2.2 V at –40°C

Table 12. COMPARATOR DC SPECIFICATIONS

CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V
CMRR	Common mode rejection ratio	42	–	–		$V_{DDD} \leq 2.7$ V
ICMP1	Block current, normal mode	–	–	400	µA	
ICMP2	Block current, low power mode	–	–	100		
ICMP3	Block current in ultra low–power mode	–	–	6		$V_{DDD} \geq 2.2$ V at –40°C
ZCMP	DC Input impedance of comparator	35	–	–	MΩ	

Table 13. COMPARATOR AC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
TRESP3	Response time, ultra–low power mode, 200 mV overdrive	–	2.3	15	µs	$V_{DD} \geq 2.2$ V at –40°C

Table 14. TEMPERATURE SENSOR SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85°C

Table 15. SAR SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC DC Specifications						
A_RES	Resolution	–	–	12	bits	
A–MONO	Monotonicity	–	–	–		Yes.
A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1–V reference
A_ISAR	Current consumption	–	–	1	mA	
A_VINS	Input voltage range – single ended	VSS	–	VDDD	V	
A_VIND	Input voltage range – differential[	VSS	–	VDDD	V	
A_INRES	Input resistance	–	–	2.2	KΩ	
A_INCAP	Input capacitance	–	–	10	pF	
SAR ADC AC Specifications						
A_PSRR	Power supply rejection ratio	70	–	–	dB	
A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
A_SAMP	Sample rate	–	–	1	Msps	
A_SNR	Signal–to–noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	
A_INL	Integral non linearity V_{DD} = 1.8 V to 3.6 V, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 V to V_{DD}
A_INL	Integral non linearity. V_{DD} = 1.8 V to 3.6 V, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.8 V to V_{DD}
A_INL	Integral non linearity. V_{DD} = 1.8 V to 3.6 V, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 V to V_{DD}
A_DNL	Differential non linearity. V_{DD} = 1.8 V to 3.6 V, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}

Table 15. SAR SPECIFICATIONS

A_DNL	Differential non linearity. V_{DD} = 1.8 V to 3.6 V, 1 Msps	–1	–	2	LSB	V_{REF} = 1.8 V to V_{DD}
A_DNL	Differential non linearity. V_{DD} = 1.8 V to 3.6 V, 500 ksps	–1	–	2.2	LSB	V_{REF} = 1 V to V_{DD}
A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
FSARINTRE F	SAR operating speed without external ref. bypass	–	–	100	ksps	12–bit resolution

Table 16. CSD AND IDAC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25°C T_A, Sensitivity = 0.1 pF
VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75 V (with ripple), 25°C T_A, Parasitic Capaci–tance (C_P) < 20 pF, Sensi-tivity ≥ 0.4 pF
ICSD	Maximum block current	–	–	4000	μA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
VREF	Voltage reference for CSD and Comparator	0.6	1.2	VDDD – 0.6	V	VDDD – 0.06 or 4.4, whichever is lower
VREF_EXT	External Voltage reference for CSD and Com-parator	0.6		VDDD – 0.6	V	VDDD – 0.06 or 4.4, whichever is lower
IDAC1IDD	IDAC1 (7–bits) block current	–	–	1750	μA	
IDAC2IDD	IDAC2 (7–bits) block current	–	–	1750	μA	
VCSD	Voltage range of operation	1.8	–	3.6	V	
VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	VDDD –0.6	V	VDDD – 0.06 or 4.4, whichever is lower
IDAC1DNL	DNL	–1	–	1	LSB	
IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for VDDD < 2 V
IDAC2DNL	DNL	–1	–	1	LSB	
IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for VDDD < 2 V
SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1–pF sensitivity. All use cases. VDDD > 2 V.
IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5–nA typ.
IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	μA	LSB = 300–nA typ.
IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	μA	LSB = 2.4–μA typ.
IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	μA	LSB = 75–nA typ.
IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	μA	LSB = 600–nA typ.
IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	μA	LSB = 4.8–μA typ.
IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	μA	LSB = 37.5–nA typ.

Table 16. CSD AND IDAC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300–nA typ.
IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	µA	LSB = 2.4–µA typ.
IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75–nA typ.
IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600–nA typ.
IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8–µA typ.
IDAC3CRT13	Output current of IDAC in 8–bit mode in low range	8	–	10.5	µA	LSB = 37.5–nA typ.
IDAC3CRT23	Output current of IDAC in 8–bit mode in medium range	69	–	82	µA	LSB = 300–nA typ.
IDAC3CRT33	Output current of IDAC in 8–bit mode in high range	540	–	660	µA	LSB = 2.4–µA typ.
IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
IDACGAIN	Full–scale error less offset	–	–	±10	%	
IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5–nA typ.
IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medi-um mode	–	–	5.6	LSB	LSB = 300–nA typ.
IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4–µA typ.
IDACSET8	Settling time to 0.5 LSB for 8–bit IDAC	–	–	10	µs	Full–scale transition. No external load.
IDACSET7	Settling time to 0.5 LSB for 7–bit IDAC	–	–	10	µs	Full–scale transition. No external load.
CMOD	External modulator capacitor.	–	2.2	–	nF	5–V rating, X7R or NP0 cap.

Table 17. 10–BIT CSD ADC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
A_RES	Resolution	–	–	10	bits	Auto–zeroing is required every millisecond
A_CHNLS_S	Number of channels – single ended	–	–	16		Defined by AMUX Bus.
A–MONO	Monotonicity	–	–	–	Yes	
A_GAINERR	Gain error	–	–	±2	%	In V_{REF} (2.4 V) mode with VDDD bypass capacitance of 10 µF
A_OFFSET	Input offset voltage	–	–	3	mV	In V_{REF} (2.4 V) mode with VDDD bypass capacitance of 10 µF
A_ISAR	Current consumption	–	–	0.25	mA	
A_VINS	Input voltage range – single ended	VSSA	–	VDDD	V	
A_INRES	Input resistance	–	2.2	–	KΩ	
A_INCAP	Input capacitance	–	20	–	pF	

Table 17. 10–BIT CSD ADC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with VDDD bypass capacitance of 10 μF
A_TACQ	Sample acquisition time	–	1	–	μs	
A_CONV8	Conversion time for 8–bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	μs	Does not include acqui– sition time. Equivalent to 44.8 ksps including acqui- sition time.
A_CONV10	Conversion time for 10–bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	μs	Does not include acqui– sition time. Equivalent to 11.6 ksps including acqui- sition time.
A_SND	Signal–to–noise and Distortion ratio (SINAD)	–	61	–	dB	With 10–Hz input sine wave, external 2.4–V refer- ence, V_{REF} (2.4 V) mode
A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8–bit resolution
A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater
A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse–Width Modulator (TCPWM)

Table 18. TCPWM SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maxi- mum = 48 MHz
$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events [7]
$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Com- pare value) outputs
TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width be- tween Quadrature phase inputs

7. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

I^2C

Table 19. FIXED I^2C DC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	
I_{I2C2}	Block current consumption at 400 kHz	–	–	135		
I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		
I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	μA	

*Guaranteed by characterization.

Table 20. FIXED I^2C AC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
F_{I2C1}	Bit rate	–	–	1	Mbps	

*Guaranteed by characterization.

Table 21. SPI DC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
ISPI1	Block current consumption at 1 Mbps	–	–	360	μA	
ISPI2	Block current consumption at 4 Mbps	–	–	560		
ISPI3	Block current consumption at 8 Mbps	–	–	600		

*Guaranteed by characterization.

Table 22. SPI AC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	–
Fixed SPI Master Mode AC Specifications						
TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications						
TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*T_{CPU}		T_{CPU} = 1/F_{CPU}
TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
THSO	Previous MISO data hold time	0	–	–		–
TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

*Guaranteed by characterization.

Table 23. UART DC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{UART1}	Block current consumption at 100 Kbps	–	–	55	μA	
I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	μA	

*Guaranteed by characterization.

Table 24. UART AC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
F_{UART}	Bit rate	–	–	1	Mbps	

*Guaranteed by characterization.

Memory

Table 25. FLASH SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
$T_{ROWWRITE}$ [8]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
$T_{ROWERASE}$ [8]	Row erase time	–	–	16		–
$T_{ROWPROGRAM}$ [8]	Row program time after erase	–	–	4		–
$T_{BULKERASE}$ [8]	Bulk erase time (64 KB)	–	–	35		–
$T_{DEVPROG}$ [8] [9]	Total device program time	–	–	7	Seconds	–
F_{END} [9]	Flash endurance	100 K	–	–	Cycles	–
F_{RET} [9]	Flash retention. $T_A \leq 55°C$, 100 K P/E cycles	20	–	–	Years	–
	Flash retention. $T_A \leq 85°C$, 10 K P/E cycles	10	–	–		–
TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

8. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
9. Guaranteed by characterization.

System Resources

Power−on Reset (POR)

Table 26. POWER ON RESET (PRES)

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SR_POWER_UP	Power supply slew rate	3.3	–	67	V/ms	At power−up
$V_{RISEIPOR}$ [10]	Rising trip voltage	0.80	–	1.5	V	–
$V_{FALLIPOR}$ [10]	Falling trip voltage	0.70	–	1.4	V	–

10. Guaranteed by characterization.

Table 27. BROWN−OUT DETECT (BOD) FOR REGULATED DIGITAL VOLTAGE

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
$V_{FALLPPOR}$ [11]	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
$V_{FALLDPSLP}$ [11]	BOD trip voltage in Deep Sleep	1.11	–	1.5	V	–

11. Guaranteed by characterization.

SWD Interface

Table 28. SWD INTERFACE SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 3.6 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
F_SWDCLK2	1.8 V ≤ V_{DD} ≤ 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
T_SWDI_SETUP [12]	T = 1/f SWDCLK	0.25*T	–	–	ns	–
T_SWDI_HOLD [12]	T = 1/f SWDCLK	0.25*T	–	–		–
T_SWDO_VALID [12]	T = 1/f SWDCLK	–	–	0.5*T		–
T_SWDO_HOLD [12]	T = 1/f SWDCLK	1	–	–		–

12. Guaranteed by characterization.

Internal Main Oscillator

Table 29. IMO DC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	–
I_{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	–

*Guaranteed by design.

Table 30. IMO AC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	–
$T_{STARTIMO}$	IMO startup time	–	–	7	μs	–
$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low–Speed Oscillator

Table 31. ILO DC SPECIFICATIONS *

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
I_{ILO1}	ILO operating current	–	0.3	1.05	μA	–

*Guaranteed by design.

Table 32. ILO AC SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
$T_{STARTILO1}$ [13]	ILO startup time	–	–	2	ms	–
$T_{ILODUTY}$ [13]	ILO duty cycle	40	50	60	%	–
$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

13. Guaranteed by characterization.

Table 33. WATCH CRYSTAL OSCILLATOR (WCO) SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
FWCO	Crystal Frequency	–	32.768	–	kHz	
FTOL	Frequency tolerance	–	50	250	ppm	With 20–ppm crystal
ESR	Equivalent series resistance	–	50	–	kΩ	
PD	Drive Level	–	–	1	μW	

Table 33. WATCH CRYSTAL OSCILLATOR (WCO) SPECIFICATIONS

TSTART	Startup time	–	–	500	ms	
CL	Crystal Load Capacitance	6	–	12.5	pF	
C0	Crystal Shunt Capacitance	–	1.35	–	pF	
IWCO1	Operating Current (high power mode)	–	–	8	μA	
IWCO2	Operating Current (low power mode)	–	–	1	μA	

Table 34. BLOCK SPECS

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
TCLKSWITCH [13]	System clock source switching time	3	–	4	Periods	

Table 35. SMART I/O PASS−THROUGH TIME (DELAY IN BYPASS MODE)

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

Table 36. CRYSTAL OSCILLATOR (RF REFERENCE OSCILLATOR)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{XTAL}	Crystal or frequency	Note 1, 2, 3	10	16	50	MHz
gm_{osc}	Oscillator transconductance range	Self−regulated see note 4	0.2		20	mS
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	AX5043_XTALCAP = 0x00 default		3		pF
		AX5043_XTALCAP = 0x01		8.5		pF
		AX5043_XTALCAP = 0xFF		40		pF
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of AX5043_XTALCAP	AX5043_XTALCAP = 0x01 – 0xFF		0.5		pF
f_{ext}	External clock input (TCXO)	Note 2, 3, 5	10	16	50	MHz
RIN_{osc}	Input DC impedance		10			kΩ
$NDIV_{SYSCLK}$	Divider ratio $f_{SYSCLK} = F_{XTAL} / NDIV_{SYSCLK}$		2^0	2^4	2^{10}	

1. Tolerances and start−up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register AX5043_TRKFREQ.
2. The choice of crystal oscillator or TCXO frequency depends on the targeted regulatory regime for TX, see separate documentation on meeting regulatory requirements.
3. To avoid spurious emission, the crystal or TCXO reference frequency should be chosen so that the RF carrier frequency is not an integer multiple of the crystal or TCXO frequency.
4. The oscillator transconductance is regulated for fastest start−up time during start−up and for lowest power curing steady state oscillation. This means that values depend on the crystal used.
5. If an external clock or TCXO is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and AX5043_XTALCAP = 000000. For detailed TCXO network recommendations depending on the TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock.

Table 37. LOW−POWER OSCILLATOR (TRANSCEIVER WAKE ON RADIO CLOCK)

Symbol	Description	Condition	Min	Typ	Max	Units
$f_{osc-slow}$	Oscillator frequency slow mode LPOSC FAST = 0 in AX5043_LPOSCCONFIG register	No calibration	480	640	800	Hz
		Internal calibration vs. crystal clock has been performed	630	640	650	
$f_{osc-fast}$	Oscillator frequency fast mode LPOSC FAST = 1 in AX5043_LPOSCCONFIG register	No calibration	7.6	10.2	12.8	kHz
		Internal calibration vs. crystal clock has been performed	9.8	10.2	10.8	

Table 38. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{REF}	Reference frequency	The reference frequency must be chosen so that the RF carrier frequency is not an integer multiple of the reference frequency	10	16	50	MHz
Dividers						
$NDIV_{ref}$	Reference divider ratio range	Controlled directly with bits REFDIV in register AX5043_PLLVCODIV	2^0		2^3	
$NDIV_m$	Main divider ratio range	Controlled indirectly with register AX5043_FREQ	4.5		66.5	
$NDIV_{RF}$	RF divider range	Controlled directly with bit RFDIV in register AX5043_ PLLVCODIV	1		2	
Charge Pump						
I_{CP}	Charge pump current	Programmable in increments of 8.5 μA via register AX5043_PLLCPI	8.5		2168	μA
Internal VCO (VCOSEL = 0)						
f_{RF}	RF frequency range	RFDIV = 1	400		525	MHz
		RFDIV = 0	800		1050	
f_{step}	RF frequency step	RFDIV = 1 f_{REF} = 16.000000 MHz		0.98		Hz
BW	Synthesizer loop bandwidth	The synthesizer loop bandwidth an start−up time can be programmed with the registers AX5043_PLLLOOP and AX5043_PLLCPI. For recommendations see the AX5043 Programming Manual, the AX−RadioLab software and AX5043 Application Notes on compliance with regulatory regimes.	50		500	kHz
T_{start}	Synthesizer start−up time if crystal oscillator and reference are running		5		25	μs
PN868	Synthesizer phase noise 868 MHz f_{REF} = 48 MHz	10 kHz from carrier		−95		dBc/Hz
		1 MHz from carrier		−120		
PN433	Synthesizer phase noise 433 MHz f_{REF} = 48 MHz	10 kHz from carrier		−105		dBc/Hz
		1 MHz from carrier		−120		
VCO with external inductors (VCOSEL = 1, VCO2INT = 1)						
f_{RFrng_lo}	RF frequency range For choice of L_{ext} values as well as VCO gains see Figure 3 and Figure 4	RFDIV = 1	27		262	MHz
f_{RFrng_hi}		RFDIV = 0	54		525	
PN169	Synthesizer phase noise 169 MHz L_{ext}=47 nH (wire wound 0603) AX5043_RFDIV = 0, f_{REF}= 16 MHz Note: phase noises can be improved with higher f_{REF}	10 kHz from carrier		−97		dBc/Hz
		1 MHz from carrier		−115		
External VCO (VCOSEL = 1, VCO2INT = 0)						
f_{RF}	RF frequency range fully external VCO	Note: The external VCO frequency needs to be 2 x f_{RF}	27		1000	MHz
V_{amp}	Differential input amplitude at L1, L2 terminals			0.7		V
V_{inL}	Input voltage levels at L1, L2 terminals		0		1.8	V
V_{ctrl}	Control voltage range	Available at FILT in external loop filter mode	0		1.8	V

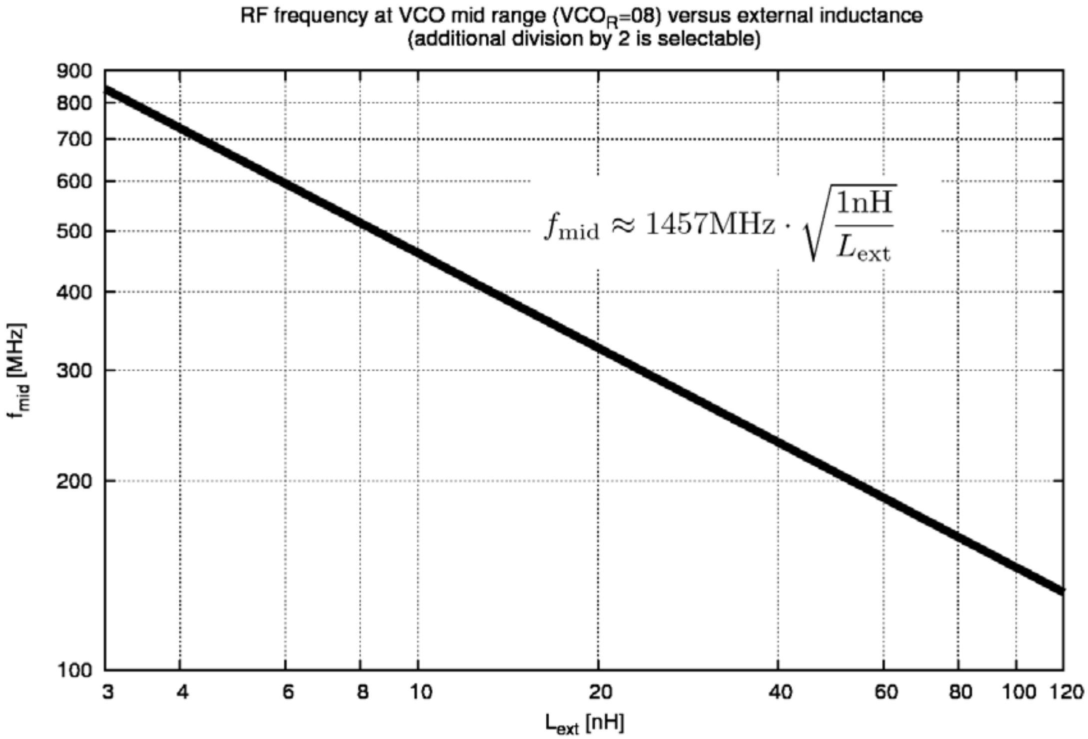


Figure 3. VCO with External Inductors: Typical Frequency vs. L_{ext}

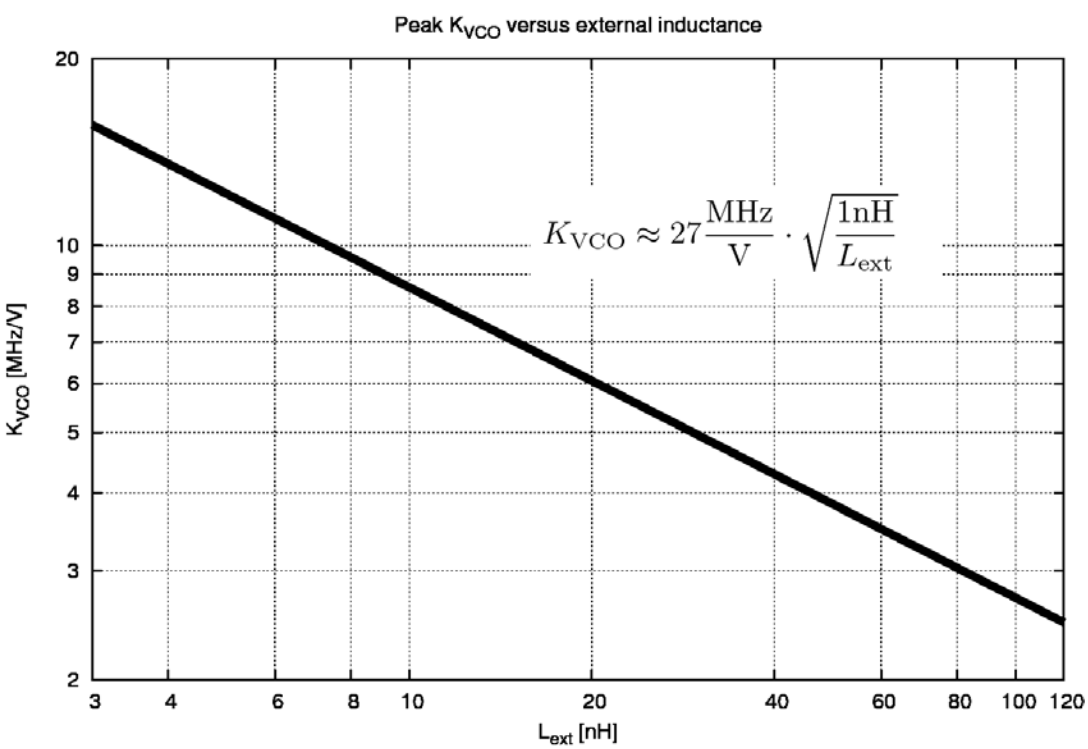


Figure 4. VCO with External Inductors: Typical K_{VCO} vs. L_{ext}

The following table shows the typical frequency ranges for frequency synthesis with external VCO inductor for different inductor values.

Table 39.

Lext [nH]	Freq [MHz] RFDIV = 0	Freq [MHz] RFDIV = 1	PLL Range
8.2	482	241	0
8.2	437	219	15
10	432	216	0
10	390	195	15
12	415	208	0
12	377	189	15
15	380	190	0
15	345	173	15
18	345	173	0
18	313	157	15
22	308	154	0
22	280	140	14
27	285	143	0
27	258	129	15
33	260	130	0
33	235	118	15
39	245	123	0
39	223	112	14
47	212	106	0
47	194	97	14
56	201	101	0
56	182	91	15
68	178	89	0
68	161	81	15
82	160	80	1
82	146	73	14
100	149	75	1
100	136	68	14
120	136	68	0
120	124	62	14

For tuning or changing of ranges a capacitor can be added in parallel to the inductor.

Table 40. TRANSMITTER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate		0.1		125	kbps
PTX	Transmitter power @ 868 MHz	Differential PA, 50 Ω single ended measurement at an SMA connector behind the matching network, Note 2	−10		16	dBm
	Transmitter power @ 433 MHz		−10		16	
	Transmitter power @ 169 MHz		−10		16	
PTX_{step}	Programming step size output power	Note 1			0.5	dB
dTX_{temp}	Transmitter power variation vs. temperature	−40°C to +85°C Note 2		± 0.5		dB
dTX_{Vdd}	Transmitter power variation vs. VDD_IO	1.8 to 3.6 V Note 2		± 0.5		dB
Padj	Adjacent channel power GFSK BT = 0.5, 500 Hz deviation, 1.2 kbps, 25 kHz channel spacing, 10 kHz channel BW	868 MHz		−44		dBc
		433 MHz		−51		
$PTX_{868-harm2}$	Emission @ 2nd harmonic	868 MHz, Note 2		−40		dBc
$PTX_{868-harm3}$	Emission @ 3rd harmonic			−60		
$PTX_{433-harm2}$	Emission @ 2nd harmonic	433 MHz, Note 2		−40		dBc
$PTX_{433-harm3}$	Emission @ 3rd harmonic			−40		

1. $P_{out} = \frac{AX5043\_TXPWRCOEFFB}{2^{12} - 1} \times P_{max}$

2. 50 Ω single ended measurements at an SMA connector behind the matching network. For recommended matching networks see Applications section.

Table 41. RECEIVER SENSITIVITIES

The table lists typical input sensitivities (without FEC) in dBm at the SMA connector with the complete matching network for BER=10^{-3} at 433 or 868 MHz.

Data rate [kbps]		FSK h = 0.66	FSK h = 1	FSK h = 2	FSK h = 4	FSK h = 5	FSK h = 8	FSK h = 16	PSK
0.1	Sensitivity [dBm]	−135	−134.5	−132.5	−133	−133.5	−133	−132.5	−138
	RX Bandwidth [kHz]	0.2	0.2	0.3	0.5	0.6	0.9	2.1	0.2
	Deviation [kHz]	0.033	0.05	0.1	0.2	0.25	0.4	0.8	
1	Sensitivity [dBm]	−126	−125	−123	−123.5	−124	−123.5	−122.5	−130
	RX Bandwidth [kHz]	1.5	2	3	6	7	11	21	1
	Deviation [kHz]	0.33	0.5	1	2	2.5	4	8	
10	Sensitivity [dBm]	−117	−116	−113	−114	−113.5	−113		−120
	RX Bandwidth [kHz]	15	20	30	50	60	110		10
	Deviation [kHz]	3.3	5	10	20	25	40		
100	Sensitivity [dBm]	−107	−105.5						−109
	RX Bandwidth [kHz]	150	200						100
	Deviation [kHz]	33	50						
125	Sensitivity [dBm]	−105	−104						−108
	RX Bandwidth [kHz]	187.5	200						125
	Deviation [kHz]	42.3	62.5						

1. Sensitivities are equivalent for 1010 data streams and PN9 whitened data streams.
2. RX bandwidths < 0.9 kHz cannot be achieved with an 48 MHz TCXO. A 16 MHz TCXO was used for all measurements at 0.1 kbps.

Table 42. RECEIVER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate		0.1		125	kbps
IS_{BER868}	Input sensitivity at BER = 10^{-3} for 868 MHz operation, continuous data, without FEC	FSK, h = 0.5, 100 kbps		−106		dBm
		FSK, h = 0.5, 10 kbps		−116		
		FSK, 500 Hz deviation, 1.2 kbps		−126		
		PSK, 100 kbps		−109		
		PSK, 10 kbps		−120		
		PSK, 1 kbps		−130		
$IS_{BER868FEC}$	Input sensitivity at BER = 10^{-3}, for 868 MHz operation, continuous data, with FEC	FSK, h = 0.5, 50 kbps		−111		dBm
		FSK, h = 0.5, 5 kbps		−122		
		FSK, 0.1 kbps		−137		
IS_{PER868}	Input sensitivity at PER = 1%, for 868 MHz operation, 144 bit packet data, without FEC	FSK, h = 0.5, 100 kbps		−103		dBm
		FSK, h = 0.5, 10 kbps		−115		
		FSK, 500 Hz deviation, 1.2 kbps		−125		
IS_{WOR868}	Input sensitivity at PER = 1% for 868 MHz operation, WOR−mode, without FEC	FSK, h= 0.5, 100 kpbs		−102		dBm
		FSK		10		
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		−35		dBm
RSSIR	RSSI control range	FSK, 500 Hz deviation, 1.2 kbps	−126		−46	dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AX5043_AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AX5043_AGCCOUNTER, AX5043_TRKAMPL		0.1		dB
$RSSIS_3$	RSSI step size	Behind digital channel filter; reading register AX5043_RSSI		1		dB
SEL_{868}	Adjacent channel suppression	25 kHz channels , Note 1		45		dB
		100 kHz channels, Note 1		47		
BLK_{868}	Blocking at ± 10 MHz offset	Note 2		78		dB
R_{AFC}	AFC pull−in range	The AFC pull−in range can be programmed with the AX5043_MAXRFOFFSET registers. The AFC response time can be programmed with the AX5043_FREQGAIND register.	± 15			%
R_{DROFF}	Bitrate offset pull−in range	The bitrate pull−in range can be programmed with the AX5043_MAXDROFFSET registers.	± 10			%

1. Interferer/Channel @ BER = 10^{-3}, channel level is +3 dB above the typical sensitivity, the interfering signal is CW; channel signal is modulated with shaping
2. Channel/Blocker @ BER = 10^{-3}, channel level is +3 dB above the typical sensitivity, the blocker signal is CW; channel signal is modulated with shaping

Table 43. RECEIVER AND TRANSMITTER SETTLING PHASES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{xtal}	XTAL settling time	Powermodes: POWERDOWN to STANDBY Note that T_{xtal} depends on the specific crystal used.		0.5		ms
T_{synth}	Synthesizer settling time	Powermodes: STANDBY to SYNTHTX or SYNTHRX		40		μs
T_{tx}	TX settling time	Powermodes: SYNTHTX to FULLTX T_{tx} is the time used for power ramping, this can be programmed to be 1 x t_{bit}, 2 x t_{bit}, 4 x t_{bit} or 8 x t_{bit}. Note 1	0	1 x t_{bit}	8 x t_{bit}	μs
T_{rx_init}	RX initialization time			150		μs
T_{rx_rssi}	RX RSSI acquisition time (after T_{rx_init})	Powermodes: SYNTHRX to FULLRX Modulation (G)FSK Note 1		80 + 3 x t_{bit}		μs
$T_{rx\_preamble}$	RX signal acquisition time to valid data RX at full sensitivity/selectivity (after T_{rx_init})			9 x t_{bit}		

1. t_{bit} depends on the datarate, e.g. for 10 kbps t_{bit} = 100 μs

Table 44. OVERALL STATE TRANSITION TIMES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{tx_on}	TX startup time	Powermodes: STANDBY to FULLTX Note 1	40	40 + 1 x t_{bit}		μs
T_{rx_on}	RX startup time	Powermodes: STANDBY to FULLRX		190		μs
T_{rx_rssi}	RX startup time to valid RSSI	Powermodes: STANDBY to FULLRX Modulation (G)FSK Note 1		270 + 3 x t_{bit}		μs
T_{rx_data}	RX startup time to valid data at full sensitivity/selectivity			190 + 9 x t_{bit}		μs
T_{rxtx}	RX to TX switching	Powermodes: FULLRX to FULLTX		62		μs
T_{txrx}	TX to RX switching (to preamble start)	Powermodes: FULLTX to FULLRX		200		
T_{hop}	Frequency hop	Switch between frequency defined in register AX5043_FREQA and AX5043_FREQB		30		μs

1. t_{bit} depends on the datarate, e.g. for 10 kbps t_{bit} = 100 μs

CIRCUIT DESCRIPTION

The AXM0F243 is a true single chip narrow−band, ultra−low power RF−microcontroller SoC for use in licensed and unlicensed bands ranging from 27 MHz to 1050 MHz. The on−chip transceiver consists of a fully integrated RF front−end with modulator and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication.

The AXM0F243 contains a high speed Arm® Cortex®−M0+ Microcontroller. It contains 64 kBytes of FLASH and 8 kBytes of internal SRAM.

The AXM0F243 features two opamps, 12−bit 1−Msps SAR ADC with differential and single−ended modes, single−slope 10−bit ADC function, two current DACs (IDACs) for general−purpose applications on any pin, two low−power comparators that operate in Deep Sleep low−power mode, programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs, two independent run−time reconfigurable Serial Communication Blocks (SCBs) with re−configurable I2C, SPI, or UART functionality, five 16−bit timer/counter/pulse−width modulator (TCPWM) blocks, up to 20 Programmable GPIO Pins, a temperature sensor.

While the radio carrier/LO synthesizer can only be clocked by the crystal oscillator (carrier stability requirements dictate a high stability reference clock in the MHz range), the microcontroller and its peripherals provide extremely flexible clocking options. The system clock that clocks the microcontroller, as well as peripheral clocks, can be selected from one of the following clock sources: the crystal oscillator, the internal main oscillator (IMO) with default frequency of 24 MHz, internal low−frequency oscillator (ILO) of 40 kHz, a 32 kHz Watch Crystal Oscillator (WCO). Clock dividers are provided to generate clocks for peripherals on a fine−grained basis.

AXM0F243 can be operated from a 1.8 V to 3.6 V power supply over a temperature range of –40°C to 85°C, it consumes 5 − 55 mA for transmitting, depending on the output power and frequency, 6.8 – 11 mA for receiving.

The AXM0F243 features make it an ideal interface for integration into various battery powered solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220−1 and the US Federal Communications Commission (FCC) standard Title 47 CFR part 15 as well as Part 90. Additionally AXM0F243 is suited for systems targeting compliance with Wireless M−Bus standard EN 13757−4:2005. Wireless M−Bus frame support (S, T, R) is built−in.

The AXM0F243 sends and receives data in frames. This standard operation mode is called Frame Mode. Pre and post ambles as well as checksums can be generated automatically.

AXM0F243 supports any data rate from 0.1 kbps to 125 kbps for FSK, MSK, 4−FSK, GFSK, GMSK and ASK modulations. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AXM0F243 are necessary, they are outlined in the following, for details see the AXSEM RadioLab software which calculates the necessary register settings and the AX5043 Programming Manual.

The receiver supports multi−channel operation for all data rates and modulation schemes.

MICROCONTROLLER

CPU and Memory Subsystem

CPU

The Cortex−M0+ CPU in the AXM0F243 is part of the 32−bit MCU subsystem, which is optimized for low−power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb−2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two−wire form of JTAG. The debug configuration used for AXM0F243 has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The AXM0F243 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low−power flash block is designed to deliver two wait−state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single−cycle SRAM access performance on average.

SRAM

Eight KB of SRAM are provided with zero wait−state access at 48 MHz.

System Resources

Power System

The power system is described in detail in the section “Power”. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power−on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown−out detection). The AXM0F243 operates with a single external supply over the range of 1.8 to 3.6 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The AXM0F243 provides Active, Sleep, and Deep Sleep low−power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock−gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake−up on a wake−up event. In Deep Sleep mode, the high−speed clock and associated circuitry is switched off; wake−up from this mode takes 35 μs. The opamps can remain operational in Deep Sleep mode.

Clock System

The AXM0F243 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the AXM0F243 consists of the internal main oscillator (IMO), internal low−frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine−grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

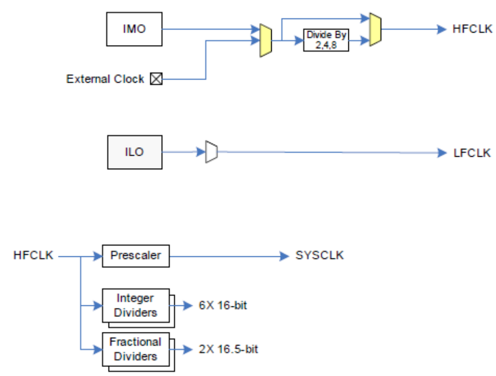


Figure 5. AXM0F243 MCU Clocking Architecture

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the AXM0F243; two of those are fractional dividers. The 16−bit capability allows flexible generation of fine−grained frequency values.

The IMO is the primary source of internal clocking in the AXM0F243. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power, nominally 40−kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode.

Watch Crystal Oscillator (WCO)

The AXM0F243 clock subsystem also implements a low−frequency (32−kHz watch crystal) oscillator that can be used for precision timing applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

Reset

The AXM0F243 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull−up resistor that is always enabled.

Analog Blocks

12−bit SAR ADC

The 12−bit, 1−Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12−bit conversion.

The Sample−and−Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is not available in Deep Sleep mode as it requires a high−speed clock (up to 18 MHz). The SAR operating range is 1.8 V to 3.6 V.

Two Opamps (Continuous−Time Block; CTB)

The AXM0F243 has two opamps with Comparator modes which allow most common analog functions to be performed on−chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans−Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on−chip opamps are designed with enough bandwidth to drive the Sample−and−Hold circuit of the ADC without requiring external buffering.

Low−power Comparators (LPC)

The AXM0F243 has a pair of low−power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low−power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake−up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

The AXM0F243 has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

The AXM0F243 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware−programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

The Programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16−bit counter with user−programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto−reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead−band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over−current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the AXM0F243.

Serial Communication Block (SCB)

The AXM0F243 has three serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I^2C Mode: The hardware I^2C block implements a full multi−master and slave interface (it is capable of multi−master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the AXM0F243 and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8−deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard−mode and Fast−mode devices as defined in the NXP I^2C−bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open−drain modes.

The AXM0F243 is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot−swapped or powered up independently of the rest of the I^2C system.

UART Mode: This is a full−feature UART operating at up to 1 Mbps. It supports automotive single−wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9−bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8−deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half−duplex form of SPI). The SPI block can use the FIFO.

GPIO

The AXM0F243 has up to 20 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull−up with strong pull−down
  - Strong pull−up with weak pull−down
  - Open drain with strong pull−down
  - Open drain with strong pull−up
  - Strong pull−up with strong pull−down
  - Weak pull−up with weak pull−down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports. During power−on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn−on current. A multiplexing network known as a high−speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for AXM0F243).

Power

The power system has a voltage regulator in active mode for the digital circuitry.

The supply voltage range is 1.8 V to 3.6 V (unregulated externally; internal regulator operational).

The AXM0F243 is powered by an external power supply that can be anywhere in the range of 1.8 to 3.6 V. This range is also designed for battery−powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V, the internal regulator supplies the internal logic.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1−μF range, in parallel with a smaller capacitor (0.1 μF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

TRANSCEIVER

The transceiver block is controllable through its registers. The transceiver block features its own 256 byte FIFO. The microcontroller can be interrupted at a programmable FIFO fill level.

RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 μs depending on the settings (see section AC Characteristics). Fast settling times mean fast start−up and fast RX/TX switching, which enables low−power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power−amplifier.

The frequency must be programmed to the desired carrier frequency.

The synthesizer loop bandwidth can be programmed, this serves three purposes:

1. Start−up time optimization, start−up is faster for higher synthesizer loop bandwidths
2. TX spectrum optimization, phase−noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths
3. Adaptation of the bandwidth to the data−rate. For transmission of FSK and MSK it is required that the synthesizer bandwidth must be in the order of the data−rate.

VCO

An on−chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the AX5043_FREQ registers. For operation in the 433 MHz band, the RFDIV bit in the AX5043_PLLVCODIV register must be programmed.

The fully integrated VCO allows to operate the device in the frequency ranges 800 – 1050 MHz and 400 – 520 MHz.

The carrier frequency range can be extended to 54 – 525 MHz and 27 – 262 MHz by using an appropriate external inductor between device pins L1 and L2. The bits VCO2INT and VCOSEL in the AX5043_PLLVCODIV register must be set high to enter this mode.

It is also possible to use a fully external VCO by setting bits VCO2INT = 0 and VCOSEL = 1 in the AX5043_PLLVCODIV register. A differential input at a frequency of double the desired RF frequency must be input at device pins L1 and L2. The control voltage for the VCO can be output at device pin FILT when using external filter mode. The voltage range of this output pin is 0 – 1.8 V. This mode of operation is recommended for special applications where the phase noise requirements are not met when using the fully internal VCO or the internal VCO with external inductor.

VCO Auto−Ranging

The AXM0F243 has an integrated auto−ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power−up. The function is initiated by setting the RNG_START bit in the AX5043_PLLRANGINGA or AX5043_PLLRANGINGB register. The bit is readable and a 0 indicates the end of the ranging process. Setting RNG_START in the AX5043_PLLRANGINGA register ranges the frequency in AX5043_FREQA, while setting RNG_START in the AX5043_PLLRANGINGB register ranges the frequency in AX5043_FREQB. The RNGERR bit indicates the correct execution of the auto−ranging. VCO auto−ranging works with the fully integrated VCO and with the internal VCO with external inductor.

Loop Filter and Charge Pump

The AXM0F243 internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The internal loop−filter has three configurations that can be programmed via the register bits FLT[1:0] in registers AX5043_PLLLOOP or AX5043_PLLLOOPBOOST the charge pump current can be programmed using register bits PLLCPI[7:0] in registers AX5043_PLLCPI or AX5043_PLLCPIBOOST. Synthesizer bandwidths are typically 50 – 500 kHz depending on the AX5043_PLLLOOP or AX5043_PLLLOOPBOOST settings, for details see the section: AC Characteristics.

The AXM0F243 can be setup in such a way that when the synthesizer is started, the settings in the registers AX5043_PLLLOOPBOOST and AX5043_PLLCPIBOOST are applied first for a programmable duration before reverting to the settings in AX5043_PLLLOOP and AX5043_PLLCPI. This feature enables automated fastest start−up.

Setting bits FLT[1:0] = 00 bypasses the internal loop filter and the VCO control voltage is output to an external loop filter at pin FILT. This mode of operation is recommended for achieving lower bandwidths than with the internal loop filter and for usage with a fully external VCO.

Registers

Table 45. RF FREQUENCY GENERATION REGISTERS

Register	Bits	Purpose
AX5043_PLLLOOP AX5043_PLLLOOPBOOST	FLT[1:0]	Synthesizer loop filter bandwidth and selection of external loop filter, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
AX5043_PLLCPI AX5043_PLLCPIBOOST		Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase−noise) for low data−rate transmissions.
AX5043_PLLVCODIV	REFDIV	Sets the synthesizer reference divider ratio.
	RFDIV	Sets the synthesizer output divider ratio.
	VCOSEL	Selects either the internal or the external VCO
	VCO2INT	Selects either the internal VCO inductor or an external inductor between pins L1 and L2
AX5043_FREQA, AX5043_FREQB		Programming of the carrier frequency
AX5043_PLLRANGINGA, AX5043_PLLRANGINGB		Initiate VCO auto−ranging and check results

RF Input and Output Stage (ANTP/ANTN/ANTP1)

The AXM0F243 has two main antenna interface modes:

1. Both RX and TX use differential pins ANTP and ANTN. RX/TX switching is handled internally. This mode is recommended for highest output powers, highest sensitivities and for direct connection to dipole antennas. Also see Figure 10.
2. RX uses the differential antenna pins ANTP and ANTN. TX uses the single ended antenna pin ANTP1. RX/TX switching is handled externally. This can be done either with an external RX/TX switch or with a direct tie configuration. This mode is recommended for low output powers at high efficiency Figure 13 and for usage with external power amplifiers Figure 12.

When antenna diversity is enabled, the radio controller will, when not in the middle of receiving a packet, periodically probe both antennas and select the antenna with the highest signal strength. The radio controller can be instructed to periodically write both RSSI values into the FIFO. Antenna diversity mode is fully automatic.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to GND must be provided at the antenna pins.

PA

In TX mode the PA drives the signal generated by the frequency generation subsystem out to either the differential antenna terminals or to the single ended antenna pin. The antenna terminals are chosen via the bits TXDIFF and TXSE in register AX5043_MODECFGA.

The output power of the PA is programmed via the register AX5043_TXPWRCOEFFB.

The PA can be digitally pre−distorted for high linearity.

The output amplitude can be shaped (raised cosine), this mode is selected with bit AMPLSHAPE in register AX5043_MODECFGA PA ramping is programmable in increments of the bit time and can be set to 1 – 8 bit times via bits SLOWRAMP in register AX5043_MODECFGA.

Output power as well as harmonic content will depend on the external impedance seen by the PA.

Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit−stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data−rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 995 Hz up to 221 kHz.

The AXSEM RadioLab Software calculates the necessary register settings for optimal performance. An overview of the registers involved is given in the following table as reference, for details see the AX5043 Programming Manual. The register setups typically must be done once at power−up of the device.

Registers

Table 46. CHANNEL FILTER AND DEMODULATOR REGISTERS

Register	Remarks
AX5043_DECIMATION	This register programs the bandwidth of the digital channel filter.
AX5043_RXDATARATE2… AX5043_RX-DATARATE0	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
AX5043_MAXDROFFSET2… AX5043_MAXDROFFSET0	These registers specify the maximum possible data rate offset
AX5043_MAXRFOFFSET2… AX5043_MAXR-FOFFSET0	These registers specify the maximum possible RF frequency offset
AX5043_TIMEGAIN, AX5043_DRGAIN	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal−to−noise ratio.
AX5043_MODULATION	This register selects the modulation to be used by the transmitter and the receiver, i.e. whether ASK, FSK should be used.
AX5043_PHASEGAIN, AX5043_FREQGAINA, AX5043_FREQGAINB, AX5043_FREQGAINC, AX5043_FREQGAIND, AX5043_AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops.
AX5043_AGCGAIN	This register controls the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit−rate, the faster the AGC loop should be.
AX5043_TXRATE	These registers control the bit rate of the transmitter.
AX5043_FSKDEV	These registers control the frequency deviation of the transmitter in FSK mode. The receiver does not explicitly need to know the frequency deviation, only the channel filter bandwidth has to be set wide enough for the complete modulation to pass.

Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit−stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform spectral shaping (also know as whitening). Spectral shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self synchronizing feedback shift register.

The encoder is programmed using the register AX5043_ENCODING, details and recommendations on usage are given in the AX5043 Programming Manual.

Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit−stream suitable for the modulator, and to extract packets from the continuous bit−stream arriving from the demodulator.

The Framing unit supports two different modes:

- Packet modes
- Raw modes

The microcontroller communicates with the framing unit through a 256 byte FIFO. Data in the FIFO is organized in Chunks. The chunk header encodes the length and what data is contained in the payload. Chunks may contain packet data, but also RSSI, Frequency offset, Timestamps, etc.

The AXM0F243 contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the microcontroller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Packet Modes

The AXM0F243 offers different packet modes. For arbitrary packet sizes HDLC is recommended since the flag and bit−stuffing mechanism. The AXM0F243 also offers packet modes with fixed packet length with a byte indicating the length of the packet.

In packet modes a CRC can be computed automatically.

HDLC Mode is the main framing mode of the AXM0F243. In this mode, the AXM0F243 performs automatic packet delimiting, and optional packet correctness check by inserting and checking a cyclic redundancy check (CRC) field.

NOTE: HDLC mode follows High−Level Data Link Control (HDLC, ISO 13239) protocol.

The packet structure is given in the following table.

Table 47. HDLC PACKET STRUCTURE

Flag	Address	Control	Information	FCS	(Optional Flag)
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In AXM0F243 the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC−CCITT, CRC−16 or CRC−32.

The receiver checks the CRC, the result can be retrieved from the FIFO, the CRC is appended to the received data.

In Wireless M−Bus Mode, the packet structure is given in the following table.

NOTE: Wireless M−Bus mode follows EN13757−4

Table 48. WIRELESS M−BUS PACKET STRUCTURE

Preamble	L	C	M	A	FCS	Optional Data Block (optionally repeated with FCS)	FCS
variable	8 bit	8 bit	8 bit	8 bit	16 bit	8 − 96 bit	16 bit

For details on implementing a HDLC communication as well as Wireless M−Bus please use the AXSEM RadioLab software and see the AX5043 Programming Manual.

Raw Modes

In Raw mode, the AXM0F243 does not perform any packet delimiting or byte synchronization. It simply serializes transmit bytes and de−serializes the received bit−stream and groups it into bytes. This mode is ideal for implementing legacy protocols in software.

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit−stream. When it detects the preamble, it aligns the de−serialization to it.

The preamble can be between 4 and 32 bits long.

RX AGC and RSSI

AXM0F243 features three receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register AX5043_AGCCOUNTER contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.625 dB. The value can be used as soon as the RF frequency generation sub−system has been programmed.
2. RSSI behind the digital IF channel filter.
   The register AX5043_RSSI contains the current value of the RSSI behind the digital IF channel filter. The step size of this RSSI is 1 dB.
3. RSSI behind the digital IF channel filter high accuracy. The demodulator also provides amplitude information in the AX5043_TRK_AMPLITUDE register. By combining both the AX5043_AGCCOUNTER and the AX5043_TRK_AMPLITUDE registers, a high resolution (better than 0.1 dB) RSSI value can be computed at the expense of a few arithmetic operations on the micro−controller. The AXSEM RadioLab Software calculates the necessary register settings for best performance.

Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA:

Table 49. MODULATIONS

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bitrate
ASK	PA off	PA on	BW = BITRATE	125 kBit/s
FSK/MSK/GFSK/GMSK	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	BW = (1 + h) ·BITRATE	125 kBit/s
PSK	$\Delta\Phi = 0°$	$\Delta\Phi = 180°$	BW = BITRATE	125 kBit/s

h = modulation index. It is the ratio of the deviation compared to the bit−rate; $f_{deviation} = 0.5 \cdot h \cdot BITRATE$, AXM0F243 can demodulate signals with h < 32.

ASK = amplitude shift keying

FSK = frequency shift keying

MSK= minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation} = 0.25 \cdot BITRATE$; the advantage of MSK over FSK is that it can be demodulated more robustly.

PSK = phase shift keying

All modulation schemes, except 4−FSK, are binary.

Amplitude can be shaped using a raised cosine waveform. Amplitude shaping will also be performed for constant amplitude modulation ((G)FSK, (G)MSK) for ramping up and down the PA. Amplitude shaping should always be enabled.

Frequency shaping can either be hard (FSK, MSK), or Gaussian (GMSK, GFSK), with selectable BT = 0.3 or BT = 0.5.

Table 50. 4−FSK MODULATION

Modulation	DiBit = 00	DiBit = 01	DiBit = 11	DiBit = 10	Main Lobe Bandwidth	Max. Bitrate
4−FSK	$\Delta f = -3f_{deviation}$	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	$\Delta f = +3f_{deviation}$	BW = (1 + 3 h) ·BITRATE	125 kBit/s

4−FSK Frequency shaping is always hard.

Automatic Frequency Control (AFC)

The AXM0F243 features an automatic frequency tracking loop which is capable of tracking the transmitter frequency within the RX filter band width. On top of that the AXM0F243 has a frequency tracking register AX5043_TRKRFFREQ to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{AX5043\_TRKRFFREQ}{2^{32}} f_{XTAL}$$

PWRMODE Register

The AXM0F243 transceiver features its own independent power management, independent from the microcontroller. While the microcontroller power mode is controlled through the PCON register, the AX5043_PWRMODE register controls which parts of the transceiver are operating.

Table 51. PWRMODE REGISTER

AX5043_PWRMODE Register	Name	Description
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltages are switched off to conserve leakage power. Register contents are preserved. Access to the FIFO is not possible and the contents are not preserved. POWERDOWN mode is only entered once the FIFO is empty.
0001	DEEPSLEEP	The transceiver is fully turned off. All digital and analog functions are disabled. All register contents are lost. To leave DEEPSLEEP mode the pin SEL has to be pulled low. This will initiate startup and reset of the transceiver. Then the MISO line should be polled, as it will be held low during initialization and will rise to high at the end of the initialization, when the chip becomes ready for operation. It is recommended to use the functions ax5043_enter_deepsleep() and ax5043_wakeup_deepsleep() provided in libmf
0101	STANDBY	The crystal oscillator and the reference are powered on; receiver and transmitter are off. Register contents are preserved and accessible. Access to the FIFO is not possible and the contents are not preserved. STANDBY is only entered once the FIFO is empty.
0110	FIFO	The reference is powered on. Register contents are preserved and accessible. Access to the FIFO is possible and the contents are preserved.

Table 51. PWRMODE REGISTER

AX5043_PWRMODE Register	Name	Description
1000	SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.
1001	FULLRX	Synthesizer and receiver are running.
1011	WOR	Receiver wakeup−on−radio mode. The mode the same as POWERDOWN, but the 640 Hz internal low power oscillator is running.
1100	SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.

Table 52. A TYPICAL AX5043_PWRMODE SEQUENCE FOR A TRANSMIT SESSION

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	FULLTX	Data transmission
4	POWERDOWN	

Table 53. A TYPICAL AX5043_PWRMODE SEQUENCE FOR A RECEIVE SESSION

Step	PWRMODE [3:0]	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	FULLRX	Data reception
4	POWERDOWN	

Voltage Regulator

The AXM0F243 transceiver uses its own dedicated on−chip voltage regulator system to create stable supply voltages for the internal circuitry from the primary supply VDD_IO. The I/O level of the digital pins is VDD_IO.

Pins VDD_ANA are supplied for external decoupling of the power supply used for the on−chip PA.

The voltage regulator system must be set into the appropriate state before receive or transmit operations can be initiated. This is handled automatically when programming the device modes via the AX5043_PWRMODE register.

Register AX5043_POWSTAT contains status bits that can be read to check if the regulated voltages are ready (bit SVIO) or if VDD_IO has dropped below the brown−out level of 1.3 V (bit SSUM).

In power−down mode the core supply voltages for digital and analog functions are switched off to minimize leakage power. Most register contents are preserved but access to the FIFO is not possible and FIFO contents are lost.

In deep−sleep mode all supply voltages are switched off. All digital and analog functions are disabled. All register contents are lost.

Typical Application Diagrams

Connecting to Debug Adapter

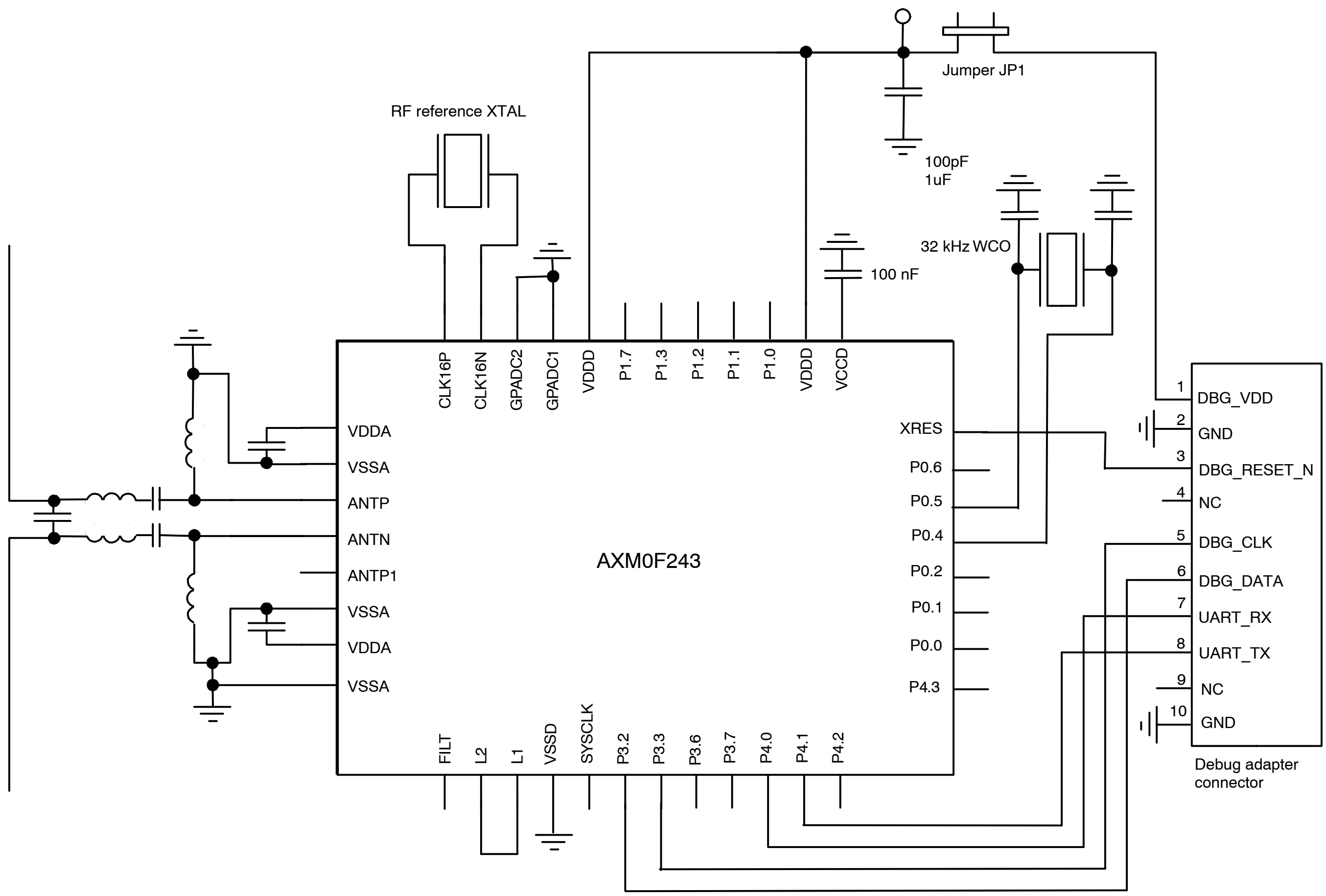


Figure 6. Typical Application Diagram with Connection to the Debug Adapter

Match to 50 Ω for Differential Antenna Pins (868 / 433 MHz RX / TX Operation)

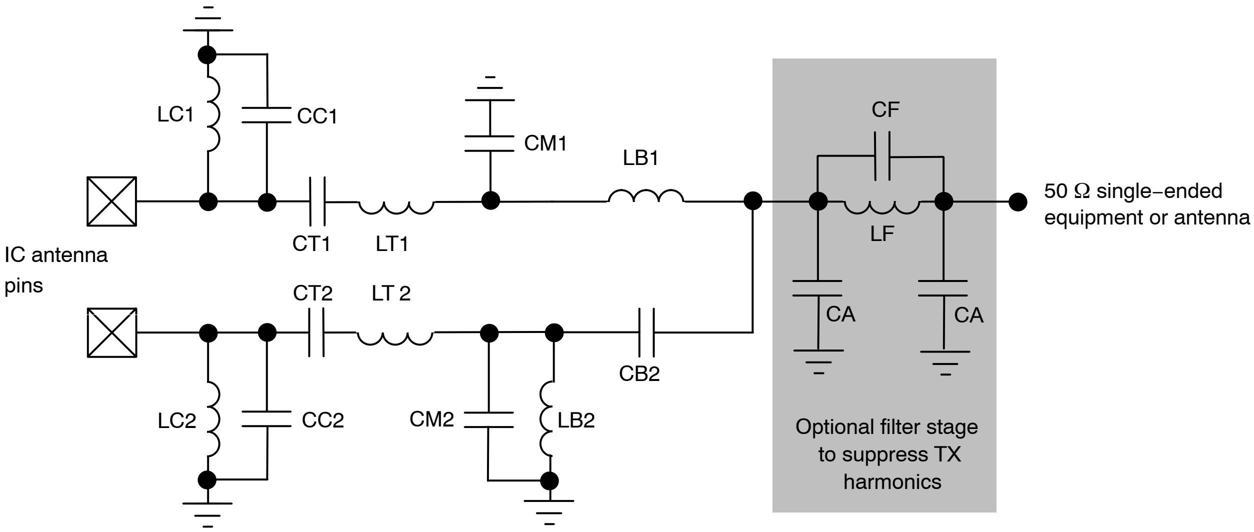


Figure 7. Structure of the Differential Antenna Interface for TX/RX Operation to 50 Ω Single−ended Equipment or Antenna

Table 54. TYPICAL COMPONENT VALUES

Frequency Band	LC1,2 [nH]	CC1,2 [pF]	CT1,2 [pF]	LT1,2 [nH]	CM1 [pF]	CM2 [pF]	LB1,2 [nH]	CB2 [pF]	CF [pF] optional	LF [nH] optional	CA [pF] optional
868 / 915 MHz	18	nc	2.7	18	6.2	3.6	12	2.7	nc	0 Ω	nc
433 MHz	100	nc	4.3	43	11	5.6	27	5.1	nc	0 Ω	nc
470 MHz	100	nc	3.9	33	4.7	nc	22	4.7	nc	0 Ω	nc
169 MHz	150	10	10	120	12	nc	68	12	6.8	30	27

Match to 50 Ω for Single−ended Antenna Pin (868 / 915 / 433 MHz TX Operation)

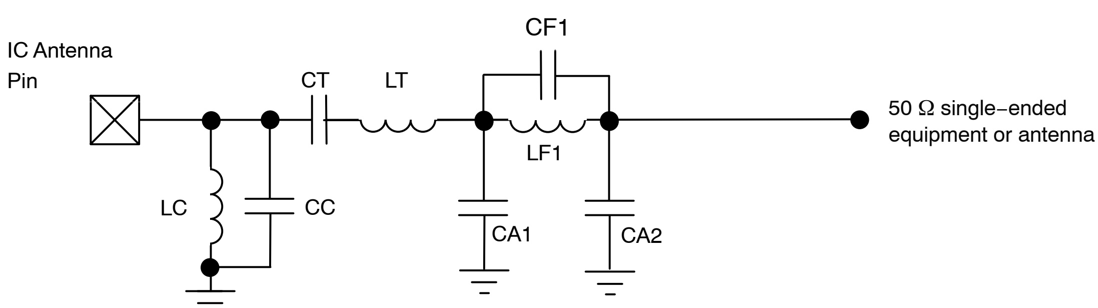


Figure 8. Structure of the Single−ended Antenna Interface for TX Operation to 50 Ω Single−ended Equipment or Antenna

Table 55. TYPICAL COMPONENT VALUES

Frequency Band	LC [nH]	CC [pF]	CT [pF]	LT [nH]	CF1 [pF]	LF1 [nH]	CA1 [pF]	CA2 [pF]
868 / 915 MHz	18	nc	2.7	18	3.6	2.2	3.6	nc
433 MHz	100	nc	4.3	43	6.8	4.7	5.6	nc

Match to 50 Ω for Single−ended Antenna Pin (169 MHz TX Operation)

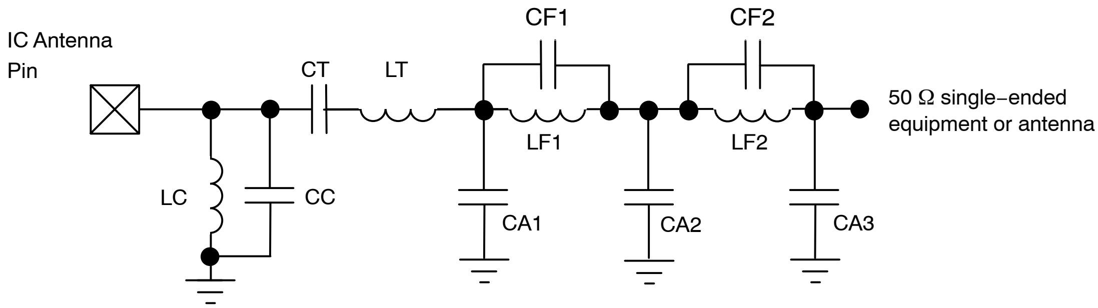


Figure 9. Structure of the Single−ended Antenna Interface for TX Operation to 50 Ω Single−ended Equipment or Antenna

Table 56. TYPICAL COMPONENT VALUES

Frequency Band	LC [nH]	CC [pF]	CT [pF]	LT [nH]	CF1 [pF]	LF1 [nH]	CF2 [pF]	LF2 [nH]	CA1 [pF]	CA2 [pF]	CA3 [pF]
169 MHz	150	2.2	22	120	4.7	39	1.8	47	33	47	15

Using a Dipole Antenna and the Internal TX/RX Switch

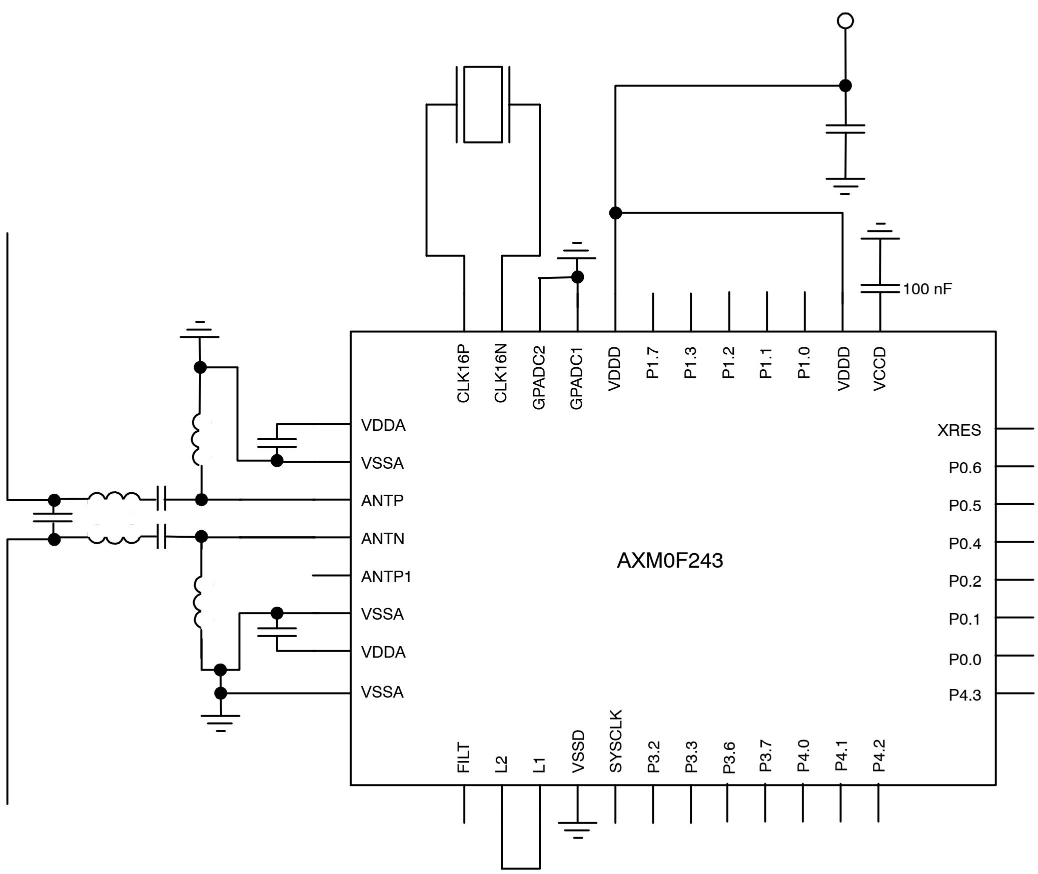


Figure 10. Typical Application Diagram with Dipole Antenna and Internal TX/RX Switch

Using a Single−ended Antenna and the Internal TX/RX Switch

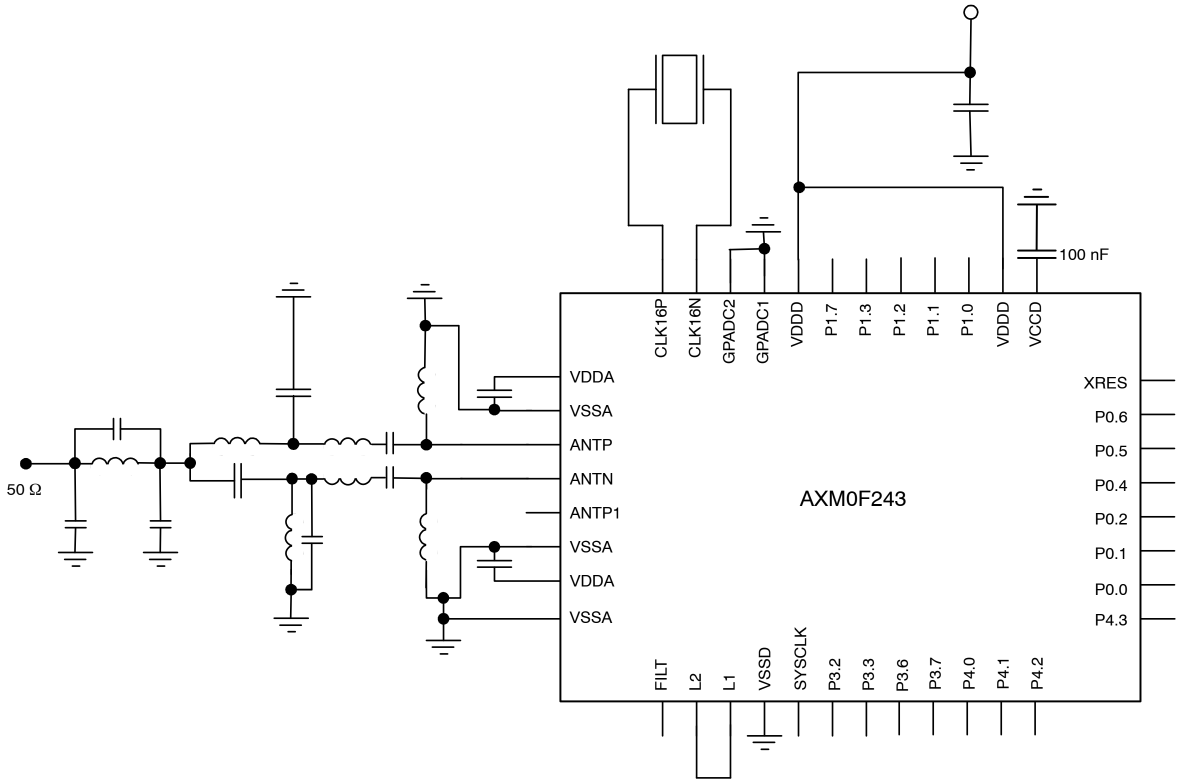


Figure 11. Typical Application Diagram with Single−ended Antenna and Internal TX/RX Switch

Using an External High−power PA and an External TX/RX Switch

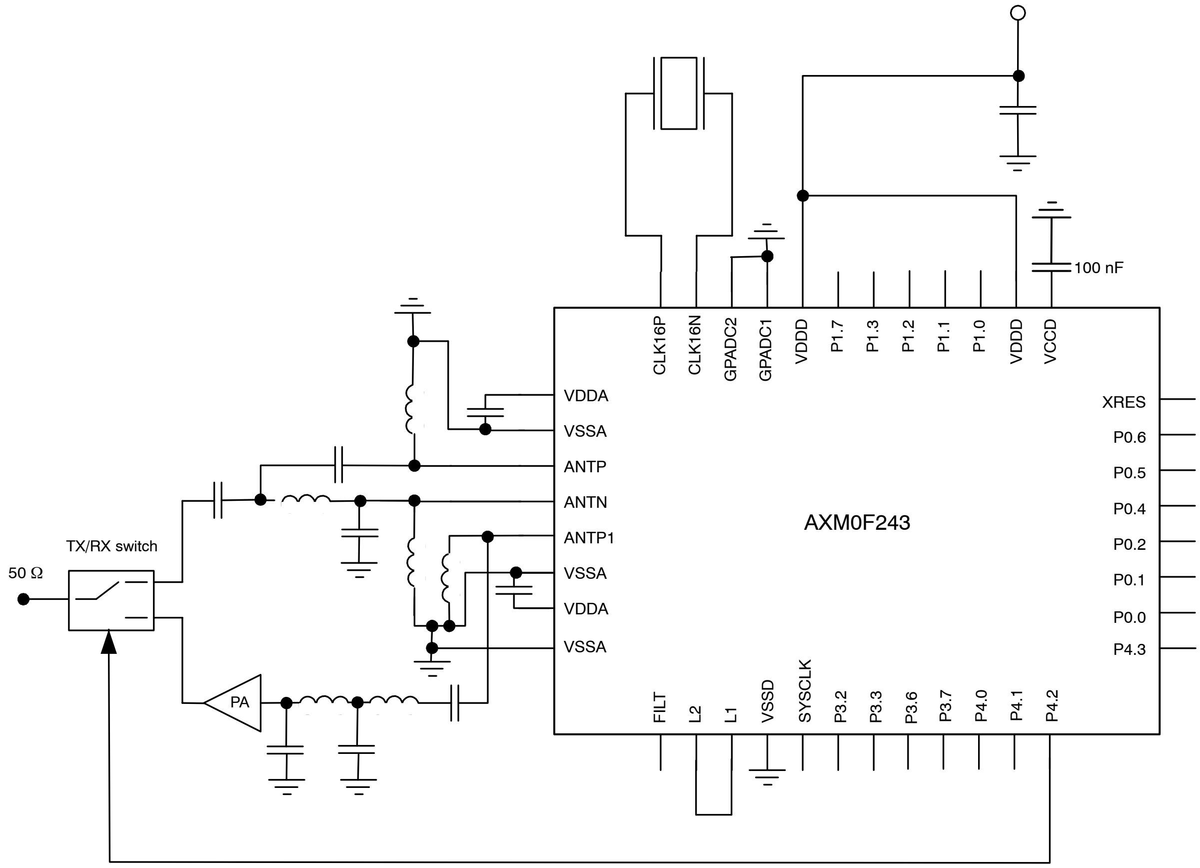


Figure 12. Typical Application Diagram with Single−ended Antenna, External PA and External Antenna Switch

Using the Single−ended PA

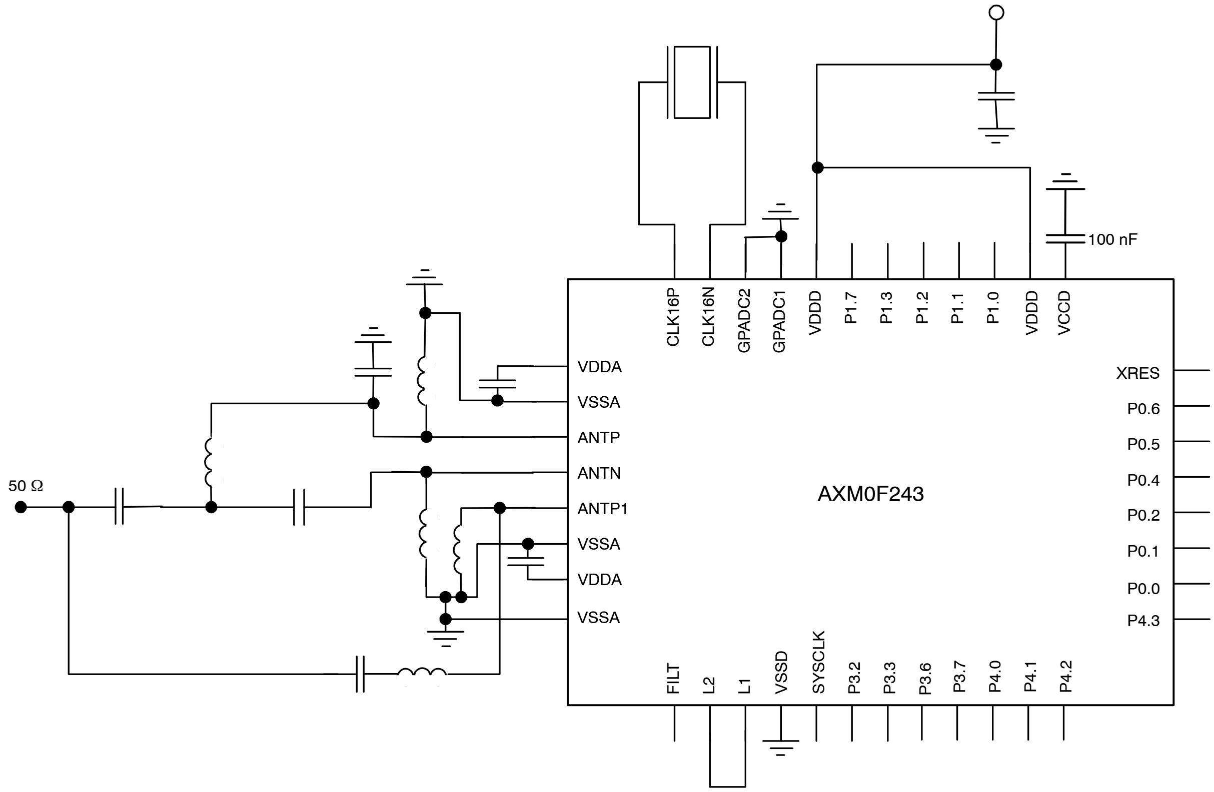


Figure 13. Typical Application Diagram with Single−ended Antenna, Single−ended Internal PA, without RX/TX Switch

Using Two Antenna

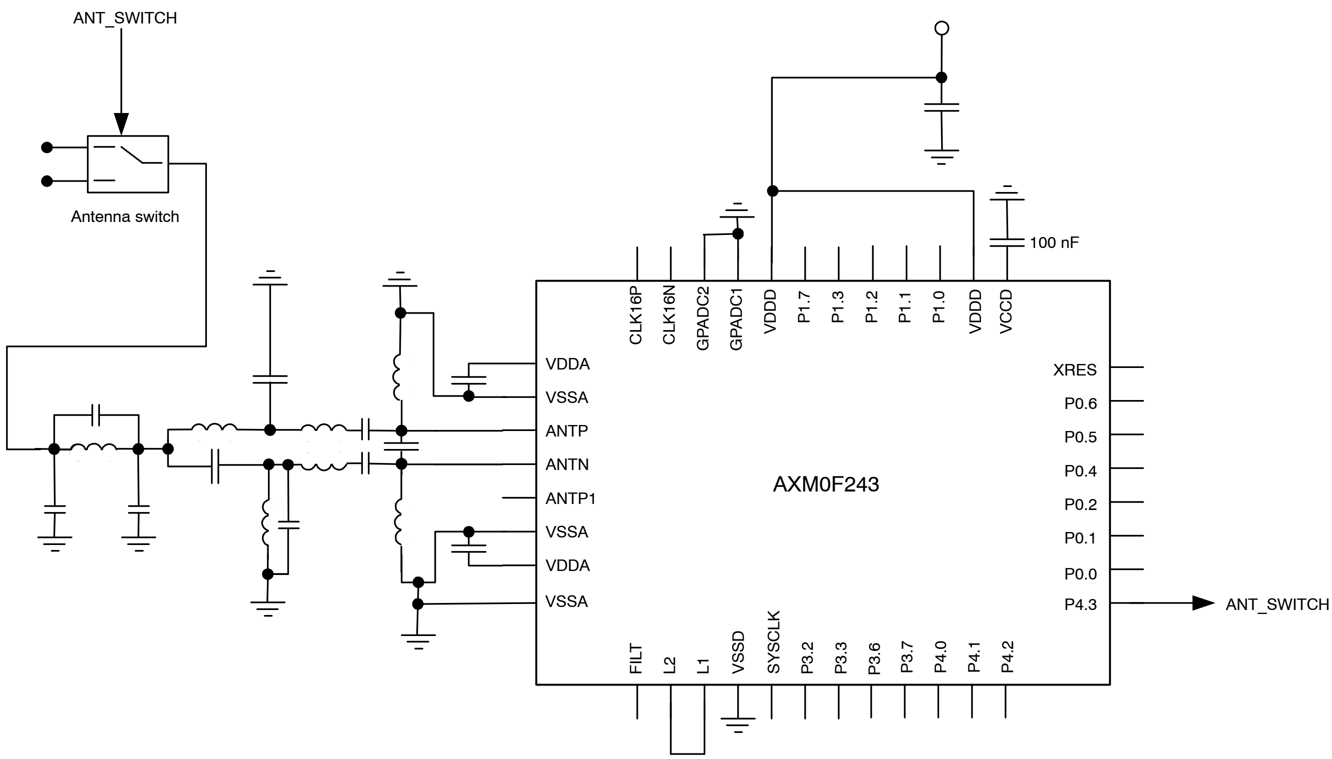


Figure 14. Typical Application Diagram with Two Single−ended Antenna and External Antenna Switch

Using an External VCO Inductor

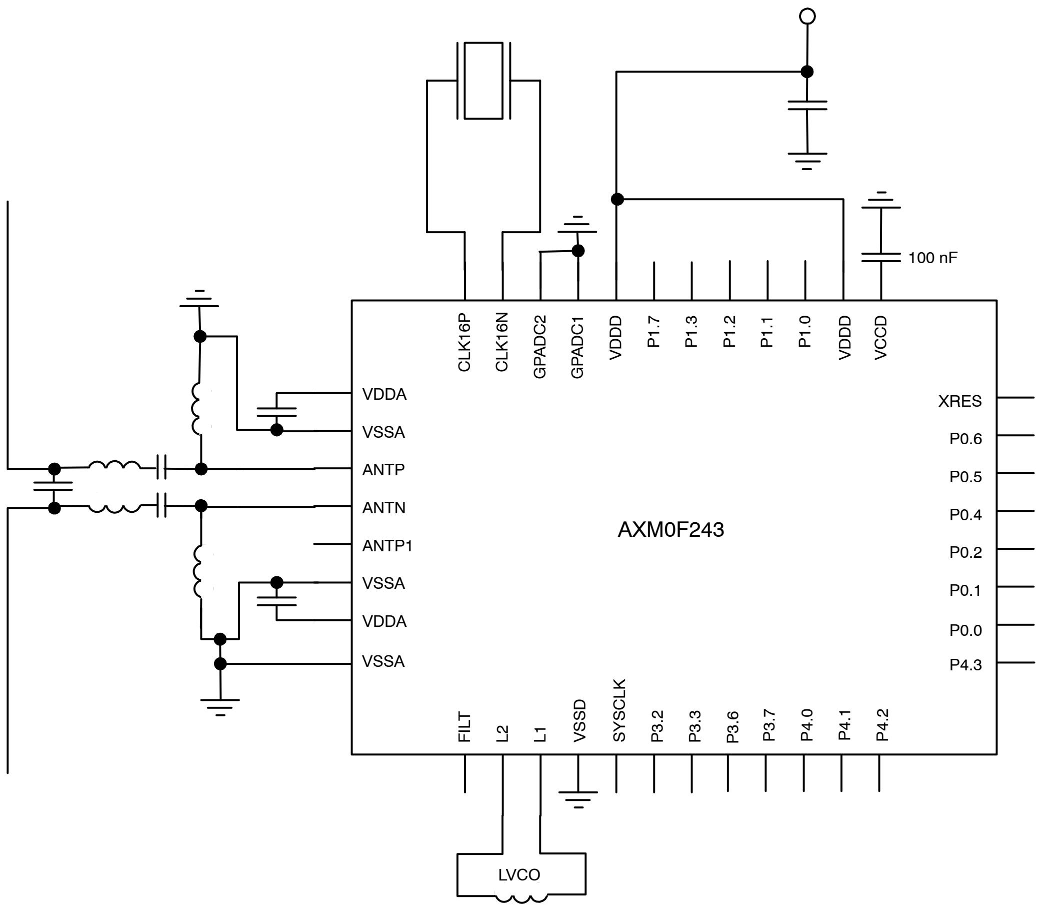


Figure 15. Typical Application Diagram with External VCO Inductor

Using an External VCO

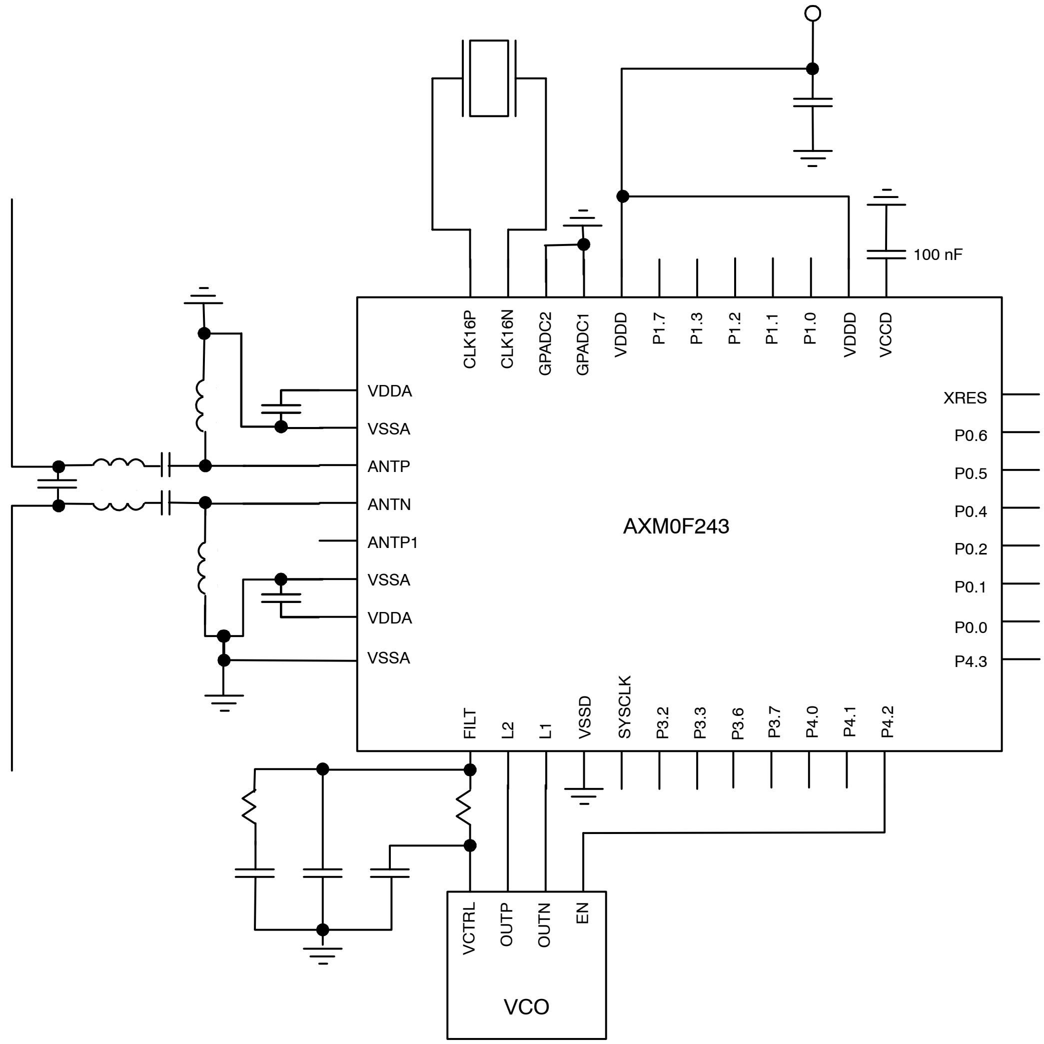


Figure 16. Typical Application Diagram with External VCO

Using a TCXO

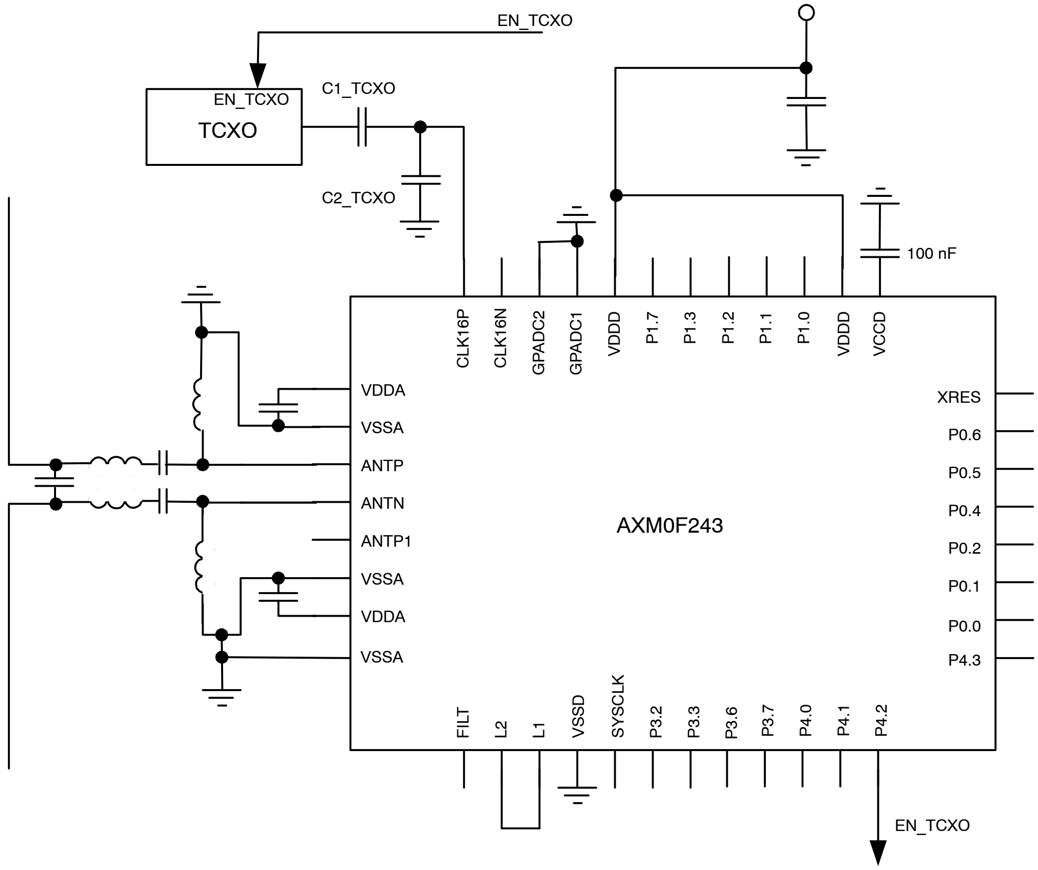


Figure 17. Typical Application Diagram with a TCXO

NOTE: For detailed TCXO network recommendations depending on TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock.

QFN40 Soldering Profile

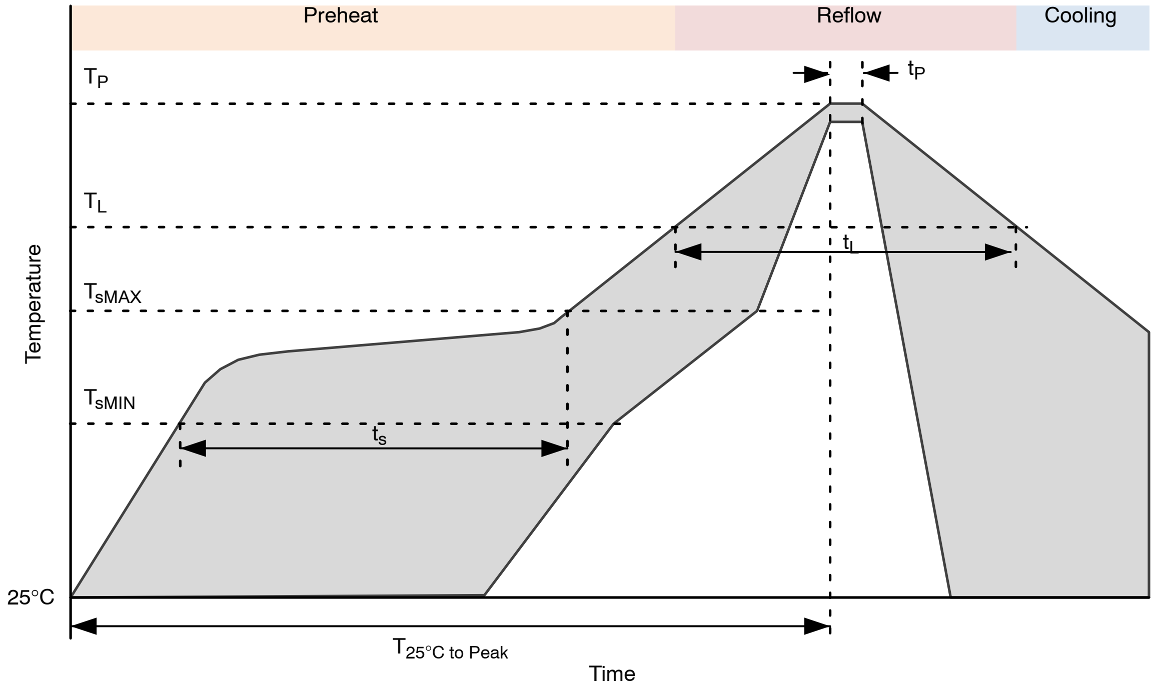


Figure 18. QFN40 Soldering Profile

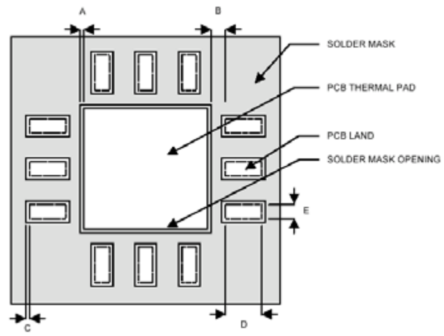
Table 57.

Profile Feature		Pb−Free Process
Average Ramp−Up Rate		3°C/s max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 – 180 sec
Time 25°C to Peak Temperature	$T_{25°C\ to\ Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 – 150 s
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 – 40 s
Cooling Phase		
Ramp−down rate		6°C/s max.

1. All temperatures refer to the top side of the package, measured on the the package body surface.

QFN40 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 19.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
D = PCB land length = QFN solder pad length + 0.1 mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 19. PCB Land and Solder Mask Recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 20.
4. The aperture opening for the signal pads should be between 50−80% of the QFN pad area as shown in Figure 21.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No−clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water−soluble flux is used.

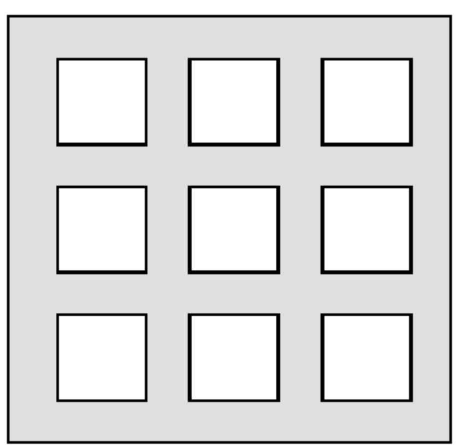


Figure 20. Solder Paste Application on Exposed Pad

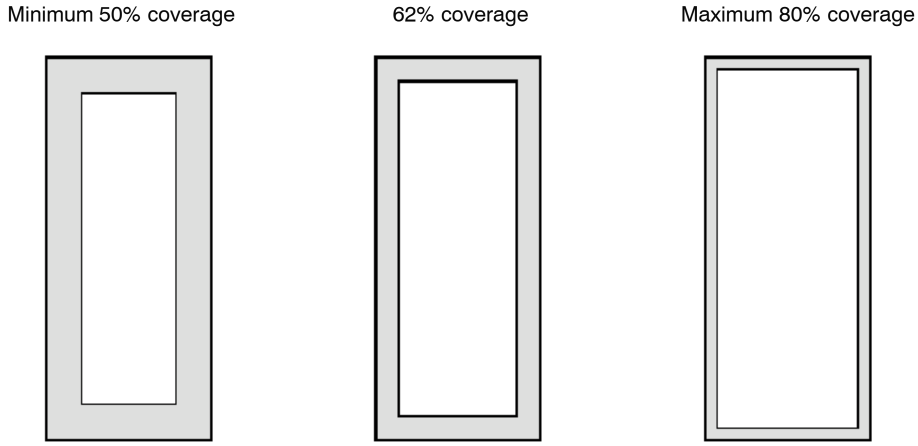
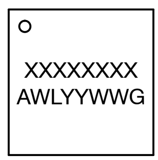


Figure 21. Solder Paste Application on Pins

MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

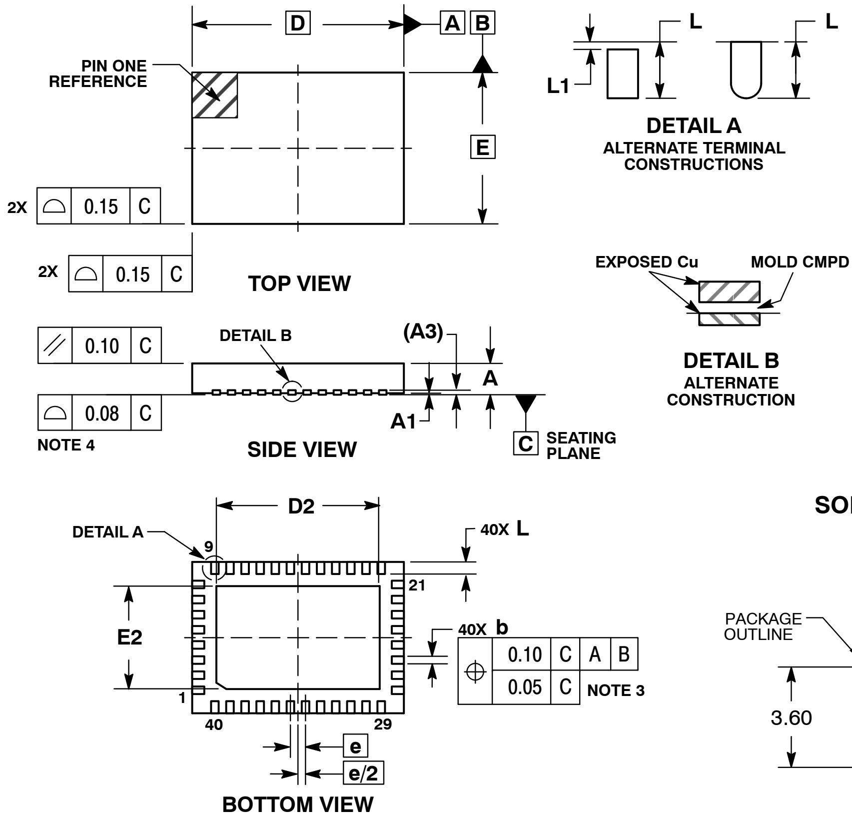
Table 58. ORDERING INFORMATION

Device	CM0P_CPUID	AX5043 Version	Package	OPN	Shipping†
AXM0F243−1	0x410CC601	1	QFN40 (Pb−Free, Halide Free)	AXM0F243−1−TX40	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

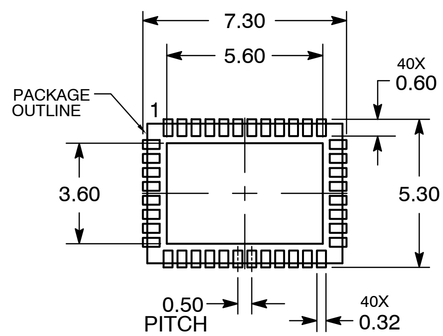
QFN40 7x5, 0.5P
CASE 485EG
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D2	5.30	5.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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For additional information, please contact your local Sales Representative