GENERAL DESCRIPTION

OB2004A is a high performance and highly integrated secondary side synchronous rectification controller used for secondary side rectification in switch mode power supply system. It drivers a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier at the secondary side of flyback converter, which can reduce heat dissipation, increases output current capability and efficiency, and simplify thermal design. It can support wide range of system output voltage 5V~12V.

It is suitable for multiple mode applications including discontinuous conduction mode (DCM), quasi-resonant mode (QR) and continuous conduction mode (CCM). Specially for CCM, to guarantee system reliability, innovative property prediction algorithm is used in SR turn-off control.

In addition, to balance reliability and efficiency, OB2004A generates a driving signal with optimized dead time with respect to the primary side PWM signal from the information on the secondary side of the isolation transformer with the help of innovative property dead time control algorithm.

The externally adjustable minimum on time and innovative property off time control effectively avoid the ring impact induced by parasitic elements so that a reliable and noise free operation of the SR system is insured.

OB2004A is offered in SOT23-6 package.

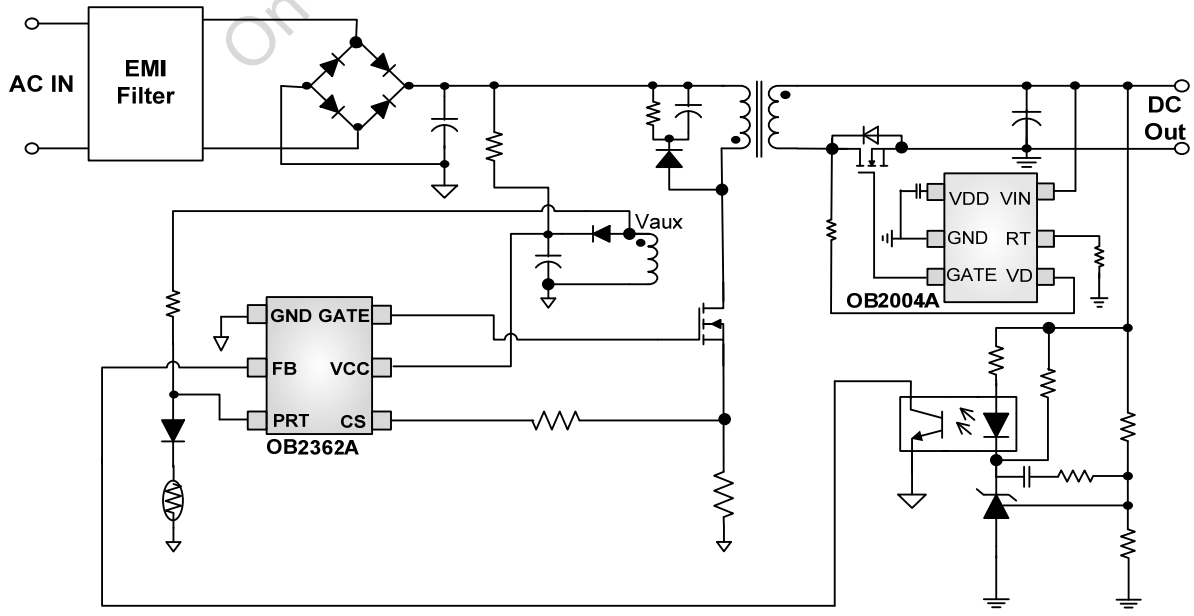
FEATURES

- Secondary-side synchronous rectification controller for 5V~12V output system
- Up to 85V VD pin high voltage tolerance
- Externally adjustable minimum on time
- Suitable for DCM, QR and CCM operation
- Prediction algorithm for CCM
- Accurate secondary side MOSFET Vds sensing
- SR turn on/off dead-time control for high efficiency and low thermal with immunity of interference
- Adaptive off time control effectively avoid the ring impact induced by parasitic elements
- 3A/2A peak current sink/source driver capability
- VDD UVLO protection

APPLICATIONS

- AC/DC 5V~12V adaptors
- Low voltage rectification circuits

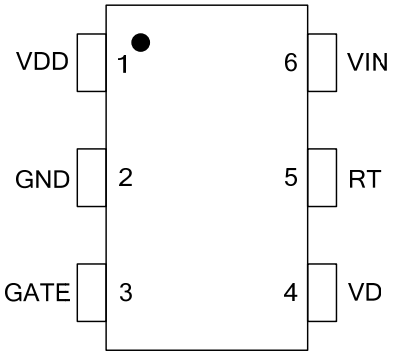
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2004A is offered in SOT23-6 package, shown as below.



Ordering Information

Part Number	Description
OB2004AMP	SOT23-6, Halogen-free in T&R

Package Dissipation Rating

Package	RθJA(℃/W)
SOT23-6	200

Absolute Maximum Ratings

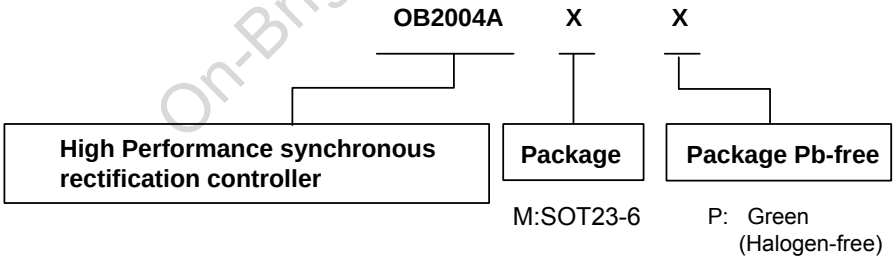
Parameter	Value
VIN pin	-0.6V to 24V
VDD pin	-0.6V to 8V
VD pin	-2.5V to 85V Note2
Gate pin	-0.6V to 8V
RT pin	-0.6V to 7V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Operating Ambient Temperature T_A	-20 to 85 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

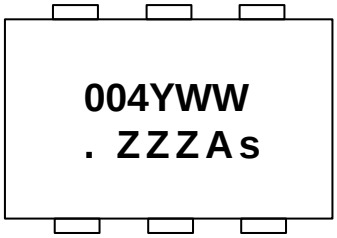
Note2: -2.5V applies to minimum duty cycle during normal operation only.

Recommended Operating Range

Symbol	Parameter	Min/Max
VDD	VDD Supply Voltage	5V to 7.5V



Marking Information

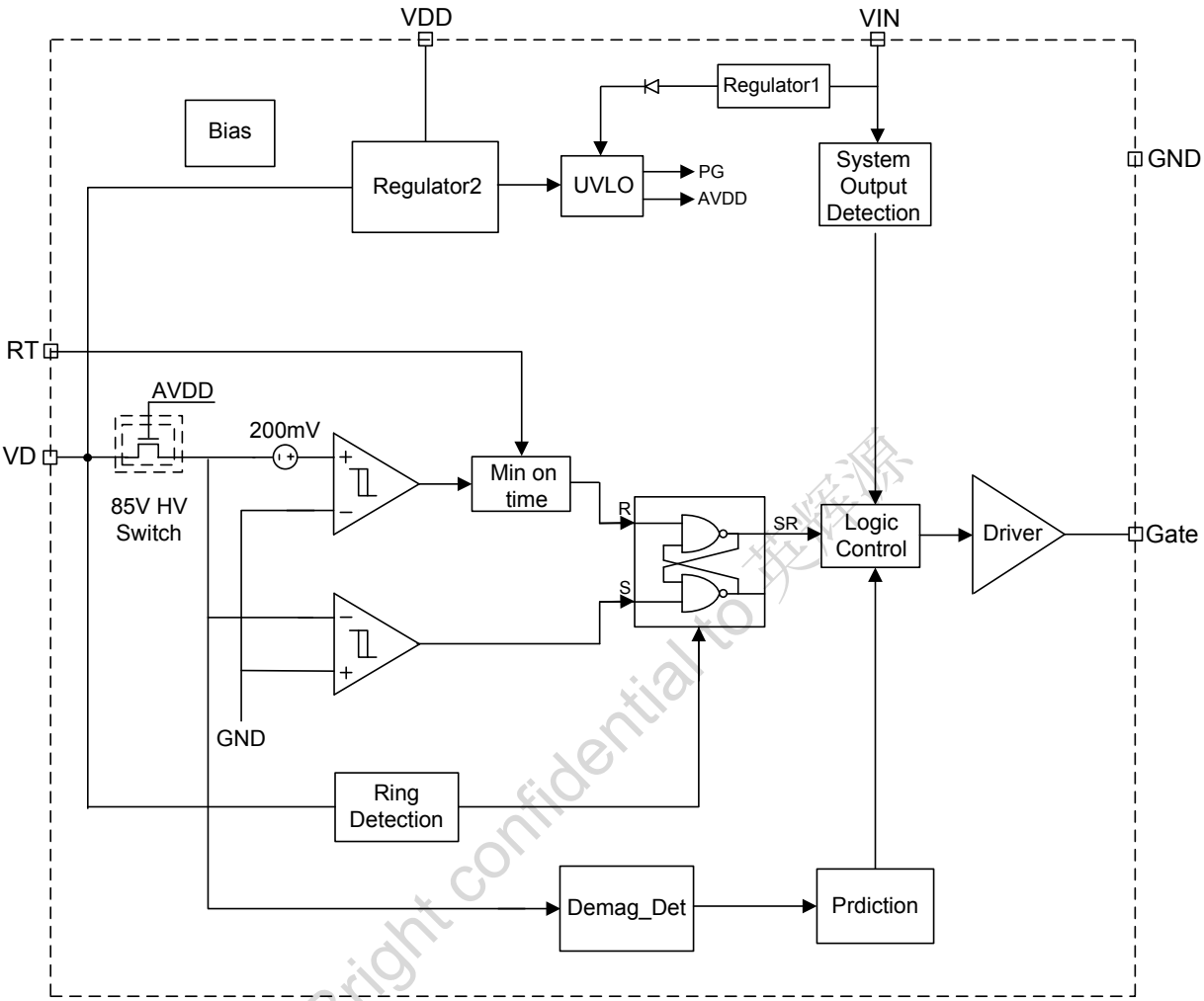


Y:Year Code
WW:Week Code(01-52)
ZZZ: Lot code
A:Character Code
s: Internal code

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
VD	I	This pin is connected to external n-channel MOSFET drain
Gate	O	Driver output for external N-channel MOSFET
GND	P	Ground
VDD	P	Power Supply
VIN	I	System output voltage detection
RT	O	Minimum on time control pin. A resistor is connected from this pin to GND

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

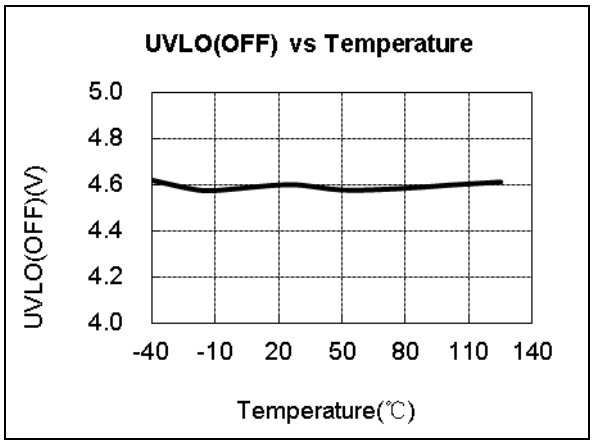
(T_A = 25℃, VDD=6.5V, unless otherwise noted)

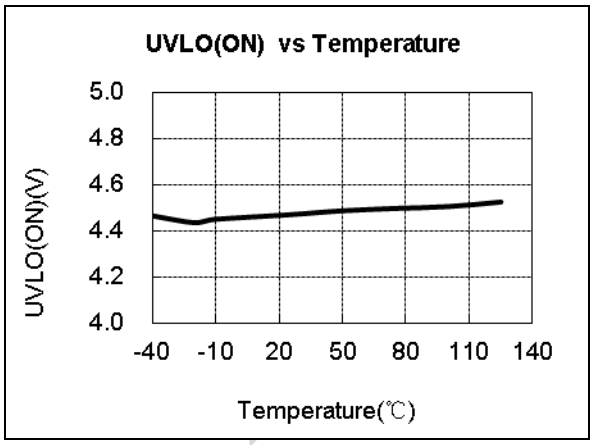
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
I_Vdd_operation	Operation current	Frequency@Vd=65KHz,VDD=5 V,1nF Cap load at GATE.		1.5	2.0	mA
		Frequency@Vd=2KHz,VDD=5V, No load at GATE.		0.8	1.0	mA
Vdd_regulation	Vdd regulation voltage	Frequency@Vd=50KHz, Duty=25%, High level @Vd=20V	6.3	6.5	6.7	V
UVLO(OFF)	VDD Under Voltage Lockout Entry		4.4	4.6	4.8	V
UVLO(ON)	VDD Under Voltage Lockout Exit (Recovery)		4.2	4.4	4.6	V
VD Detection Section						
Vth_SR_act	SR MOSFET turn on threshold voltage detection at VD		-150	-200	-250	mV
Vth_SR_deact	Adjustable SR MOSFET turn off threshold voltage detection at Vd, Which is 0.06*Rd mV, and Rd is the resistor connected to Vd. (Note2)	Rd=85 ohm		-5		mV
Tdelay_on	SR MOSFET fast path turn-on propagation delay			100		ns
	SR MOSFET slow path turn-on propagation delay			200		ns
Tdelay_off	SR MOSFET turn-off propagation delay			75		ns
T_minimum_on	SR MOSFET minimum on time	RT=25KΩ		1.9		us
Vin_sr_disable	Voltage level at VIN when SR is disable		2.2	2.5	2.8	V
CCM Prediction Section						
Rpre	Prediction ratio	No sub-harmonic condition	70	75	75	%
		With sub-harmonic condition	12	15	18	%
Tsr_on_max	Maximum SR turn-on time		35	40	45	us
RT Section						
Vrt	Voltage reference at RT pin		0.95	1	1.05	V
Dead-time Control Section						
Tdt_off_max	Maximum SR turn-off dead time			0.8		us
GATE driver Section						
VOH	Output high level @ VDD=6.5V		6			V
VOL	Output low level @ VDD=6.5V				1	V
Tf	Falling time	Gate voltage falling from 6V to 1V @ C_L=1nF		50		ns
Tr	Rising time	Gate voltage rising from 1V to 6V @ C_L=1nF		50		ns

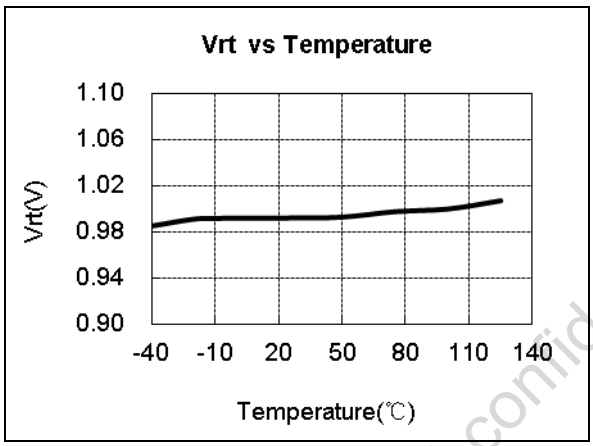
Note1：Suggesting primary side controller operating at 65kHz frequency

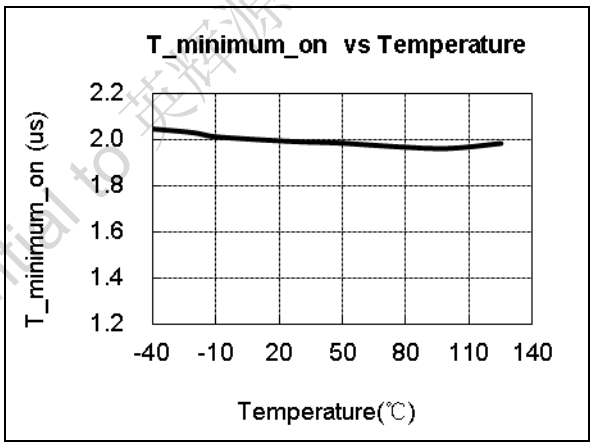
Note2： Rd can be choosed between 10~100 ohm

CHARACTERIZATION PLOTS









Operation Description

OB2004A is a high performance and highly integrated secondary side synchronous rectification controller in switch mode power supply system. It drivers a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier, which can reduce heat dissipation, increases output current capability and efficiency, and simplify the thermal design.

Startup and under voltage lockout (UVLO)

Whether OB2004 can operate normally or not depends on UVLO function implemented on chip and system output voltage. When power system is plugged in, VDD cap is charged from transformer secondary winding. When VDD rises above UVLO(off), the IC wakes up from under voltage lock out state and monitors the system output voltage through Vin pin. OB2004 will output SR gate based on correct timing after Vin rises above 2.7V(typical). Refer to the following timing diagram.

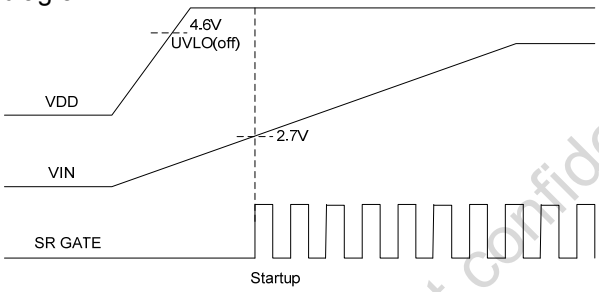


Fig.1 System start up timing diagram

With enough high Vin, OB2004 would be powered from VDD and system output (Vin), which can lead to better system efficiency. When VDD drops below UVLO(on), to guarantee thermal stability, as long as the primary side is in operation, the OB2004 still can work normally until the Vin is lower than 2.9V. Refer to the following timing diagram.

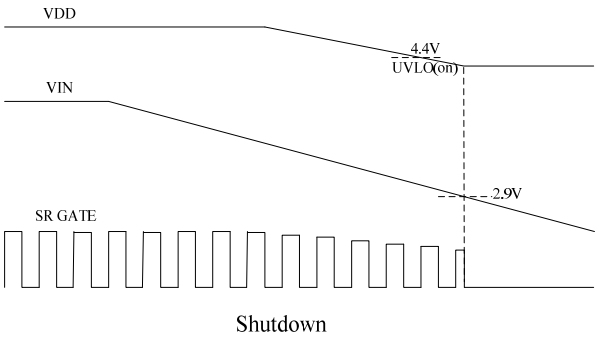


Fig.2 System shut down timing diagram

For system reliability, the SR gate would be pulled low when Vin is lower than 2.5V (typical) regardless of VDD. Refer to the following timing diagram.

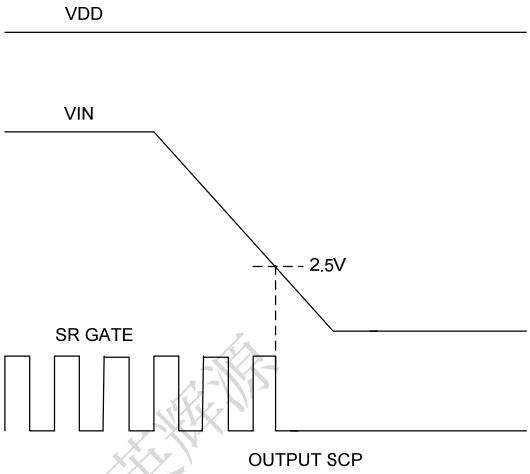


Fig.3 System output SCP timing diagram

Additionally, there is a pull down on-chip 15Kohm resistor to avoid the misconducting by VD pulse coupling. Besides, a hysteresis window between UVLO(off) and UVLO(on) makes system work reliably.

Synchronization rectifier

OB2004A controls the turn-on and turn-off of synchronization rectifier MOSFET (SR MOSFET) by detection of drain-source voltage and prediction control. When demagnetization of transformer starts, the secondary-side current will flow through the body diode of SR MOSFET and the voltage at the drain will drop to below -200mV (typical). As soon as OB2004A detects this negative voltage, the driver voltage is pulled high to turn on the SR MOSFET after variable delay time depending on input line voltage and loading condition, refer to Fig.4.This variable delay time can improve system immunity to noise.

After the SR MOSFET is turned on, the drain voltage of SR MOSFET begins to rise based on its Rdson and secondary-side current. The drain voltage becomes higher with demagnetization goes on. For reliable operation,OB2004 generate a adjustable SR turn-off threshold voltage based on resistor Rd on Vd pin， which is determined by 0.06*Rd mV. For DCM and QR, when the drain voltage rises above -5mV（Rd=85 ohm）, the gate of SR MOSFET will be pulled down to ground very quickly, refer to Fig.4. However, when the system works in CCM mode, the drain voltage may not rise above -5mV. In this situation, the property prediction algorithm would turn off SR

gate in advance. The details are described in CCM section.

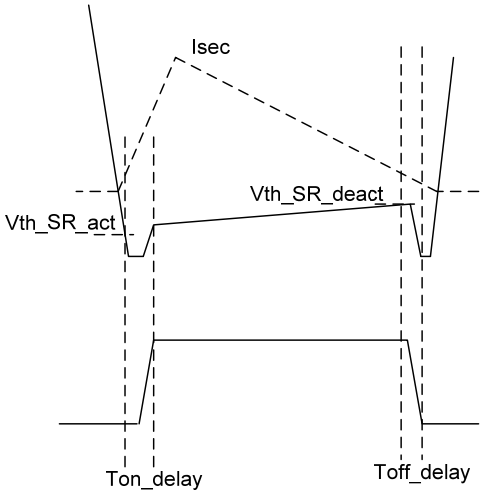


Fig.4 SR MOSFET turn-on and turn-off timing

Prediction control in CCM

When system works in CCM mode, drain voltage can not rise above -5mV when primary side turns on. In this case the property prediction algorithm implemented in OB2004A turns off the SR. OB2004A would detect the demagnetization time of current cycle and use this information to turn off SR in next cycle. For stable CCM, there is little variation between consecutive demagnetization phase, so the next cycle SR can be turn off predictively with pre-set prediction ratio, such as 75%. This means the next SR turn-on would last 75% of current demagnetization time before turn off. However when sub-harmonic switching happens, there is risk of short-circuit of transformer if both primary side and secondary side switch controllers are in turn-on phase. To avoid this risk, OB2004A would detect the primary side turn on time. If the primary side turn on time of current cycle is 600ns (typical) longer than the previous cycle, the pre-set prediction ratio would be changed from 75% to 15% so that the SR turn-on time is significantly reduced to avoid the risk of short-circuit of transformer. Fig.5 and Fig.6 illustrates the control scheme. In the next consecutive cycles, the SR on-time will be gradually increased that improve the efficiency.

In addition, a adaptive dead time control is implemented (described in next section). It regulates the time period (dead time) between the SR tune off instance and turn on instance of the primary side to be 1uS in stable CCM operation to further improve the efficiency while ensure the safe operation.

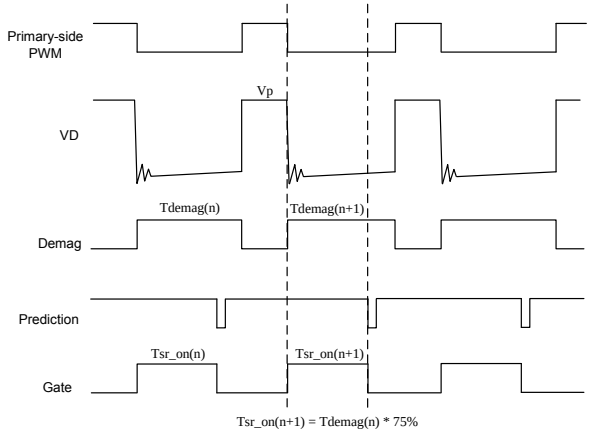


Fig.5 Prediction in stable CCM

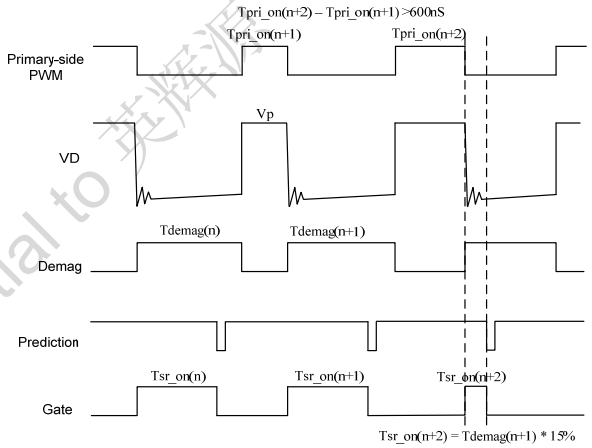


Fig.6 Prediction in CCM with sub-harmonic

Dead time control

For efficiency and thermal issue, the demagnetization current flowing through SR MOSFET body diode after SR turn off should be as small as possible, i.e the dead time between SR turn off and demagnetization ending is as short as possible. But when SR MOSFET Rdson is too small or interference riding on Vds, SR maybe turn off prematurely. In this case, an adaptive dead time control algorithm used in OB2004A can correct the dead time to 1uS (typical) for good efficiency and thermal performance.

Adjustable minimum on time

OB2004A offers adjustable minimum on time control. This timer can avoid effectively false turn-off due to high frequency interference caused by parasitic element at the start of secondary-side demagnetization.

Tonmin=8*RT*10E(-11)

Adaptive minimum off time

At the end of demagnetization, SR MOSFET will be turn off. The remaining current will flow through body diode again, which may result in negative voltage (about -700mV) appears at drain and SR

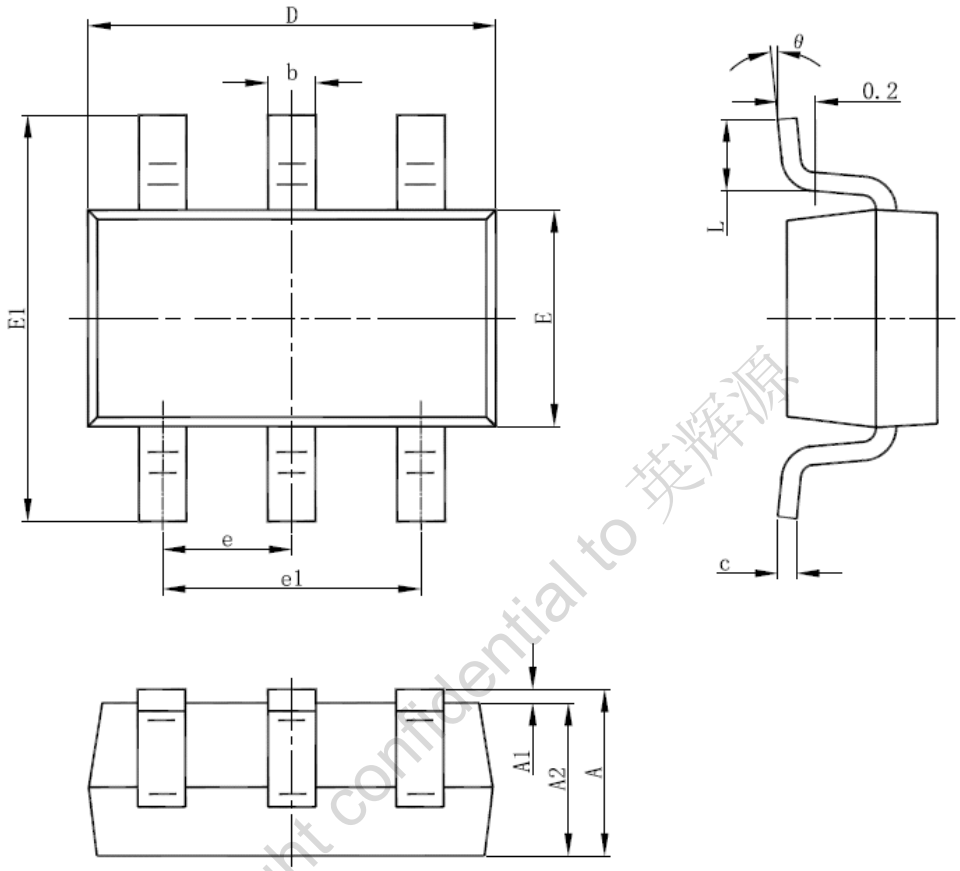
MOSFET will turn on again. In addition, the resonance oscillation between the magnetization inductance and parasitic capacitance after demagnetization may cause negative drain voltage. These may turn on SR MOSFET unexpectedly. To avoid above mis-turn-on of SR MOSFET, constant minimum off time can be used to screen it. But it may disturb SR MOSFET operation. For reliable SR operation achieve reliable SR operation, an adaptive minimum off time control is implemented in OB2004A, which can guarantee reliable synchronous rectification operation.

Gate driver

For good and efficient synchronous rectification operation, the SR MOSFET should be turned on/off in very short time. Therefore strong driver capability is needed. OB2004A can offer typical source capability 2A and typical sink capability 3A. This guarantees fast turn-on and turn-off of SR MOSFET. The gate driver voltage high level is typically 6.5V regardless of the output voltage which is ranging from 5V to 12V (typical).

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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