General Description

The OB2101H is a monolithic single-phase half-bridge gate driver IC designed for high voltage, high speed, driving power MOSFET and IGBT operating up to 650V.

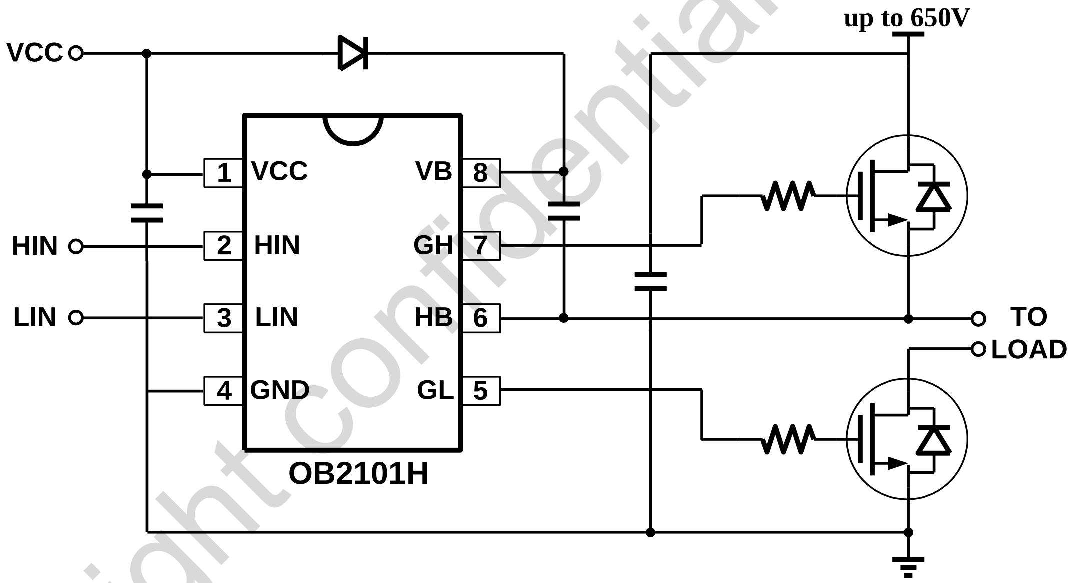
The OB2101H uses high voltage process and common mode noise canceling technique provides stable operation of high-side drivers under high dv/dt noise circumstance, and two output channels with internal deadtime to avoid cross-conduction.

The input logic level is compatible with standard 3.3V/5V. Output driver source and sink current 260mA and 530mA .

Features

- Floating channel for bootstrap operation up to 650V
- Positive input logic, and 3.3V/5V input logic compatible
- Built-in low-side supply under voltage lockout (UVLO)
- Built-in high side supply under voltage lockout (UVLO)
- Built-in cross conduction prevention logic
- Built-in dead time and matched propagation delay
- Available in SOP8 package

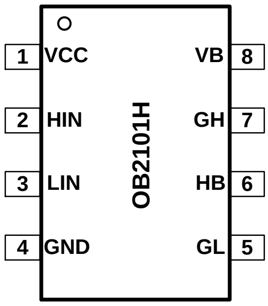
Typical Application



GENERAL INFORMATION

Pin Configuration

The pin map is shown as below for SOP8



Ordering Information

Part Number	Description
OB2101HCP	SOP8, Halogen-free, Tube
OB2101HCPA	SOP8, Halogen-free, T&R

Package Dissipation Rating

Package	RθJA (℃/W)
SOP8	90

Note: Drain Pin Connected 100mm^2 PCB copper clad.

Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VB	High side floating supply voltage	-0.3	650	V
V_{HB}	High side floating offset voltage	VB-25	VB+0.3	
V_{GH}	High side floating output voltage	V_{HB}-0.3	VB+0.3	
VCC	Low side and supply voltage	-0.3	20	
V_{GL}	Low side gate driver output	-0.3	VCC+0.3	
V_{IN}	Logic input voltage(HIN & LIN)	-0.3	VCC+0.3	
dV_{HB}/dt	Allowable offset voltage transient		50	V/ns
P_D	Package power dissipation@T_A≤+25°C		0.6	W
T_J	Junction temerature	-40	150	°C
T_S	Storage temerature	-40	125	

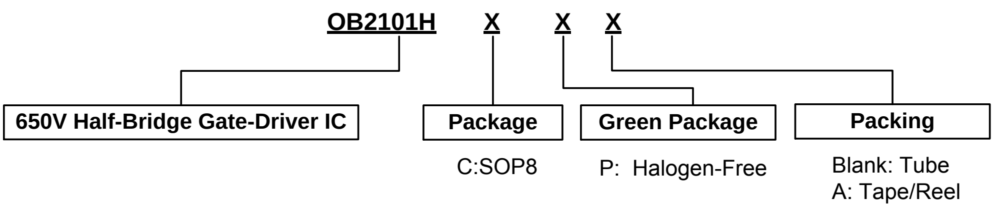
Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

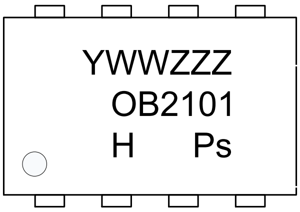
Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Description	Min	Max	Units
VB	High side floating supply voltage	V_{HB}+10	V_{HB}+20	V
V_{HB}	High side floating offset voltage		600	
V_{GH}	High side floating output voltage	V_{HB}	VB	
VCC	Low side and supply voltage	10	15	
V_{GL}	Low side gate driver output	0	VCC	
V_{IN}	Logic input voltage(HIN & LIN)	0	VCC	
T_A	Ambient temerature	-40	125	°C

Marking Information





Y:Year Code
WW:Week Code(01-52)
ZZZ:Lot Code
H:Character Code
P:Green Package(Halogen-free)
S:Internal Code(Optional)

PIN Definitions

Symbol	Description
VCC	Low side supply voltage
HIN	Logic input for high side gate driver output(GH),in phase
LIN	Logic input for low side gate driver output(GL),in phase
GND	Low side ground
GL	Low side gate driver output
HB	High side floating supply return
GH	High side gate driver output
VB	High side floating supply

Dynamic Electrical Characteristics

Setup：VCC=VB=12V，GND=HB=0V and T_A=25°C unless otherwise specified.

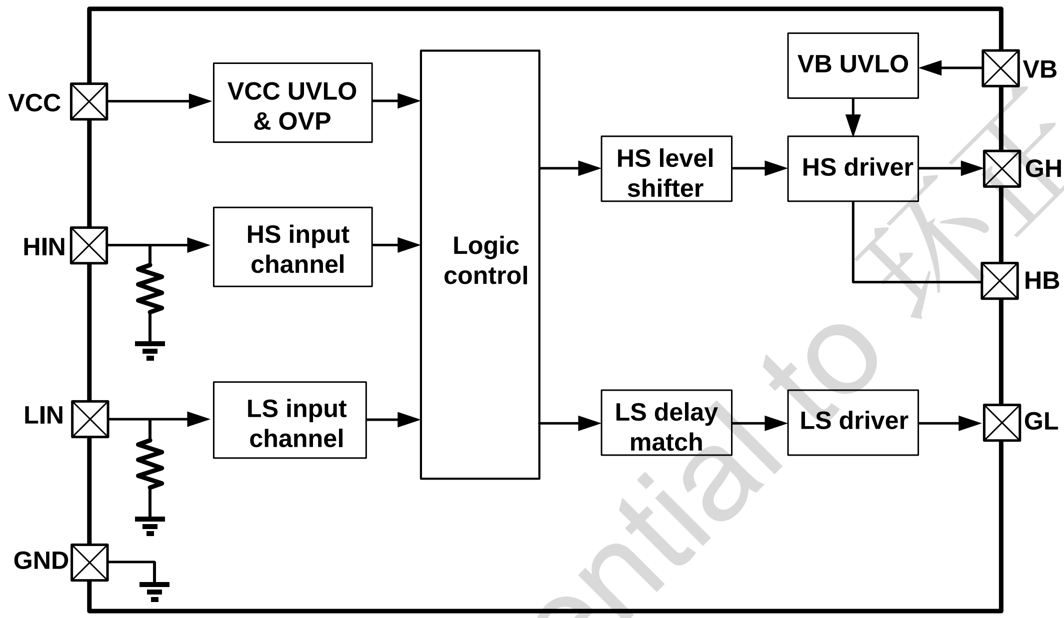
Symbol	Description	Test Conditions	Min	Typ	Max	Units
GH_t_{on}	GH turn-on propagation delay		200	310	550	
GH_t_{off}	GH turn-off propagation delay		200	310	550	
GL_t_{on}	GL turn-on propagation delay		200	350	550	
GL_t_{off}	GL turn-off propagation delay		200	350	550	ns
t_r	Turn-on rise time	Cload=1nF		95		
t_f	Turn-off fall time			45		
MT	Delay matching HS & LS turn-on/off			40		

Static Electrical Characteristics

Setup：VCC=VB=12V，Cload=10nF and T_A=25°C unless otherwise specified.

Symbol	Description	Test Conditions	Min	Typ	Max	Units
V_{IH}	Logic"1"input voltage	VCC=12V	2			V
V_{IL}	Logic"0"input voltage				0.8	
I_{IN+}	Logic"1"input bias current	V_{IN}=5V		50	150	uA
I_{IN-}	Logic"0"input bias current	V_{IN}=0V			1	
I_{LK}	Offset voltage leakage current	VB=HB=600V			1	
I_{QBS}	Quiescent VBS supply current	HIN=LIN=0V		110	200	
I_{QCC}	Quiescent VCC supply current	HIN=LIN=0V		65	120	
V_{CCUV+}	VCC supply under voltage positive going threshold		7.3	8.3	9.3	V
V_{CCUV-}	VCC supply under voltage negative going threshold		7.8	8.8	9.8	
V_{BSUV+}	VBS supply under voltage positive going threshold		6.1	7.1	8.1	
V_{BSUV-}	VBS supply under voltage negative going threshold		6.5	7.5	8.5	
I_{SOURCE_GH}	Source current of GH driver	GH=15V, HIN=5V, with PW≤10us,	160	275		mA
I_{SINK_GH}	Sink current of GH driver	GH=0V, HIN=0V, with PW≤10us,	320	530		
I_{SOURCE_GL}	Source current of GL driver	GH=15V, HIN=5V, with PW≤10us,	150	260		
I_{SINK_GL}	Sink current of GL driver	GH=0V, HIN=0V, with PW≤10us,	350	590		

Functional Block Diagram



Typical Performance Chart

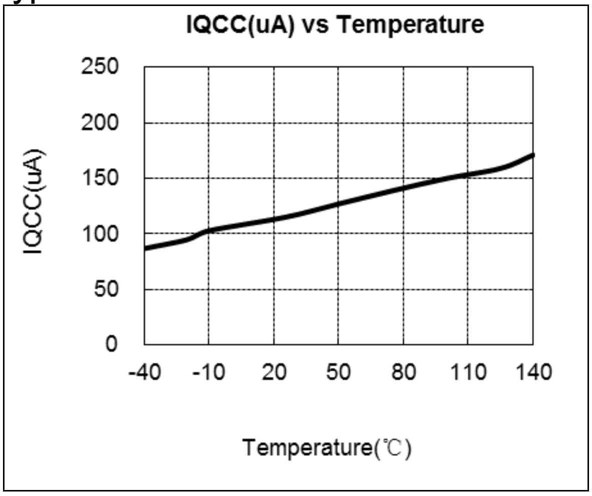


Figure 1 IQCC vs Temperature

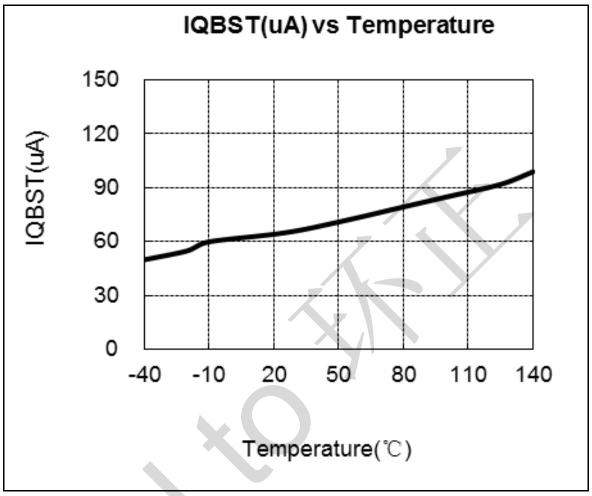


Figure 2 IQBST vs Temperature

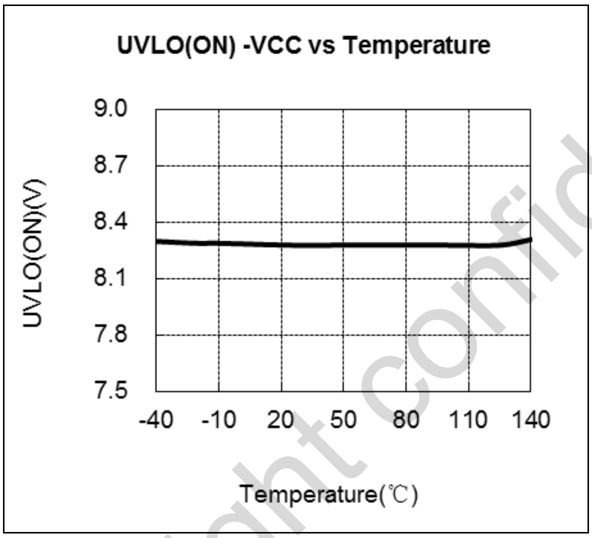


Figure 3 VCC UVLO(ON) vs Temperature

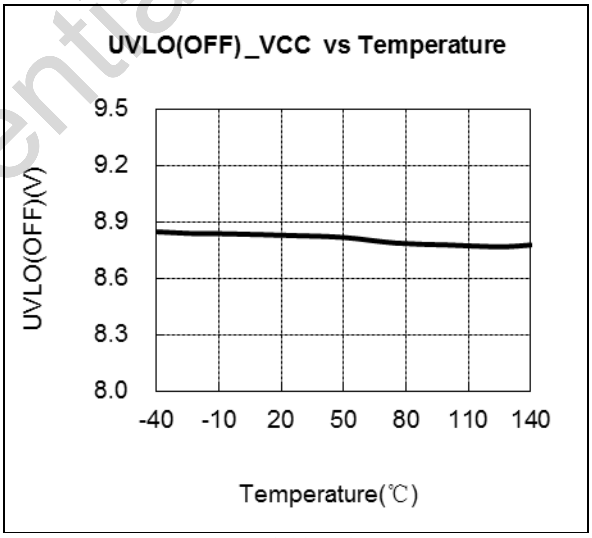


Figure 4 VCC UVLO(OFF) vs Temperature

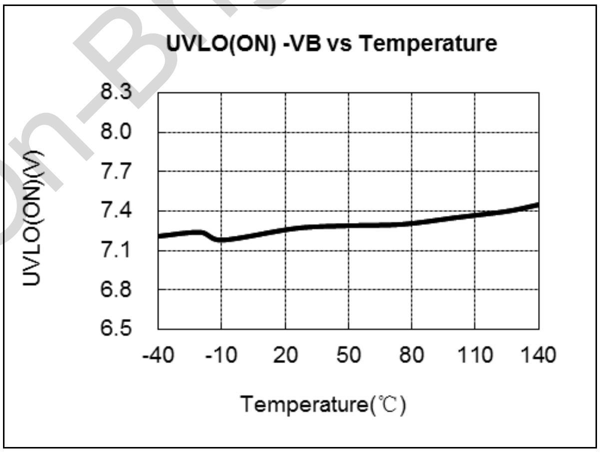


Figure 5 VB UVLO(ON) vs Temperature

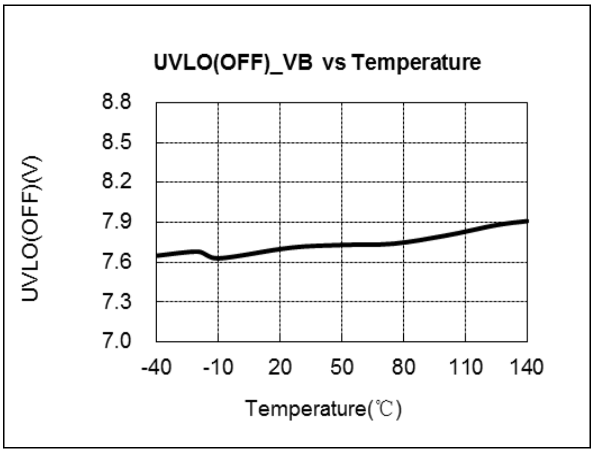


Figure 6 VB UVLO(OFF) vs Temperature

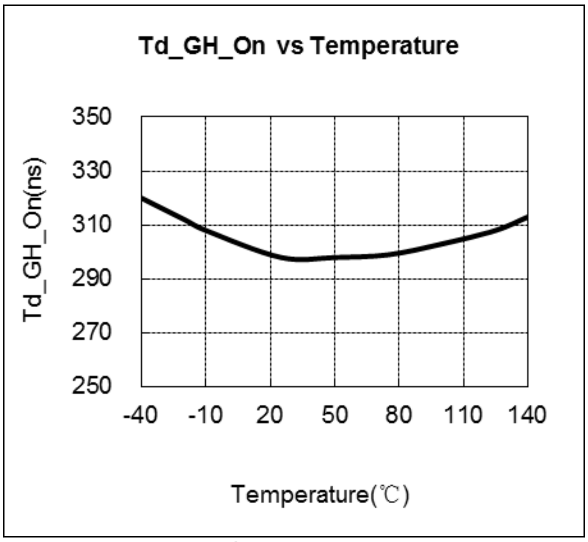


Figure 7 GH t_{ON} vs Temperature

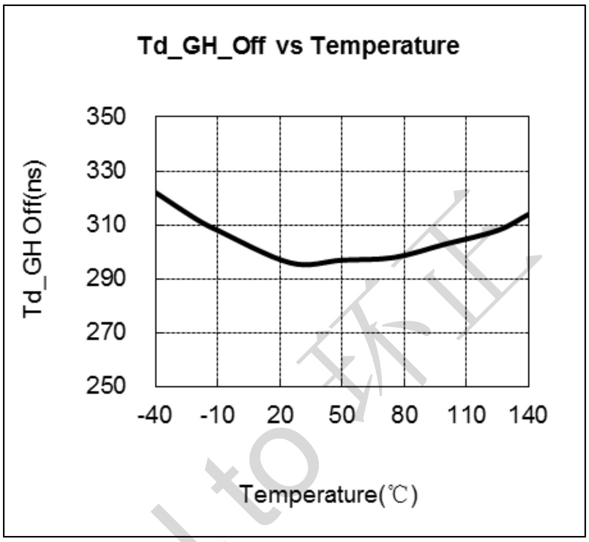


Figure 8 GH t_{OFF} vs Temperature

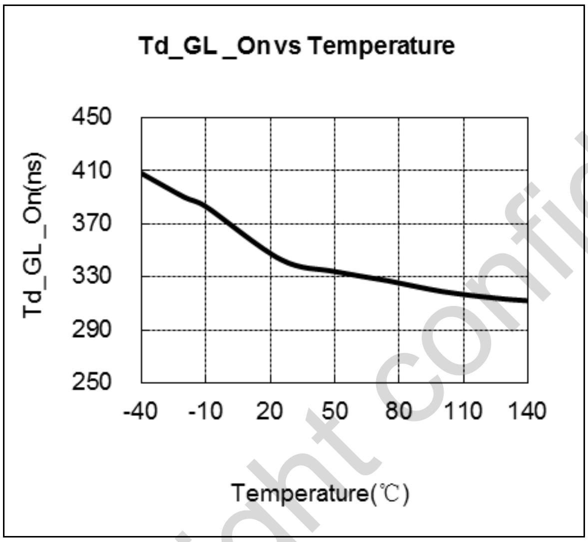


Figure 9 GL t_{ON} vs Temperature

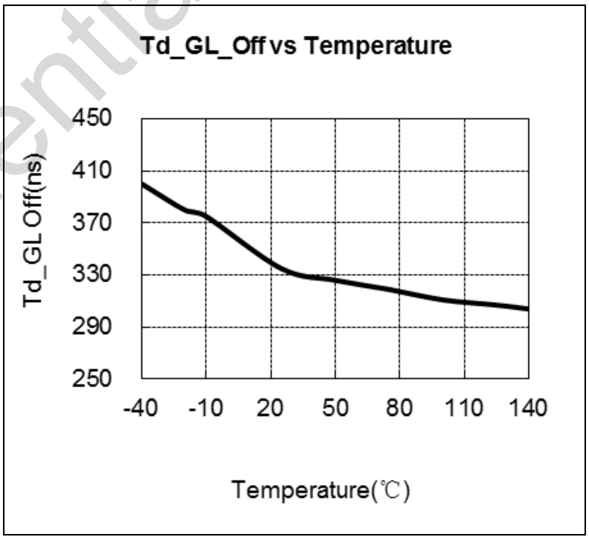


Figure 10 GL t_{OFF} vs Temperature

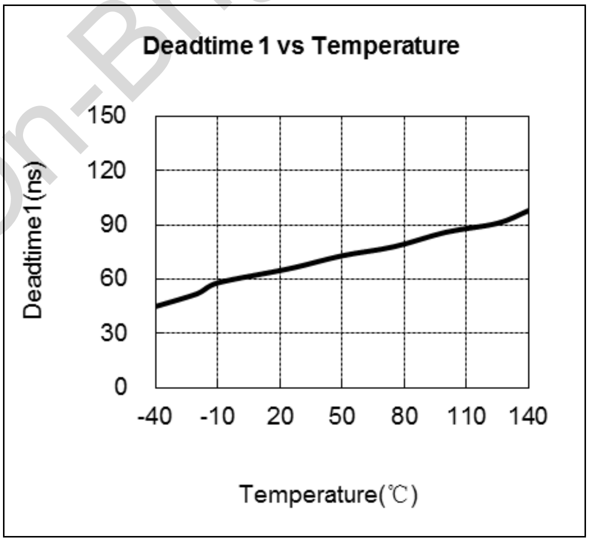


Figure 11 GLf to GHr Deadtime vs Temperature

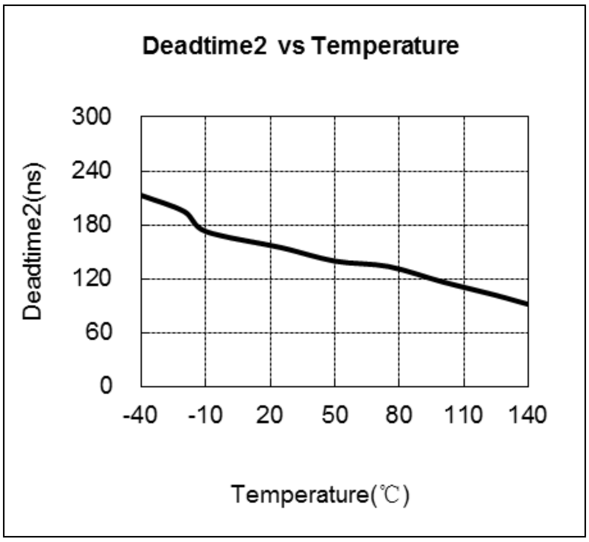


Figure 12 GHf to GLr Deadtime vs Temperature

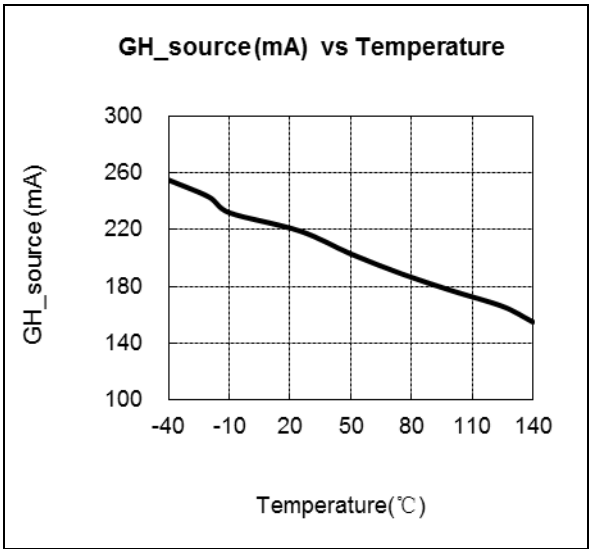


Figure 13 GH_source vs Temperature

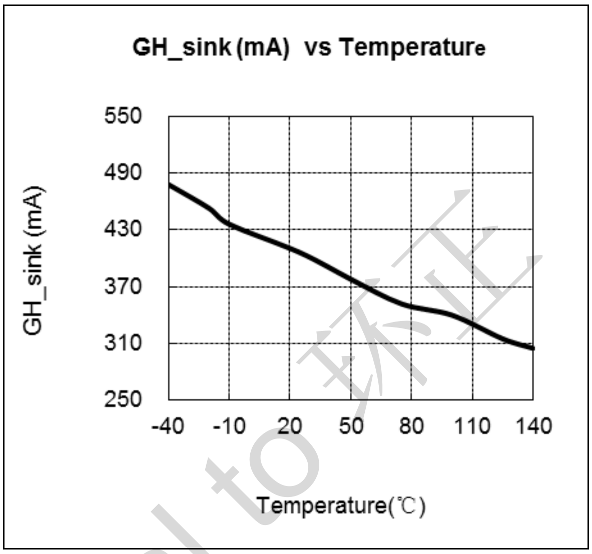


Figure 14 GH_sink vs Temperature

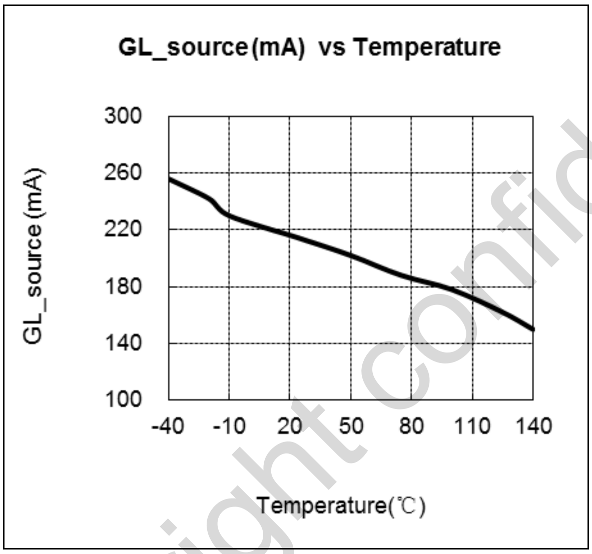


Figure 15 GL_source vs Temperature

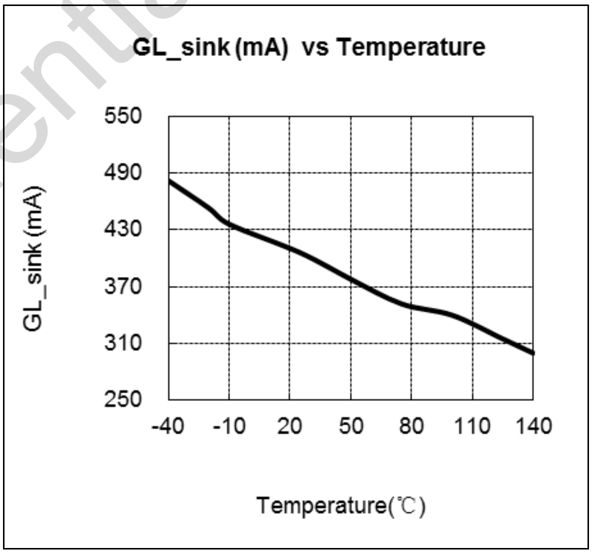
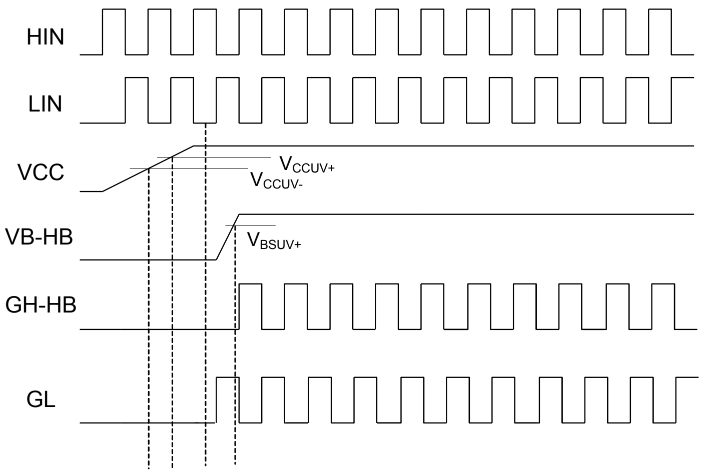


Figure 16 GL_sink vs Temperature

Timing Diagram



Operational Description

Power Supply

When VCC voltage increases above 8.8V (typical), OB2101H starts to work, open the gate drivers. When VCC voltage drops below 8.3V (typical), OB2101H shuts down the gate drivers. OB2101H will not resume working until the VCC voltage increases above 8.8V (typical).

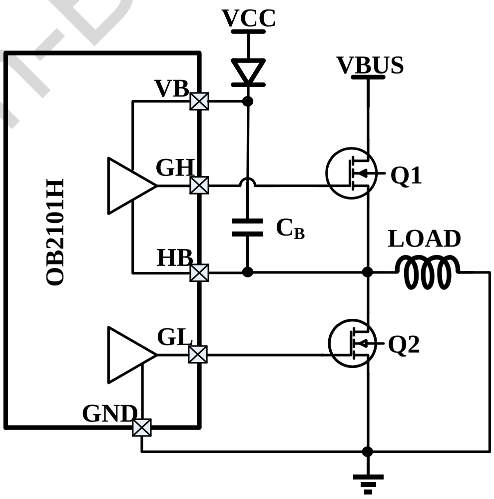
Low-Side Driver

The low-side driver is designed to drive a ground referenced N-channel MOSFET. Its low Rdson allows the external MOSFET to be turned on and off quickly.When a low-side driver is on, VCC voltage is applied to the gate of the external MOSFET.

High-Side Driver

The high-side driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HB pin. A low-power, high-speed, level-shifting circuit isolates the low-side referenced circuitry from the high-side referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit.

The bootstrap circuit consists of the diode and capacitor (C_B). In a typical application, the HB pin is at ground potential when the low-side MOSFET is on. The bootstrap diode allows capacitor C_B to be charged up to VCC-V_F during this time (where V_F is the forward voltage drop of the bootstrap diode). After the low-side MOSFET is turned off and the GH pin turns on, the voltage across capacitor C_B is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the HB pin rises with the source of the high-side MOSFET until it reaches V_{BUS}. As the VB and HB pin rise, the bootstrap diode is reverse biased preventing capacitor C_B from discharging.

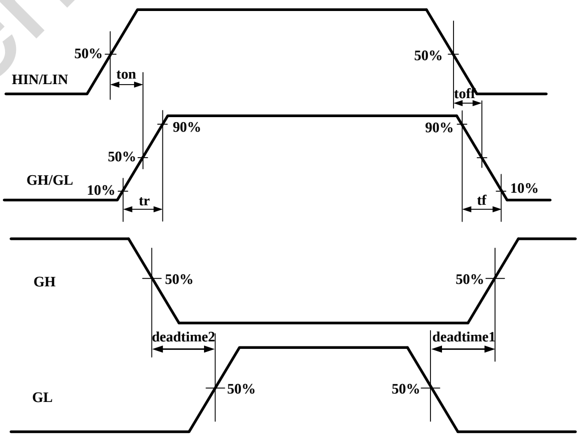


Propagation Delay and Dead-time

Propagation delay and dead-time are important considerations, as shown below. BLDC controllers use two switching MOSFETs operating complementarily. These MOSFETs must not be on at the same time or a short circuit will occur, causing high peak currents and higher power dissipation in the MOSFETs.

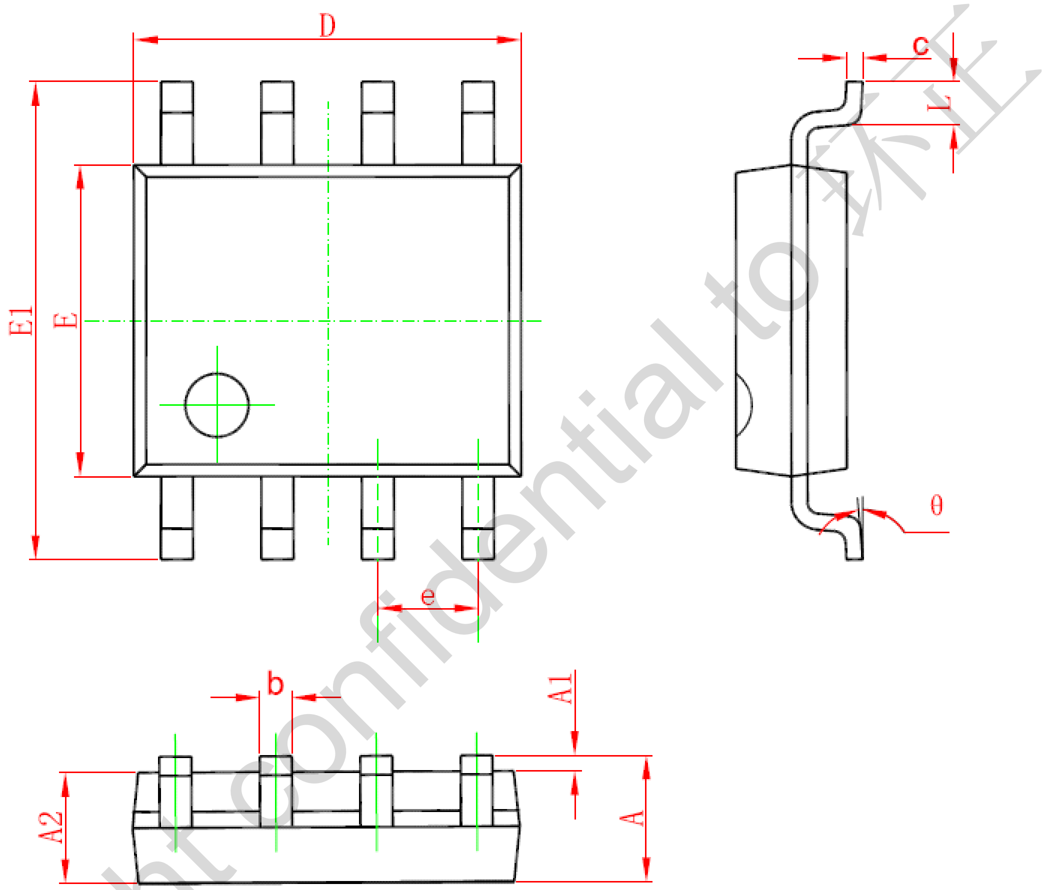
Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width results in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for C_B capacitor to charge up before the high-side driver is turned on.



PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Min
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

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