

## GENERAL DESCRIPTION

OB2269P is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with OB2269P. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. This greatly helps to reduce the external component count and system cost in application.

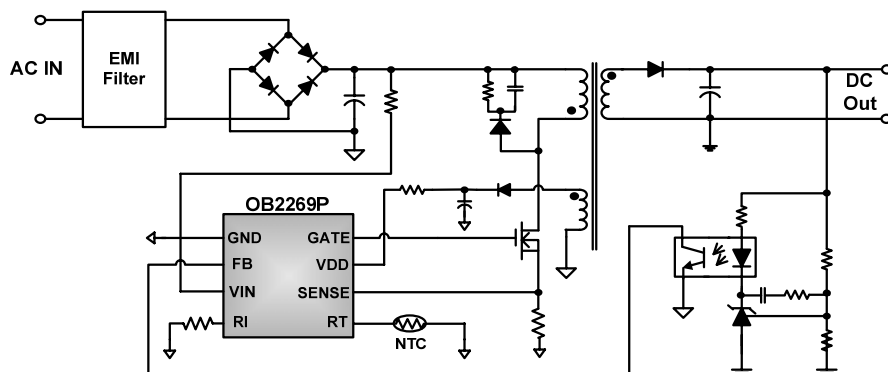
OB2269P offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage protection (OVP) and under voltage lockout (UVLO). The Gate-drive output is clamped at 18V to protect the power MOSFET.

In OB2269P, OCP threshold slope is internally optimized to reach constant output power limit over universal AC input range.

Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in operation. Consequently, audio noise performance is greatly improved.

## TYPICAL APPLICATION



OB2269P is offered in both SOP-8 and DIP-8 packages.

## FEATURES

- On-Bright Proprietary Frequency Shuffling Technology for Improved EMI Performance
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VIN/VDD Startup Current and Low Operating Current
- Power on Soft start
- Leading Edge Blanking on Current Sense Input
- Complete Protection Coverage With Auto Self-Recovery
  - External Programmable Over Temperature Protection (OTP)
  - With On-chip VDD OVP for System OVP
  - Under Voltage Lockout with Hysteresis (UVLO)
  - Gate Output Maximum Voltage Clamp (18V)
  - Line Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
  - Over Load Protection. (OLP)

## APPLICATIONS

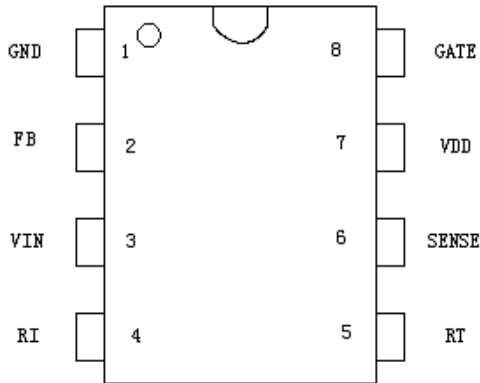
Offline AC/DC flyback converter for

- Laptop Power Adaptor
- PC/TV/Set-Top Box Power Supplies
- Open-frame SMPS
- Battery Charger

## GENERAL INFORMATION

### Pin Configuration

The OB2269P is offered in DIP and SOP packages shown as below.



### Ordering Information

Part Number	Description
OB2269PAP	With Frequency Shuffling, DIP8, Pb-free in Tube
OB2269PCP	With Frequency Shuffling, SOP8, Pb-free in Tube
OB2269PCPA	With Frequency Shuffling, SOP8, Pb-free in Taping

### Package Dissipation Rating

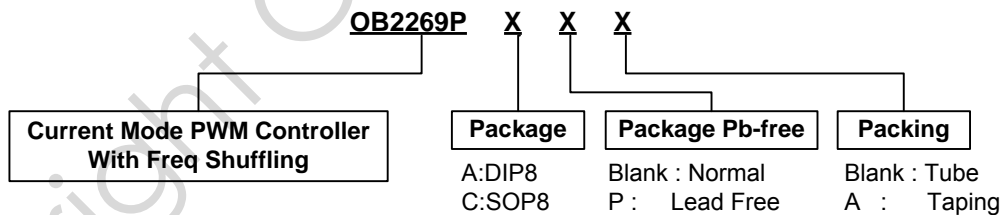
Package	R $\theta$ JA (°C/W)
DIP8	90
SOP8	150

### Absolute Maximum Ratings

Parameter	Value
VDD/VIN DC Supply Voltage	30 V
VDD Zener Clamp Voltage <sup>Note</sup>	VDD_Clamp+0.1V
VDD Clamp Continuous Current	10 mA
FB Input Voltage	-0.3 to 7V
Sense Input Voltage	-0.3 to 7V
RT Input Voltage	-0.3 to 7V
RI Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T <sub>j</sub>	-40 to 150 °C
Min/Max Storage Temperature T <sub>stg</sub>	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

**Note:** VDD\_Clamp has a nominal value of 35V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



## Marking Information



Y: Year Code  
 WW: Week Code(01-52)  
 ZZZ: Lot Code  
 A: DIP8 Package  
 P: Pb-free Package  
 X: Version Num (X=P)  
 S: Internal Code(Optional)

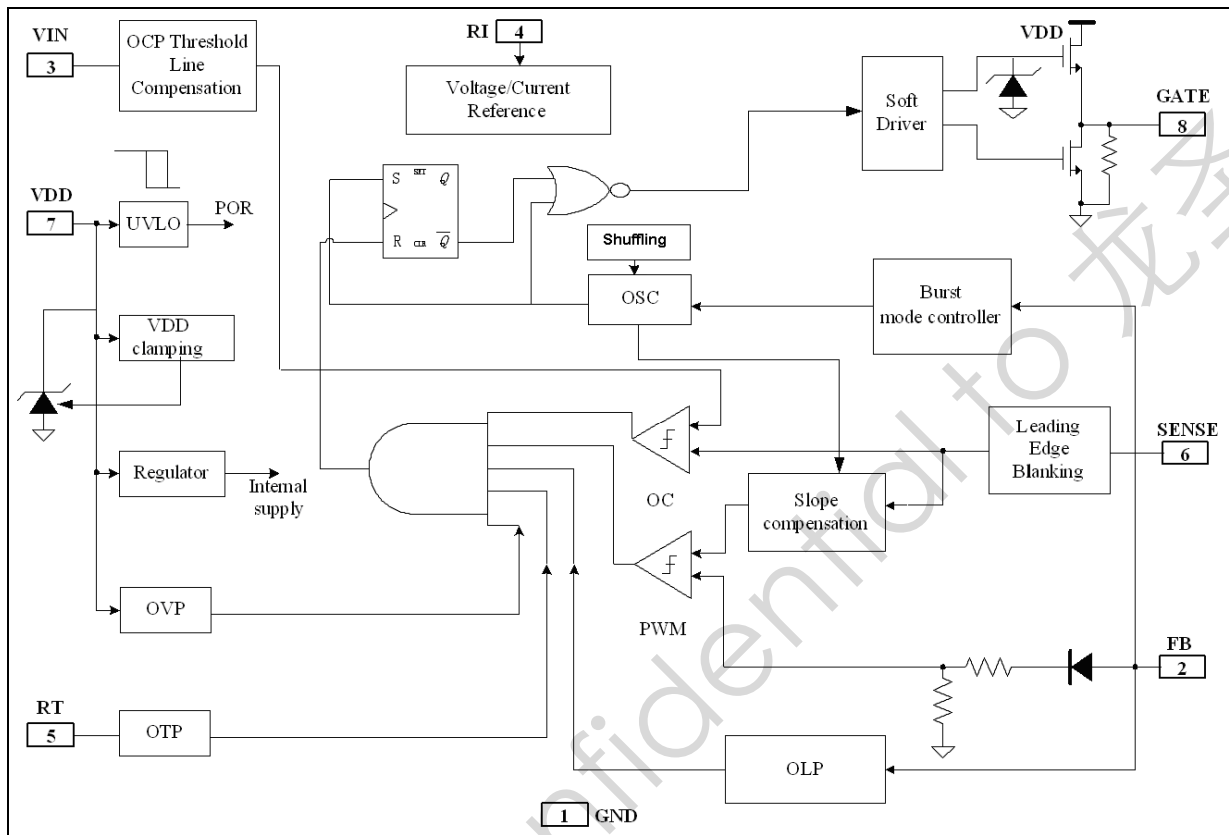


Y: Year Code  
 WW: Week Code(01-52)  
 ZZZ: Lot Code  
 C: SOP8 Package  
 P: Pb-free Package  
 X: Version Num (X=P)  
 S: Internal Code(Optional)

## TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
3	VIN	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

## BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	12	23	V
RI	RI Resistor Value	24	31	Kohm
T <sub>A</sub>	Operating Ambient Temperature	-20	85	°C

## ESD INFORMATION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HBM <sup>Note</sup>	Human Body Model on All Pins Except VIN and VDD	MIL-STD		3		KV
MM	Machine Model on All Pins	JEDEC-STD		250		V

**Note:** HBM all pins pass 3KV except High Voltage Input pin. The details are VIN passes 1kV, VDD passes 1.5KV, all other I/Os pass 3KV. In system application, High Voltage Input pin is either a high impedance input or connected to a cap. The lower rating has minimum impacts on system ESD performance.

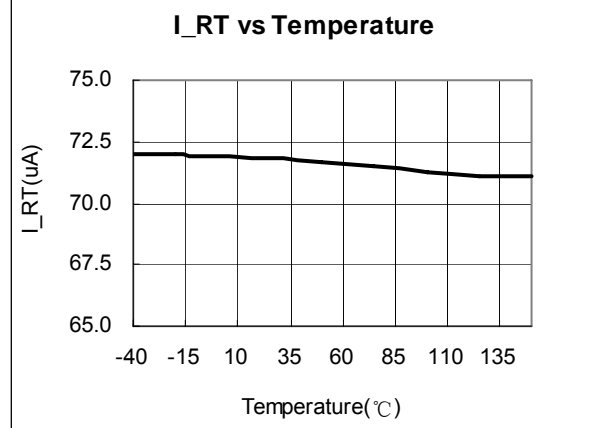
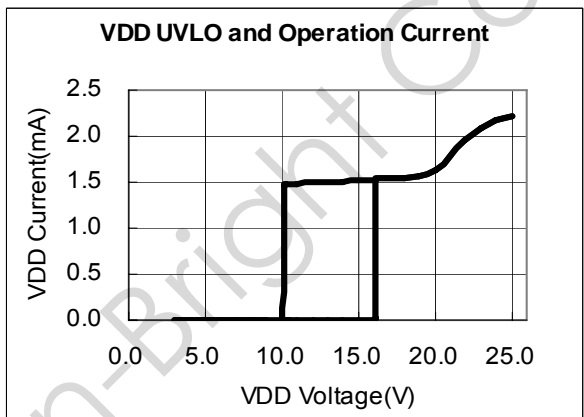
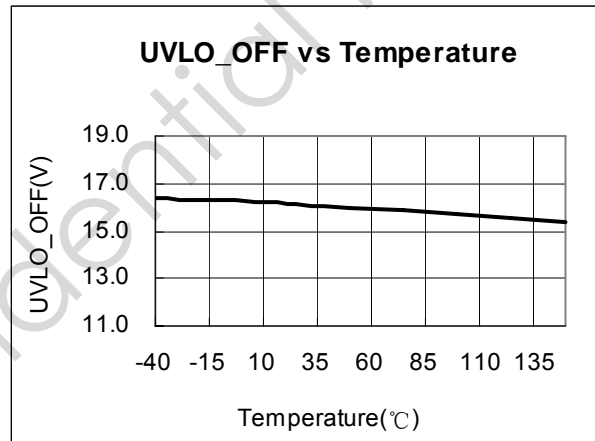
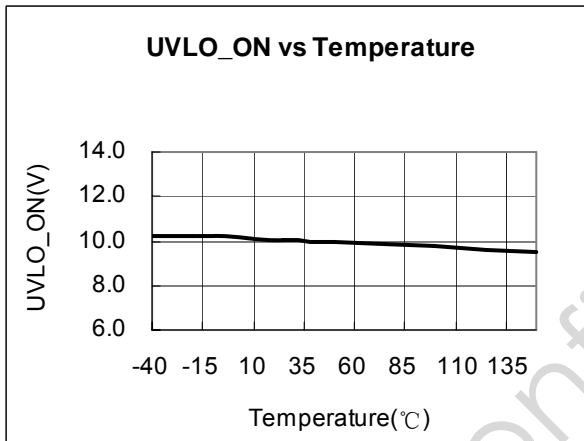
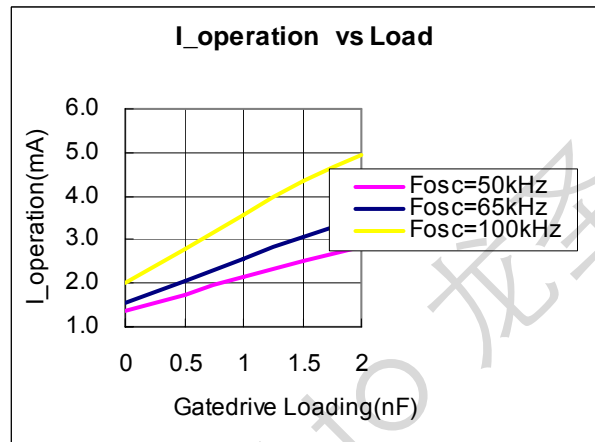
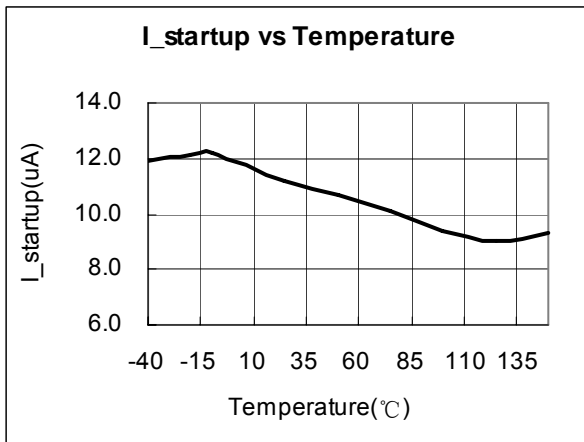
## ELECTRICAL CHARACTERISTICS

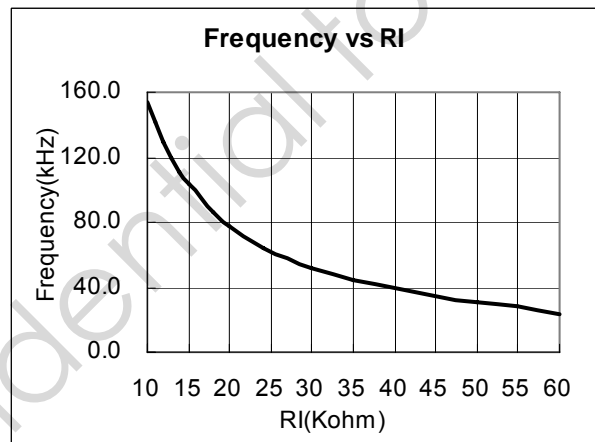
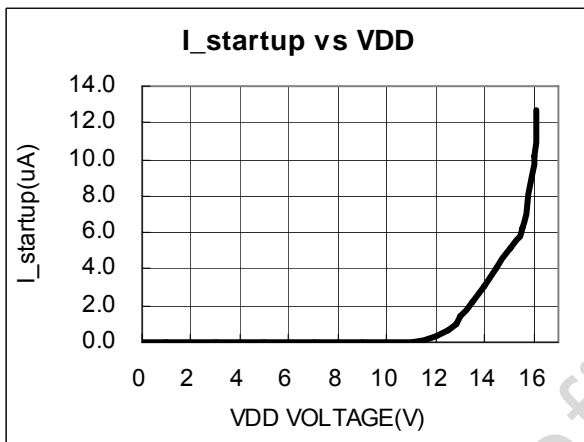
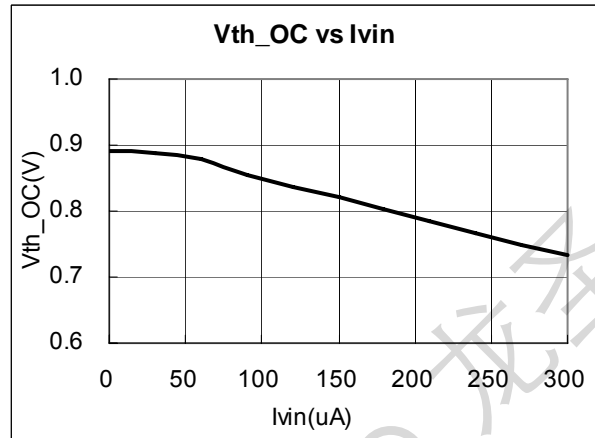
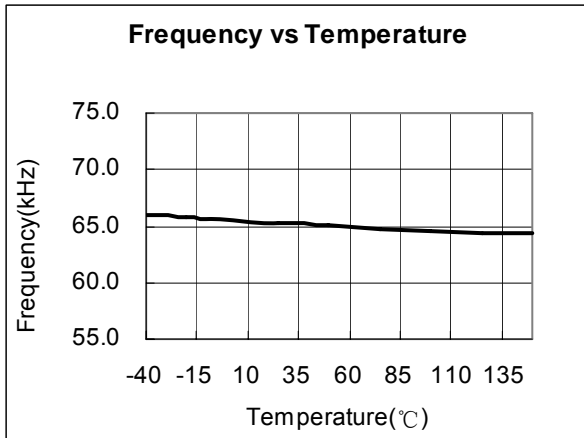
(T<sub>A</sub> = 25°C, VDD=16V, RI=24Kohm if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Supply Voltage (VDD)</b>						
I_VDD_Startup	VDD Start up Current	VDD =15V, Measure current into VDD		6.5	20	uA
I_VDD_Operation	Operation Current	V <sub>FB</sub> =3V		1.7		mA
UVLO(Enter)	VDD Under Voltage Lockout Enter		9.2	10.2	11.2	V
UVLO(Exit)	VDD Under Voltage Lockout Exit (Startup)		15.2	16.2	17.2	V
OVP(ON)	VDD Over Voltage Protection Enter		24	25.5	27	V
OVP(OFF)	VDD Over Voltage Protection Exit (Recovery)		21.5	23	24.5	V
OVP_Hys	OVP Hysteresis	OVP(ON)-OVP(OFF)		2.5		V
T <sub>D</sub> _OVP	VDD OVP Debounce time			80		uSec
V <sub>DD</sub> _Clamp	V <sub>DD</sub> Zener Clamp Voltage	I(V <sub>DD</sub> ) = 5mA		35		V
<b>Feedback Input Section(FB Pin)</b>						
A <sub>VCS</sub>	PWM Input Gain	$\Delta V_{FB} / \Delta V_{CS}$		2.8		V/V
V <sub>FB</sub> _Open	V <sub>FB</sub> Open Voltage			6.3		V
I <sub>FB</sub> _Short	FB pin short circuit current	Short FB pin to GND, measure current		0.45		mA
V <sub>TH</sub> _0D	Zero Duty Cycle FB Threshold Voltage				0.95	V
V <sub>TH</sub> _BM	Burst Mode FB Threshold Voltage			1.7		V
V <sub>TH</sub> _PL	Power Limiting FB Threshold Voltage			4.4		V
T <sub>D</sub> _PL	Power limiting Debounce Time			80		mSec
Z <sub>FB</sub> _IN	Input Impedance			7.2		Kohm
<b>Current Sense Input(Sense Pin)</b>						
T <sub>blanking</sub>	Sense Input Leading Edge Blanking Time			250		nS
Z <sub>SENSE</sub> _IN	Sense Input Impedance			30		Kohm

T <sub>D_OC</sub>	Over Current Detection and Control Delay	CL=1nf at GATE,		120		nSec
V <sub>TH_OC_0</sub>	Current Limiting Threshold at No Compensation	I(VIN) = 0uA	0.85	0.90	0.95	V
V <sub>TH_OC_1</sub>	Current Limiting Threshold at Compensation	I(VIN) = 150uA		0.81		V
T <sub>ss</sub>	Soft start time			4		ms
<b>Oscillator</b>						
F <sub>osc</sub>	Normal Oscillation Frequency		60	65	70	KHZ
Δf <sub>Temp</sub>	Frequency Temperature Stability	-20°C to 100°C		2		%
Δf <sub>VDD</sub>	Frequency Voltage Stability	VDD = 12-25V		2		%
RI <sub>range</sub>	Operating RI Range		12	24	60	Kohm
V <sub>RI<sub>open</sub></sub>	RI open voltage			2.0		V
F <sub>BM</sub>	Burst Mode Base Frequency			22		KHZ
DC <sub>max</sub>	Maximum Duty Cycle		75	80	85	%
DC <sub>min</sub>	Minimum Duty Cycle		-	-	0	%
<b>Gate Drive Output</b>						
VOL	Output Low Level	Io = -20 mA			0.3	V
VOH	Output High Level	Io = +20 mA	11			V
VG <sub>Clamp</sub>	Output Clamp Voltage Level	VDD=20V		18		V
T <sub>r</sub>	Output Rising Time	CL = 1nf		120		nSec
T <sub>f</sub>	Output Falling Time	CL = 1nf		50		nSec
<b>Over Temperature Protection</b>						
I <sub>RT</sub>	Output Current of RT pin			70		uA
V <sub>TH_OTP</sub>	OTP Threshold Voltage		1.015	1.065	1.115	V
V <sub>TH_OTP<sub>off</sub></sub>	OTP Recovery Threshold Voltage			1.165		V
T <sub>D_OTP</sub>	OTP De-bounce Time			100		uSec
V <sub>RT<sub>Open</sub></sub>	RT Pin Open Voltage			3.5		V
<b>Frequency Shuffling</b>						
Δf <sub>OSC</sub>	Frequency Modulation range /Base frequency			±4%		%
Freq <sub>Shuffling</sub>	Shuffling Frequency	RI = 24Kohm		64		HZ

**CHARACTERIZATION PLOTS**







## OPERATION DESCRIPTION

The OB2269P is a highly integrated PWM controller IC optimized for offline flyback converter applications. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

### ● Startup Current and Start up Control

Startup current of OB2269P is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

### ● Operating Current

The Operating current of OB2269P is low at 1.7mA (typical). Good efficiency is achieved with OB2269P low operating current together with extended burst mode control schemes.

### ● Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in OB2269P. The oscillation frequency is modulated with an internally generated random source so that the tone energy is evenly spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

### ● Burst Mode Operation

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. OB2269P adjusts the switching mode according to the loading condition. At the load level of no load to light/medium load, the FB input drops below burst mode threshold level (1.8V) and the device enters Burst Mode control. The Gate driver output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate driver remains at off state to minimize the switching loss

thus to reduce the standby power consumption to the greatest extent.

The nature of high frequency switching also reduces the audio noise at any loading conditions.

### ● Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = \frac{1560}{RI(Kohm)} (Khz)$$

### ● Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2269P current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

### ● Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

### ● Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current  $I_{RT}$  flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than  $V_{TH\_OTP}$ .

### ● Gate Driver

OB2269P Gate pin is connected to the Gate of an external MOSFET for power switch control. Too

weak the gate driver strength results in higher conduction and switching loss of MOSFET, while too strong gate driver output compromises the EMI.

Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

- **Protection Controls**

Good system reliability is achieved with OB2269P's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP) and under voltage lockout (UVLO).

The OCP threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold

slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on OB2269P.

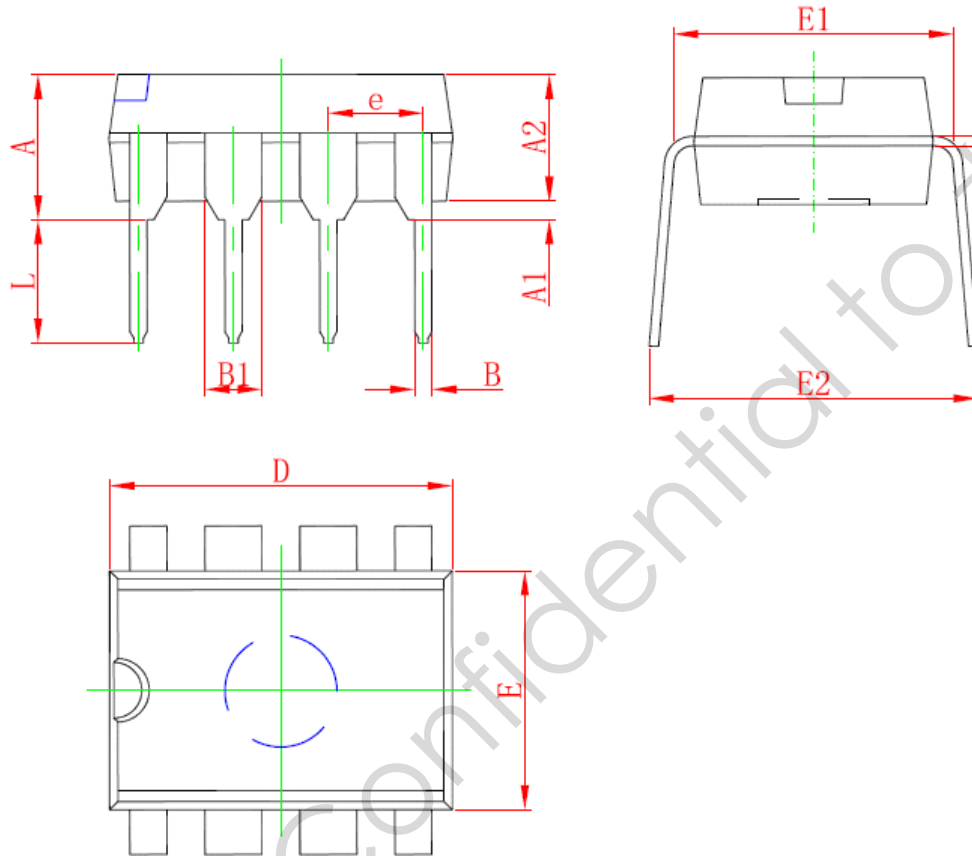
At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. OB2269P resumes the operation when temperature drops below the hysteresis value.

VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter.

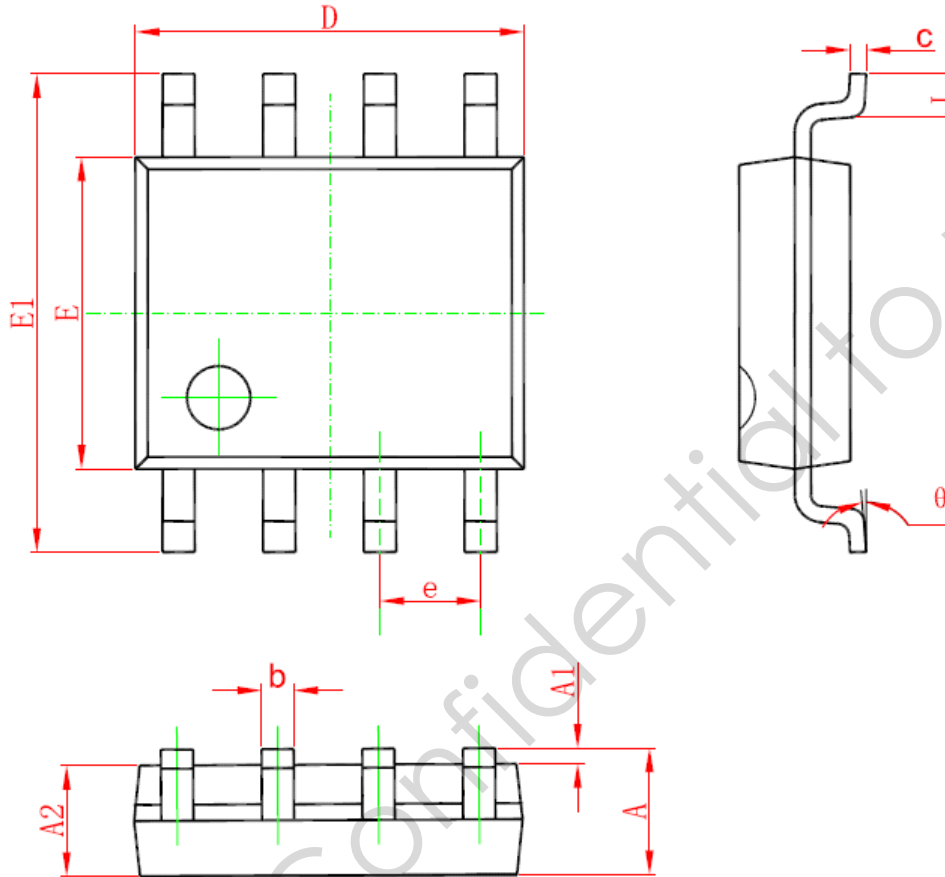
**PACKAGE MECHANICAL DATA**

**8-Pin Plastic DIP**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

**8-Pin Plastic SOP**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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