

GENERAL DESCRIPTION

OB2710 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

At normal load condition, it operates in fixed frequency mode. When the loading goes low, it operates in PFM mode for high power conversion efficiency. When the load is very small, the IC operates in 'Extended Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

VCC low startup current and low operating current contribute to a reliable power on startup and low standby design with

OB2710 offers V_{th_oc} compensation.

OB2710 offers comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), AC brownout protection, VCC under voltage lockout (UVLO), external over temperature protection (OTP), over voltage protection (OVP) and short protection (SCP). Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.

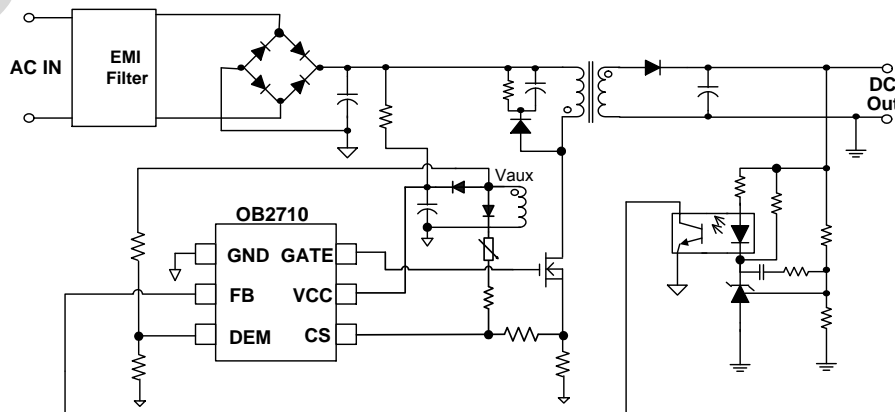
The tone energy at below 23KHz is minimized in the design and audio noise is eliminated during operation.

OB2710 is offered in SOT23-6 package.

FEATURES

- Power on soft start reducing MOSFET Vds stress
- Multi-Mode Operation
 - 77KHz maximum clamping frequency in QR mode @ Full Load in high line voltage
 - 65KHz minimum clamping frequency in CCM mode @ Heavy Load in high line voltage
 - 100KHz maximum clamping frequency in QR mode @ Full Load in low line voltage

TYPICAL APPLICATION



- 85KHz minimum clamping frequency in CCM mode @ Heavy Load in low line voltage
- Valley switching operation @ Green mode
- Burst Mode @ Light Load & No Load

- Frequency shuffling for EMI
- Extended burst mode control for improved efficiency and low standby power design
- Audio noise free operation
- Adjust V_{th_oc} compensation through CS pin, the compensate value can be regulated by the resistor series with CS pin.
- Comprehensive protection coverage
 - VCC Under Voltage Lockout with hysteresis (UVLO)
 - VCC Over Voltage Protection (VCC OVP)
 - Cycle-by-cycle over current threshold setting for constant output power limiting over universal input voltage range
 - Over Load Protection (OLP) with auto-recovery
 - Brownout protection with auto-recovery, line OVP with auto-recovery
 - Output Over Voltage Protection (Output OVP) with auto-recovery, and the OVP triggered voltage can be adjusted by the resistors connected between auxiliary winding and ground
 - Adjust Over Temperature Protection (OTP) through CS pin with auto-recovery
 - Output diode short protection with auto-recovery
 - Output SCP Protection with auto-recovery

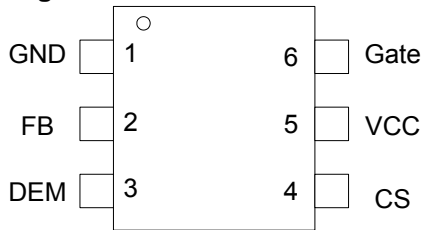
APPLICATIONS

Offline AC/DC flyback converter for

- General power supply
- Power Adapter

GENERAL INFORMATION

Pin Configuration



Ordering Information

Part Number	Description
OB2710MP	SOT23-6, Halogen-free in T&R

Package Dissipation Rating

Package	R θ JA(°C/W)
SOT23-6	200

Recommended operating condition

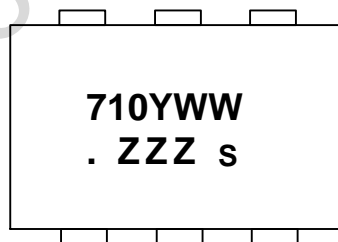
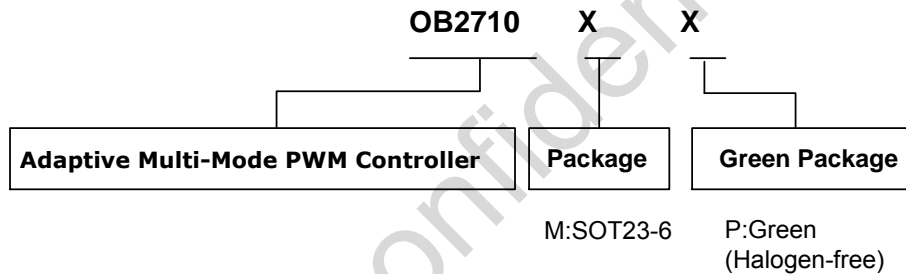
Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 26V

Absolute Maximum Ratings

Parameter	Value
VCC DC Supply Voltage	32V
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
DEM Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T _J	-40 to 150 °C
Min/Max Storage Temperature T _{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Marking Information

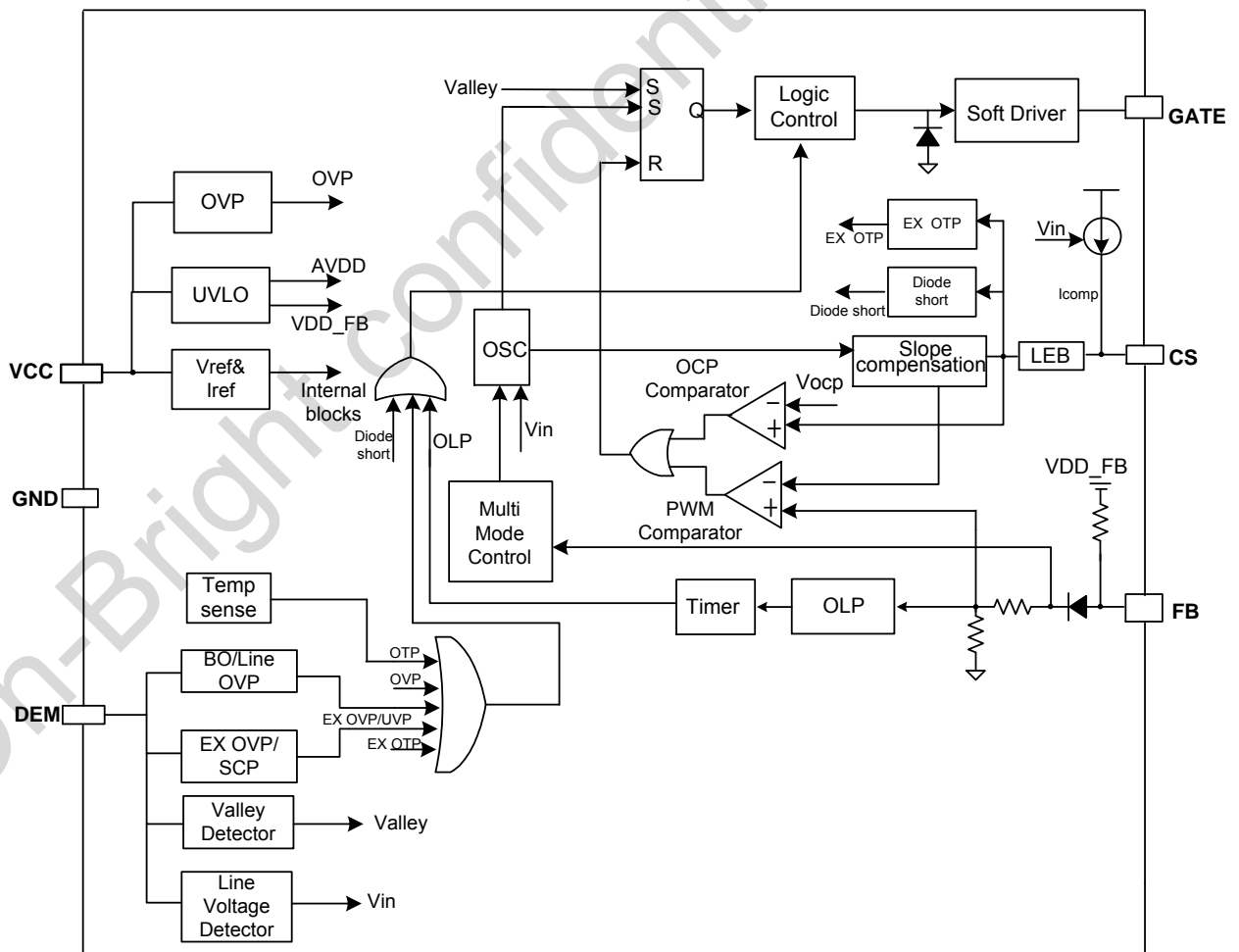


Y: Year Code
 WW: Week Code(01-52)
 ZZZ: Lot code
 S: Internal code

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
VCC	P	Power Supply
CS	I	Current sense input. Series a resistor to Rsense can adjust the V_{th_oc} to regulate the OCP point. This pin is also connected to an auxiliary winding of the PWM transformer through a NTC resistor and a diode for over temperature protection.
Gate	O	Totem-pole gate driver output for power MOSFET
GND	P	Ground
DEM	I	Multiple functions pin. Connecting two resistors from Vaux to ground can adjust output OVP trigger voltage, SCP trigger voltage, Brown-in/Brown-out, line OVP trigger current and detect transformer core demagnetization.
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin CS.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(T_A = 25°C, VCC=18V, unless otherwise noted)

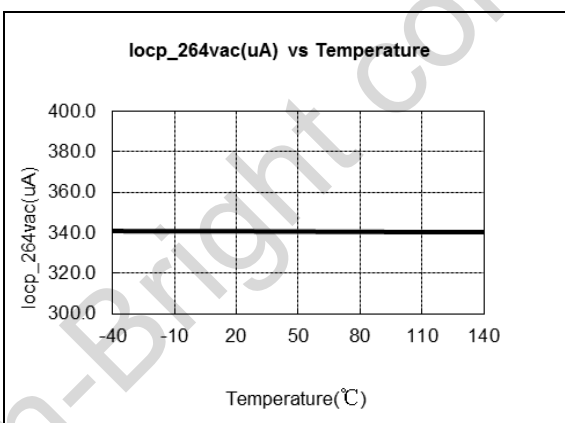
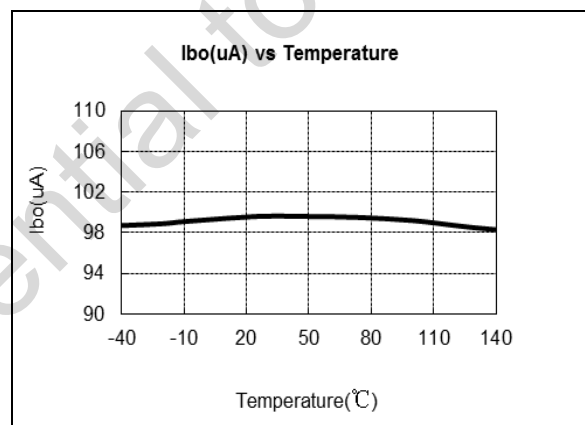
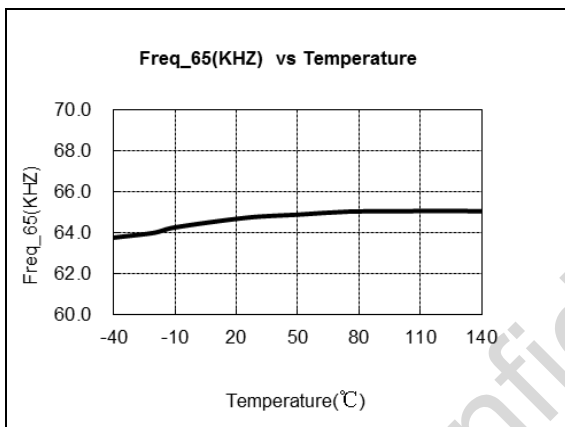
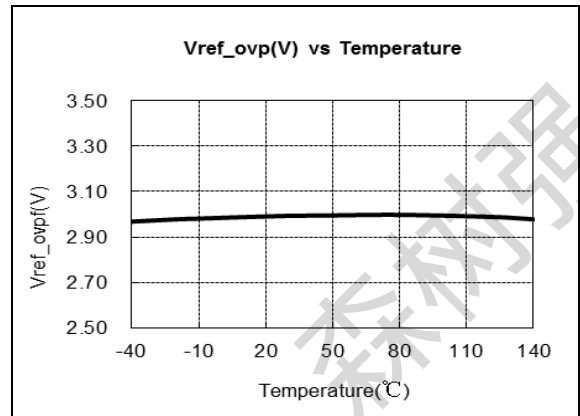
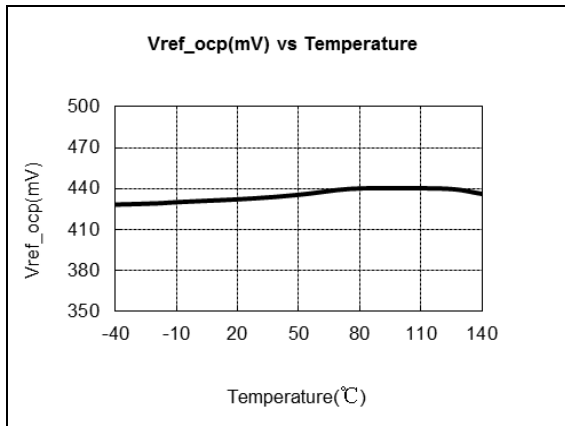
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VCC)						
I _{startup}	VCC Start up Current	VCC=UVLO(OFF)-1V, measure leakage current into VCC		2	5	uA
I _{VCC_Operation}	Operation Current	VCC=18V,CS=4V, FB=3.5V,measure I(VCC)		2	3	mA
I _{VCC_Burst}	Burst Current	CS=0V,FB=0.5V, measure I(VCC)		0.25	0.50	mA
UVLO(ON)	VCC Under Voltage Lockout Enter		7.0	7.5	8.0	V
UVLO(OFF)	VCC Under Voltage Lockout Exit (Recovery)		16	17	18	V
V _{pull-up}	Pull-up PMOS active			10		V
OVP	VCC Over Voltage Protection threshold voltage	FB=3V,CS=0V. Slowly ramp VCC, until no gate switching.	28.5	30.0	31.5	V
Feedback Input Section(FB Pin)						
V _{FB_Open}	V _{FB} Open Loop Voltage		3.4	3.8	4.2	V
Av _{cs}	PWM input gain $\Delta V_{FB}/\Delta V_{CS}$			4		V/V
Maximum duty cycle	Max duty cycle @ VCC=18V,VFB=3V,VCS=0V		75	80	85	%
V _{ref_green}	The threshold enter green mode			2.0		V
V _{ref_burst_H}	The threshold exits burst mode			1.15		V
V _{ref_burst_L}	The threshold enters burst mode			1.05		V
I _{FB_Short}	FB pin short circuit current	Short FB pin to GND and measure current		0.12		mA
V _{TH_OLP}	Open loop protection, FB Threshold Voltage		3.0	3.3	3.6	V
T _{d_OLP}	Open loop protection, Debounce Time			60		ms
Z _{FB_IN}	Input Impedance			31.5		K Ω
Current Sense Input(CS Pin)						
SST _{CS}	Soft start time for CS peak			2.5		ms
T _{blanking}	Leading edge blanking time			250		ns
T _{d_OC}	Over Current Detection and Control Delay	From Over Current Occurs till the Gate driver output start to turn off		80		ns
V _{TH_OC}	Internal Current Limiting Threshold Voltage with zero duty cycle			0.45		V
I _{comp_90v}	Compensation current@90Vac flow out from CS pin			140		uA
I _{comp_264v}	Compensation current@264Vac flow out from CS pin			335		uA
V _{ref_dio}	CS pin threshold for diode short			0.8		V
TD _{dio}				8		Cycles
V _{TH_OTP}	CS pin external OTP threshold		0.28	0.30	0.32	V
TD _{OTP}	External OTP debounce time	FB > V _{ref_burst_H}		60		ms
DEM pin						
I _{brown-in}	Brown-in threshold current		100	107	114	uA

I _{brown-out}	Brown-out threshold current		95	100	105	uA
T _{d_BO}	Brown-out protection, Debounce Time			30		ms
I _{line_OVP}	Line_OVP threshold current		415	440	465	uA
I _{line_OVP_exit}	Line_OVP threshold current exit			425		uA
T _{d_Lineovp}	Line_OVP, Debounce Time			400		ms
V _{output_ovp}	Voltage threshold for adjustable output OVP		2.85	3.0	3.15	V
T _{samp}	T _{off} sampling delay time			2.2		uS
T _{d_output_ovp}	Output OVP debounce time			8		Cycles
V _{TH_scp}	SCP threshold (Startup blanking 12ms)			600		mV
T _{D_SCP}	Output SCP debounce time			8		Cycles
In-chip OTP						
OTP enter				150		°C
OTP exit				120		°C
Oscillator						
F _{osc_max_QR_H}	Average max clamp oscillation frequency in QR mode	VCC=15V,FB=3V,Vac<150V		100		KHz
F _{osc_max_QR_L}	Average max clamp oscillation frequency in QR mode	VCC=15V,FB=3V,Vac>165V		77		KHz
Δf _{OSC_max_QR}	Max clamp oscillation frequency jittering			±6		%
F _{osc_min_CCM_H}	Min clamp oscillation frequency in CCM mode	VCC=15V,FB=3V,Vac<150V		85		KHz
F _{osc_min_CCM_L}	Min clamp oscillation frequency in CCM mode	VCC=15V,FB=3V,Vac>165V		65		KHz
Δf _{OSC_CCM}	Min clamp oscillation frequency jittering			±6		%
F _{shuffling}	Shuffling frequency			240		Hz
F _{Burst}	Burst Mode Switch Frequency			25		KHz
Gate driver						
V _{OL}	Output low level @ VCC=18V, I _o =5mA				1	V
V _{OH}	Output high level @ VCC=18V, I _o =20mA		6			V
V _{clamping}	Output clamp voltage			11		V
T _r	Output rising time 1.1V ~ 9.9V @ CL=1000pF			300		ns
T _f	Output falling time 9.9V ~ 1.1V @ CL=1000pF			50		ns

Note1: In burst mode output OTP is disable.

CHARACTERIZATION PLOTS

VCC = 18V, TA = 25°C condition applies if not otherwise noted.



OPERATION DESCRIPTION

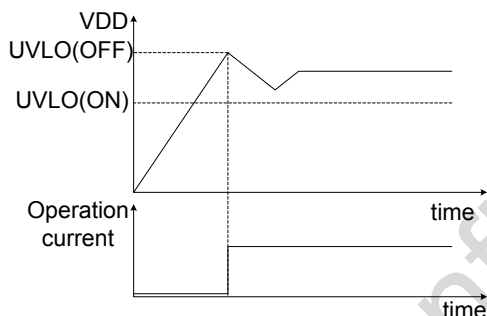
OB2710 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications. The 'extended burst mode' control greatly reduces the standby power consumption and helps the design easier to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of OB2710 is designed to be very low so that VCC could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of OB2710 is low at 2mA (typical). Good efficiency is achieved with OB2710 low operation current together with the 'extended burst mode' control features.

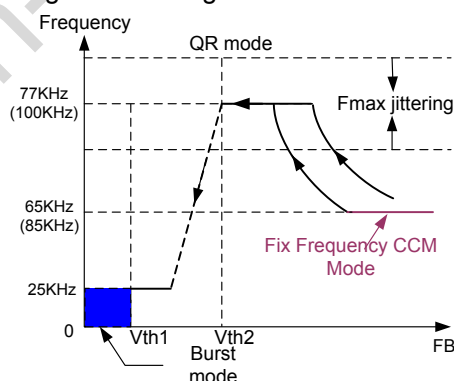


Soft Start

OB2710 features an internal 2.5ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VCC reaches UVLO(OFF), the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Multi Mode Operation for High Efficiency

OB2710 is a multi-mode QR/PWM controller. The controller changes the mode of operation according to line voltage and load conditions.



At full load conditions, there are two situations: firstly, if the system input is in low line input range, the IC operates in 85K fixed frequency CCM mode. Thus, small size transformer can be used with high power conversion efficiency. Secondly, if the system input is in high line input range, the IC operates in QR mode. In this way, high power conversion efficiency can be achieved in the universal input range when system is at full loading conditions.

At normal operating conditions ($V_{th2} < V_{FB}$), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when the average 77KHz frequency clamping is reached under high line input range, and the average 100KHz frequency clamping is reached under low line input range.

At light load conditions ($V_{th1} < V_{FB} < V_{th2}$), the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. Generally, in flyback converter, the decreasing of load results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency fold-back is realized and high power conversion efficiency is achieved.

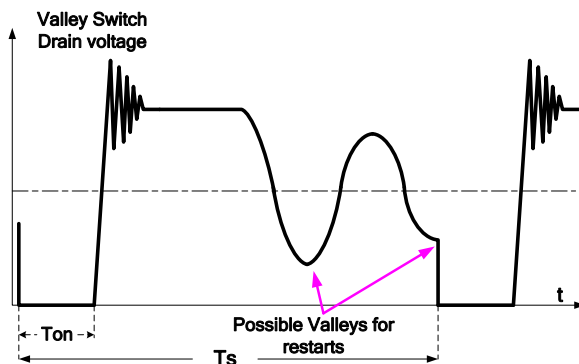
At no load or very light load conditions ($V_{FB} < V_{th1}$), the system operates in On-Bright's proprietary "extended burst mode". In the extended burst mode, the switching frequency at below 23KHz is minimized to avoid audio noise during operation.

Demagnetization Detection

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through DEM pin. This voltage features a flyback polarity. After the on time (determined by the CS voltage and FB voltage), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_p C_d}$, where L_p is the primary self inductance of primary winding of the transformer and C_d is the capacitance on the drain node.

The typical detection level is fixed at -50mV at the DEM pin. Demagnetization is recognized by

detection of a possible “valley” when the voltage at DEM is below -50mV in falling edge.

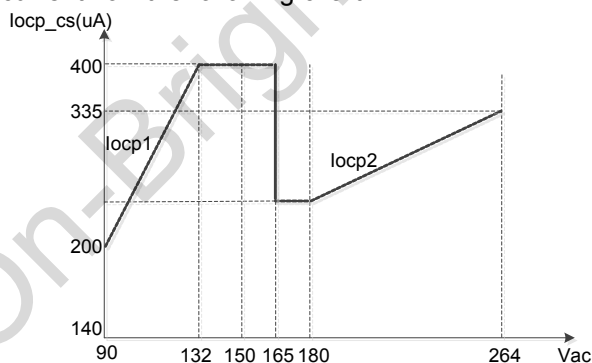


Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2710 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Vth_oc compensation

OB2710 offers adjustable Vth_oc compensation. A resistor can be series between the CS pin and the sense resistor. When FB voltage is over 3V, and gate is on, a current flow through the CS pin, a voltage drop generated on this resistor. The detected value by the sense resistor is regulated, and the OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. The compensating current flow the following chart:



At overload condition when FB input voltage exceeds power limit threshold value for more than Td_OLP, control circuit reacts to shut down the converter. It restarts when VCC voltage drops below UVLO limit.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The power MOSFET is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

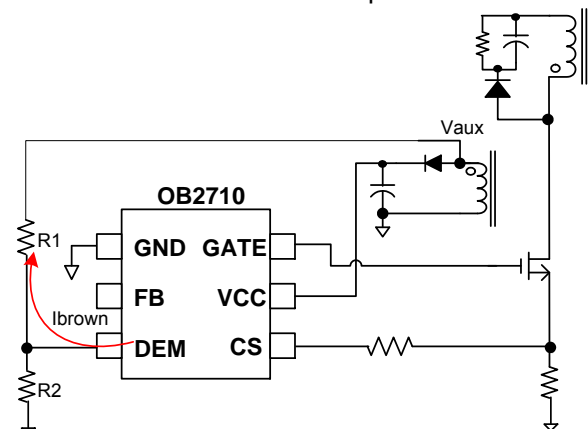
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Multiple Functions of Brown-in/Brown-out/line OVP and Output OVP

When the power MOSFET is turn on, the voltage on auxiliary windings is negative which make our Brown-in/Brown-out/line OVP protection feasible.



$$I_{AUX} = \frac{0.1}{R2} + \frac{0.1 - V_{AUX}}{R1}$$

R1: The resistor connected from DEM to AUX.

R2: The resistor connected from DEM to ground.

When system starts up, if $I_{AUX} < I_{brown_in}$, Brown-in auto-recovery protection is triggered after 2 Gate cycles debounce. When the system enters the

normal operation mode, if $I_{AUX} < I_{brown_out}$, Brown-out auto-recovery protection is triggered after 30ms debounce. As the same, when system starts up, if $I_{AUX} > I_{line_ovp}$, line_OVP protection is triggered after 2 Gate cycles debounce. In normal operation mode, Line OVP auto-recovery protection is triggered after 400ms debounce.

For output OVP detection, when Gate is off, V_{DEM} is equal to $V_{AUX} * R2 / (R1 + R2)$. If V_{DEM} is larger than 3V (typical), OVP auto-recovery protection is triggered after 8 Gate cycles debounce.

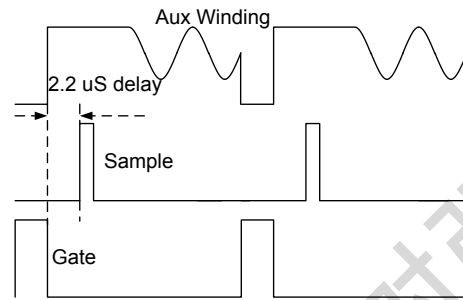
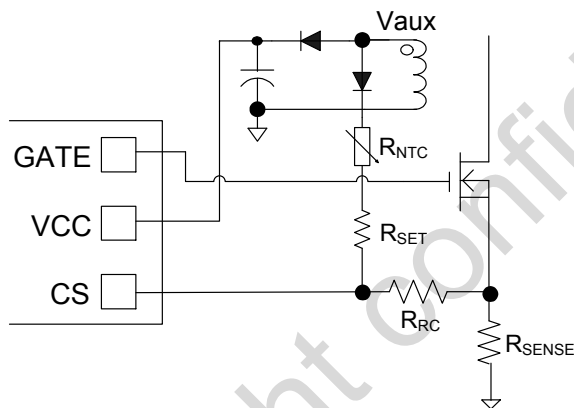
If V_{DEM} is smaller than 0.6V (typical), the internal counter starts counting subsequent SCP events more than 8 cycles, and the same time FB open > 12ms & $V_{CC} < 9.8V$, then trigger SCP protection with auto-recovery.

By selecting proper R1 and R2 resistance, output OVP level can be programmed.

$$V_{AUX} = \frac{3 * (R1 + R2)}{R2}$$

Output Over Temperature Protection

An output over voltage protection is implemented in the OB2710 by sensing the auxiliary voltage:



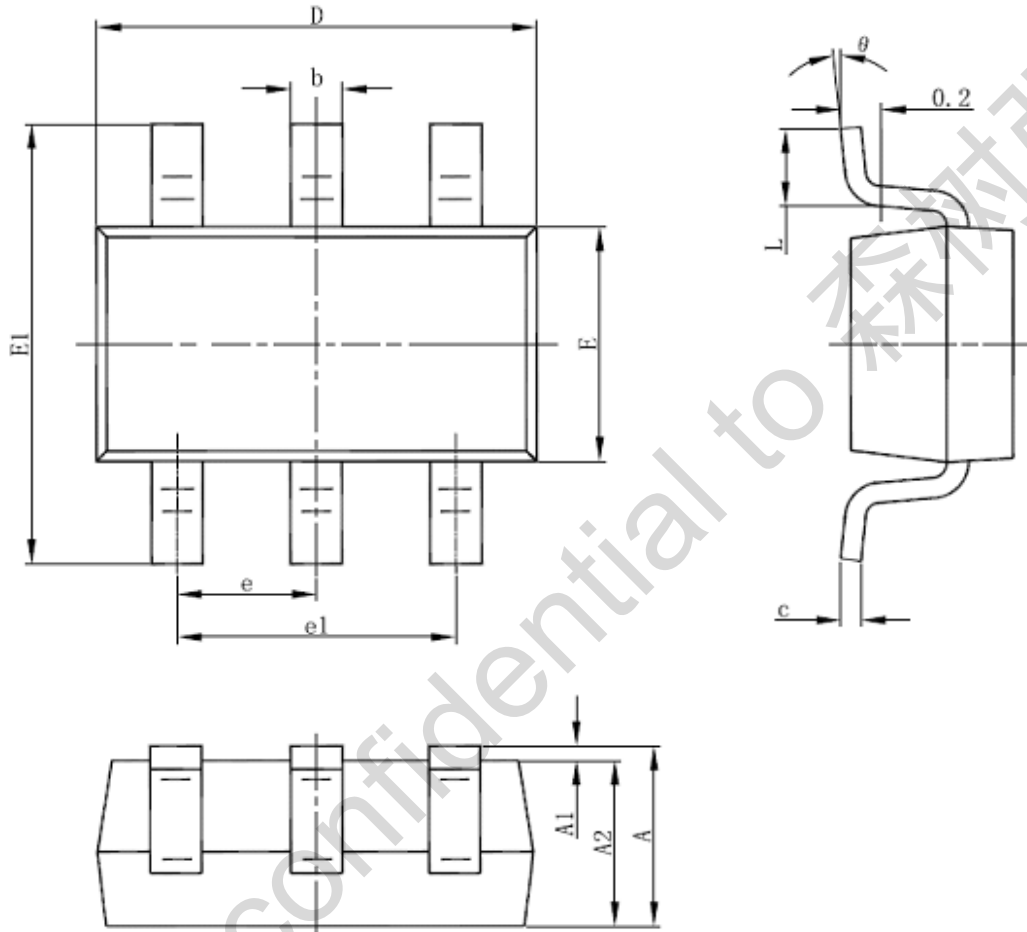
The auxiliary winding voltage is a well-defined replica of the output voltage. The OTP works by sampling the plateau voltage at CS pin during the flyback phase. OB2710 can sample this flat voltage level after a delay time to perform over temperature protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer.

The sampling voltage level is compared with internal threshold voltage 0.3V. If the sampling voltage exceeds the OTP trip level, an internal counter starts counting subsequent OTP events. If OTP events are detected in consecutive 60mS, the controller assumes a true OTP and the system enters into auto recovery.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VCC (UVLO), Over Temperature Protection (OTP), Brown-in/out/line OVP Protection, output SCP, VCC and output Over Voltage Protection (OVP).

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

IMPORTANT NOTICE

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