

### **GENERAL DESCRIPTION**

OB3398 is a primary side regulation off-line LED lighting controller which can achieve accurate LED current. It significantly simplifies LED lighting system design by eliminating the secondary side feedback circuitry. Proprietary Constant Voltage (CV) and Constant Current (CC) control is integrated as shown in the figure below.

The LED current (CC control) can be adjusted externally by the resistor Rs at CS pin.

OB3398 offers comprehensive protection coverage with auto-recovery features including Cycle-by-Cycle current limiting, VDD clamp and UVLO. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique

OB3398 is offered in SOT23-5 package.

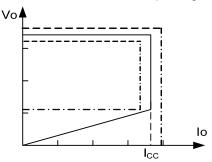


Fig.1. Typical CC/CV Curve

#### **FEATURES**

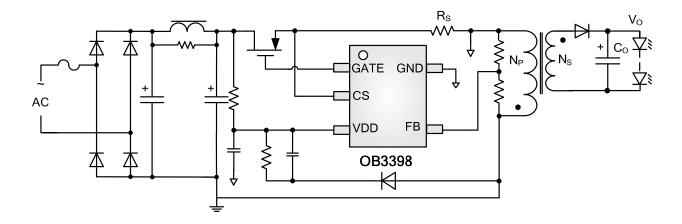
- High Precise Constant Current Regulation at Universal AC input
- Primary-side Sensing and Regulation Without TL431 and Opto-coupler
- Floating PSR control scheme with two transformer windings
- Adjustable Constant Current and Output Power Setting
- Built-in Primary winding inductance compensation
- Built-in Leading Edge Blanking (LEB)
- Cycle-by-Cycle Current Limiting
- VDD Under Voltage Lockout with Hysteresis (UVLO)
- Over temperature protection (OTP)
- VDD Clamp

### **APPLICATIONS**

Low Power AC/DC offline SMPS for

LED applications

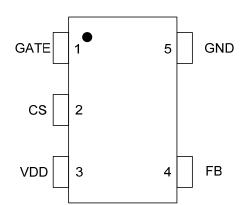
### **TYPICAL APPLICATION**





### **GENERAL INFORMATION**

# **Pin Configuration** SOT23-5.



**Ordering Information** 

Part Number	Description
OB3398MP	SOT23-5, Pb-free,T&R

**Package Dissipation Rating** 

Package	RθJA (℃/W)
SOT23-5	200

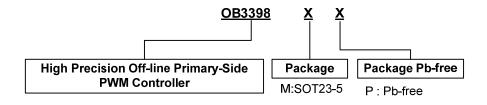
**Absolute Maximum Ratings** 

Absolute Maximum Natings					
Parameter	Value				
Gate Voltage	-0.3 to 25V				
VDD Voltage	-0.3 to V <sub>DD</sub> _clamp				
CS Input Voltage	-0.3 to 7V				
FB Input Voltage	-0.3 to 7V				
Min/Max Operating Junction Temperature T <sub>J</sub>	-40 to 150 ℃				
Operating Ambient Temperature T <sub>A</sub>	-40 to 85 ℃				
Min/Max Storage Temperature T <sub>stq</sub>	-55 to 150 ℃				
Lead Temperature (Soldering, 10secs)	260 ℃				

**Note:** Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

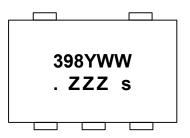
**Recommended Operating Condition** 

Symbol Paramete		Parameter	Range					
	VDD	VDD Supply Voltage	12 to 25 V					





# **Marking Information**



Y:Year Code WW:Week Code(01-52)

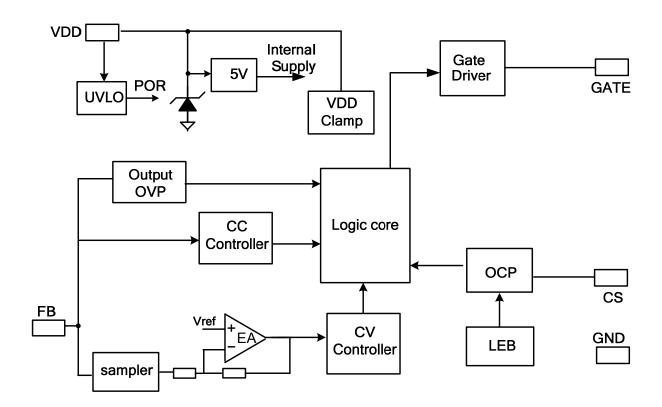
ZZZ: Lot code s: Internal code

## **TERMINAL ASSIGNMENTS**

Pin Num	Pin Name	I/O	Description
1	GATE	0	Gate driver output
2	CS	I	Current sense input.
3	VDD	Р	Power Supply
4	FB	I	Connected to resistor divider from primary winding or auxiliary winding to reflect output voltage.
5	GND	Р	Ground



# **BLOCK DIAGRAM**





# **ELECTRICAL CHARACTERISTICS**

(TA = 25°C, VDD=16V, if not otherwise noted)

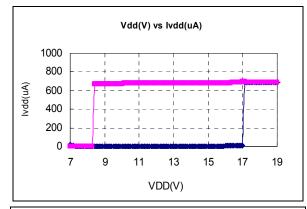
Parameter	Test Conditions	Min	Тур.	Max	Unit		
Supply Voltage (VDD) Section							
Startup Current	VDD=UVLO_OFF-1V		4	20	uA		
Operation Current	Operation supply current FB=1V, CS=0V, VDD= 20V	-	0.45	1	mA		
VDD Under Voltage Lockout Enter	VDD falling	7.3	8.3	9.3	٧		
VDD Under Voltage Lockout Exit	VDD rising	15.5	16.5	17.5	>		
Maximum VDD operation voltage	I <sub>DD</sub> =20mA		25		>		
se Input Section							
LEB time			500		ns		
Over current threshold		492	500	508	mV		
OCP Propagation delay			100		ns		
ection							
C Maximum frequency		103			KHz		
Minimum Toff			4.0		us		
Minimum frequency			103		Hz		
Frequency shuffling range			±7		%		
Error Amplifier section							
Reference voltage for EA		1.14	1.2	1.26	V		
DC gain of EA			40				
Load OVP threshold voltage			1.4		V		
Section				•			
Ouput low level @ VDD=14V, lo=5mA				1	V		
Ouput high level @ VDD=14V, lo=20mA		6			V		
Output clamp voltage			10		V		
Output rising time 1V~ 9V@ CL=500pF			95		ns		
Output falling time 9V~1V@ CL=500pF			50		ns		
On chip Over temperature Section							
Over temperature protection trigger point			135		$^{\circ}\!$		
Over temperature protection recovery point			120		$^{\circ}$		
	Startup Current  Operation Current  VDD Under Voltage Lockout Enter  VDD Under Voltage Lockout Exit  Maximum VDD operation voltage  se Input Section  LEB time  Over current threshold  OCP Propagation delay  Section  IC Maximum frequency  Minimum Toff  Minimum frequency  Frequency shuffling range  fier section  Reference voltage for EA  DC gain of EA  Load OVP threshold voltage  Section  Ouput low level @ VDD=14V, lo=5mA  Ouput high level @ VDD=14V, lo=20mA  Output clamp voltage  Output rising time 1V~ 9V@ CL=500pF  or temperature Section  Over temperature protection trigger point  Over temperature protection recovery	Startup Current  Operation Current  Operation Current  Operation supply current FB=1V, CS=0V, VDD= 20V  VDD Under Voltage Lockout Enter  VDD falling  Maximum VDD operation voltage  IDD=20mA  se Input Section  LEB time  Over current threshold  OCP Propagation delay  Section  IC Maximum frequency  Minimum Toff  Minimum frequency  Frequency shuffling range  Tier section  Reference voltage for EA  DC gain of EA  Load OVP threshold voltage  Section  Ouput low level @ VDD=14V, lo=5mA  Output clamp voltage  Output rising time 1V~ 9V@ CL=500pF  Output falling time 9V~1V@ CL=500pF  Over temperature protection trigger point  Over temperature protection recovery	Startup Current  Operation Current  Operation Supply current FB=1V, CS=0V, VDD=20V  VDD Under Voltage Lockout Enter  VDD falling  7.3  VDD Under Voltage Lockout Exit  VDD rising  15.5  Maximum VDD operation voltage  IDD=20mA  See Input Section  LEB time  Over current threshold  OCP Propagation delay  Section  IC Maximum frequency  Inimum Toff  Minimum Toff  Minimum frequency  Frequency shuffling range  Tier section  Reference voltage for EA  DC gain of EA  Load OVP threshold voltage  Section  Ouput low level @ VDD=14V, lo=5mA  Output clamp voltage  Output rising time 1V~ 9V@ CL=500pF  Output falling time 9V~1V@ CL=500pF  Over temperature protection trigger point  Over temperature protection recovery	Startup Current	Startup Current   VDD=UVLO_OFF-1V   4   20		

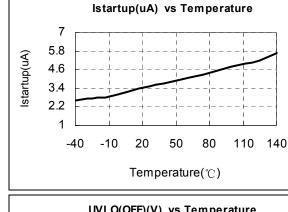
# Note:

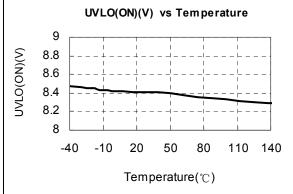
<sup>1.</sup> Freq\_Max indicates IC internal maximum clock frequency. In system application, the maximum operation frequency of 103KHz nominal occurs at maximum output power or the transition point from CV to CC.

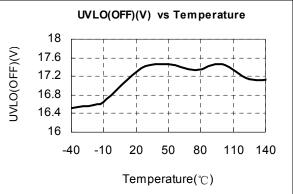


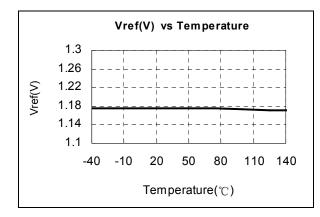
#### **CHARACTERIZATION PLOTS**

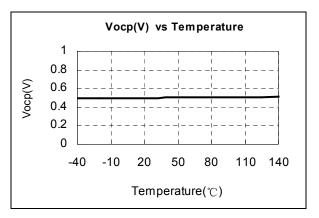














#### OPERATION DESCRIPTION

OB3398 is a cost effective PWM controller optimized for off-line LED lighting applications. Based on floating flyback converter topology working in DCM mode, it operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. Proprietary built-in CC control can achieve high precision LED current meeting LED lighting application requirements.

### Startup Current and Start up Control

Startup current of OB3398 is designed to be very low so that VDD could be charged up above UVLO threshold and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss in application.

#### **Operating Current**

The Operating current of OB3398 is as low as 0.45mA(Typ.). Typical good efficiency is achieved with the low operating current together with 'Multi-mode' control features.

#### **Principle of CC Operation**

To support OB3398 proprietary CC control, system needs to be designed in DCM mode for flyback system (Refer to Typical Application Diagram on page1). The LED output current  $I_{\text{LED}}$  is given by:

$$I_{LED} = \frac{1}{2} L_P \cdot F_{SW} \cdot I_{PK}^2 \cdot \eta / V_O \tag{1}$$

Where Lp indicates the inductance of primary winding, lpk is the peak current of primary winding.

Refer to the equation 1, the change of the primary winding inductance results in the change of the constant output current. To compensate the change from variations of primary winding inductance, the switching frequency is locked by an internal loop such that the switching frequency is

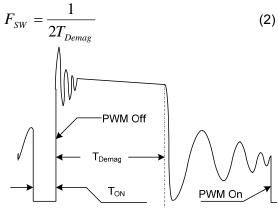


Figure.1 Primary voltage waveform

Since  $T_{\text{Demag}}$  is inversely proportional to the inductance, as a result, the product Lp and fsw is constant, thus output current will not change as primary winding inductance changes. Up to  $\pm 7\%$  variation of the primary winding inductance can be compensated.

The output LED current is

$$I_{LED} = \frac{1}{4} \cdot N \cdot \frac{V_{th\_oc}}{R_c} \tag{3}$$

Where N is the ratio of transformer between primary winding and secondary winding.

#### Adjustable CC point and Output Power

In OB3398, the CC point and maximum output power can be externally adjusted by external current sense resistor Rs at CS pin as illustrated in Typical Application Diagram. The output power is adjusted through CC point change. The larger Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.2.

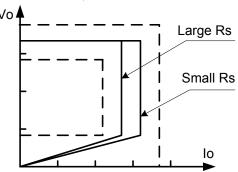


Figure.2 Adjustable output power by changing Rs

#### Operation switching frequency

The switching frequency of OB3398 is adaptively controlled according to the load conditions and the operation modes. No external frequency setting components are required. The operation switching frequency at maximum output power is set to 103K Hz internally.

For flyback operating in DCM, The maximum output power is given by

$$P_{O\max} = \frac{1}{2} \eta L_P F_{SW} I_{pk}^2$$
 (4)

Where Lp indicate the inductance of primary winding and lpk is the peak current of primary winding.

The principle of CC operation sets the product *Lp* and *fsw* to be a constant, thus the maximum output power and constant current in CC mode will not change as primary winding inductance changes. Up to +/-7% variation of the primary winding inductance can be compensated.



#### CV / OVP Mode

When LED string is open, an output voltage condition is monitored independently by the voltage at FB pin. During normal operation, the voltage at FB pin is regulated at 1.2V (typ.), with dummy load over Pmin.

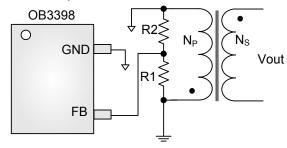


Figure.3 FB Section Circuit

$$V_{OUT} = \frac{N_s}{N_p} \times \frac{R1 + R2}{R2} \times V_{ref\_CV}$$

R1 —Resistor connected between the FB pin and the input capacitor GND, the value suggested is 330Kohms~1Mohms

R2 —Resistor connected between the FB pin and the GND pin of IC, the value suggested is 5Kohms~15Kohms

$$P_{\min} = \frac{1}{2} \times \left(\frac{Vth \_oc}{R_{CS}}\right)^2 F_{\min} L_{priamry}$$

 $V_{th\_oc}$  — Over current protection threshold voltage

 $F_{min}$  — Minimum switching frequency, which is 103Hz (typ.)

If the dummy load is less than  $P_{\text{min}}$ , the output voltage rises up. If the voltage at FB pin exceeds a threshold of approximately 1.4V (typical), the over-voltage protection function is activated and the switching is turned off immediately.

$$V_{OVP} = \frac{N_s}{N_p} \times \frac{R1 + R2}{R2} \times V_{vth\_OVP}$$

#### **CC Line Regulation**

Adjust the R1 for better CC line regulation, while driving different type MOSFET. The larger MOSFET, the smaller R1 needed. R1 allow the change from 330K to 1M ohms to cover all the applications. If the resistance is too large, it causes the interference due to the floating ground, too small resistance results the efficiency decreased at HV AC line.

### Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in OB3398. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

#### **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB3398. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on state so that the external RC filtering on sense input is no longer needed. The PWM duty cycle is determined by the current sense input voltage and the EA output voltage.

#### **Protection Control**

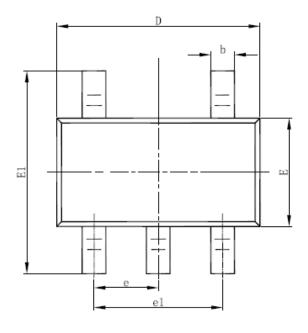
Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), VDD clamp, on-chip OTP, and Under Voltage Lockout on VDD (UVLO).

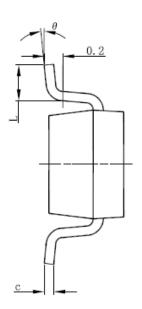
VDD is supplied by transformer primary winding output. The output of OB3398 is shut down when VDD drops below UVLO (ON) limit and the power converter enters power on start-up sequence thereafter.

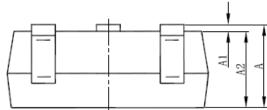


# **PACKAGE MECHANICAL DATA**

5-Pin Plastic SOT (SOT23-5)







Symbol	Dimensions In Millimeters		Dimensions In Inches		
Syllibol	Min	Max	Min	Max	
Α	1.000	1.450	0.039	0.057	
A1	0.000	0.150	0.000	0.006	
A2	0.900	1.300	0.035	0.051	
b	0.300	0.500	0.012	0.020	
С	0.080	0.220	0.003	0.009	
D	2.800	3.020	0.110	0.119	
E	1.500	1.726	0.059	0.068	
E1	2.600	3.000	0.102	0.118	
е	0.950	(BSC)	0.037	(BSC)	
e1	1.800	2.000	0.071	0.079	
L	0.300	0.600	0.012	0.024	
θ	0°	8°	0°	8°	



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