GENERAL DESCRIPTION

OB3399 is a primary side regulation off-line LED lighting controller which can achieve accurate LED current. It significantly simplifies LED lighting system design by eliminating the secondary side feedback circuitry. Proprietary Constant Voltage (CV) and Constant Current (CC) control is integrated as shown in the figure below.

The LED current (CC control) can be adjusted externally by the resistor Rs at CS pin.

OB3399 offers comprehensive protection coverage with auto-recovery features including Cycle-by-Cycle current limiting, VDD clamp and UVLO. Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique.
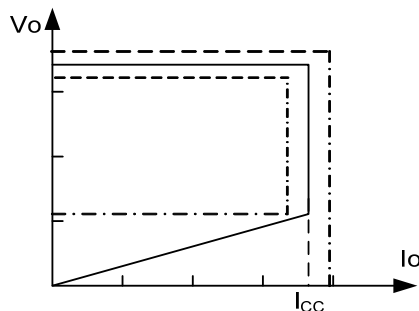
OB3399 is offered in SOT23-6 package.

Fig.1. Typical CC/CV Curve

FEATURES

- High Precise Constant Current Regulation at Universal AC input
- Primary-side Sensing and Regulation Without TL431 and Opto-coupler
- Adjustable Constant Current and Output Power Setting
- Adjustable Constant Voltage Load Compensation
- Built-in Primary Winding Inductance Compensation
- Built-in Leading Edge Blanking (LEB)
- Cycle-by-Cycle Current Limiting
- VDD Under Voltage Lockout with Hysteresis (UVLO)
- Latched over temperature protection (OTP)
- VDD Clamp

APPLICATIONS

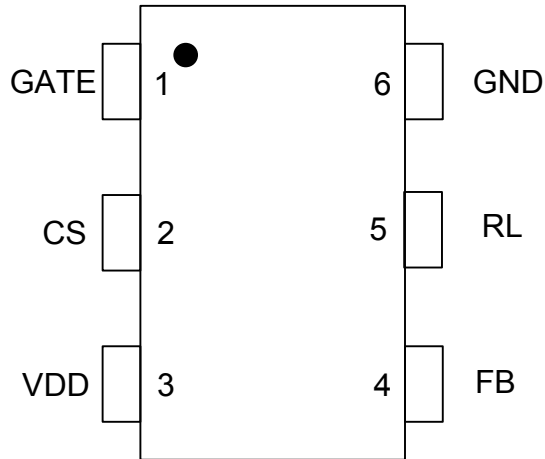Low Power AC/DC offline SMPS for
- LED applications

TYPICAL APPLICATION

Confidential *Preliminary Datasheet*
OB_DOC_DS_339903
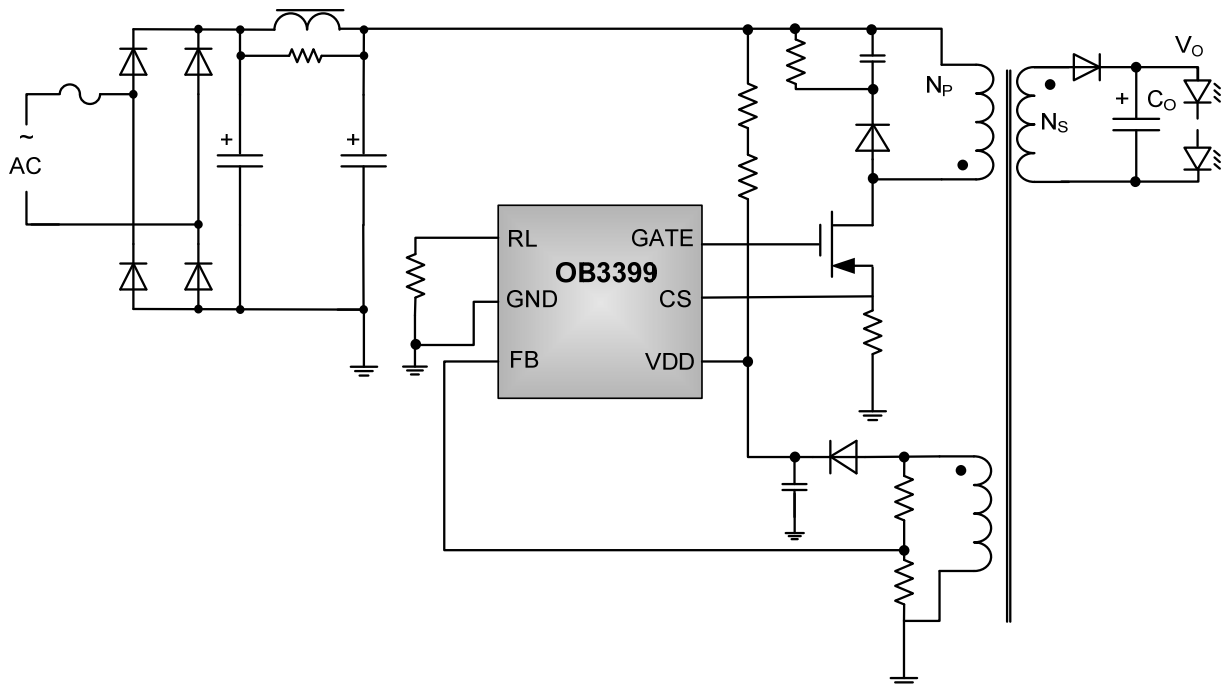
GENERAL INFORMATION

Pin Configuration
The pin map is shown as below for SOT23-6.

GATE	1			6	GND
CS	2			5	RL
VDD	3			4	FB

Ordering Information

Part Number	Description
OB3399MP	SOT23-6, Halogen-free, T&R

Package Dissipation Rating

Package	RθJA (℃/W)
SOT23-6	200

Absolute Maximum Ratings

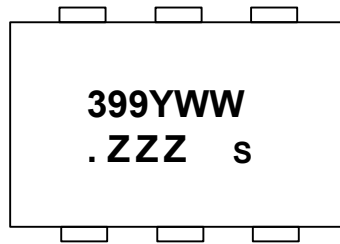| Parameter	Value
VDD Voltage	-0.3 to $V_{DD\_}$ clamp
Gate Voltage	-0.3 to 25V
CS Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
RL input voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Operating Ambient Temperature T_A	-40 to 85 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Condition

Symbol	Parameter	Range
VDD	VDD Supply Voltage	12 to 25 V

OB3399   X   X

High Precision Offline Primary-Side PWM Controller	Package	Green Package

M: SOT23-6

P : Green (Halogen-free)
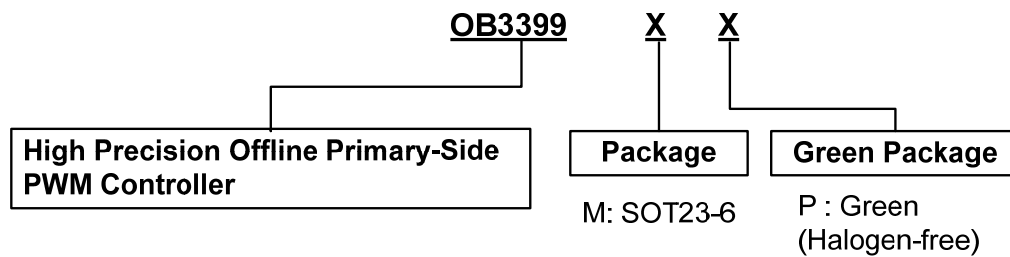
Marking Information

```
399YWW
.ZZZ   s
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Y:Year Code
WW:Week Code(01-52)
ZZZ: Lot code
S: Internal code

TERMINAL ASSIGNMENTS for OB3399

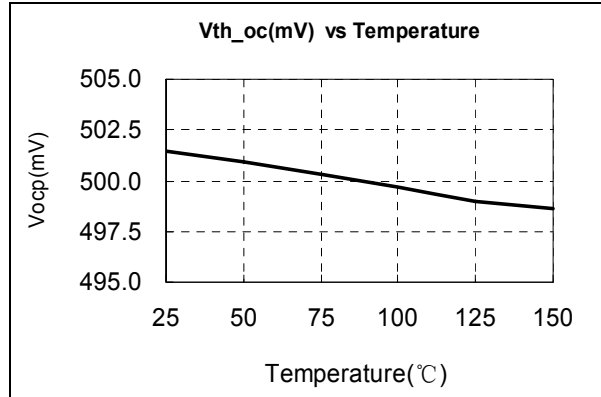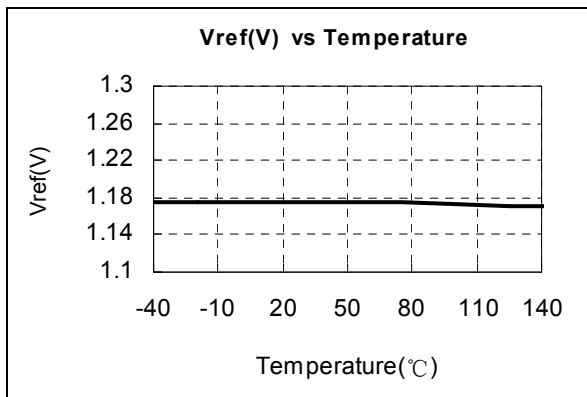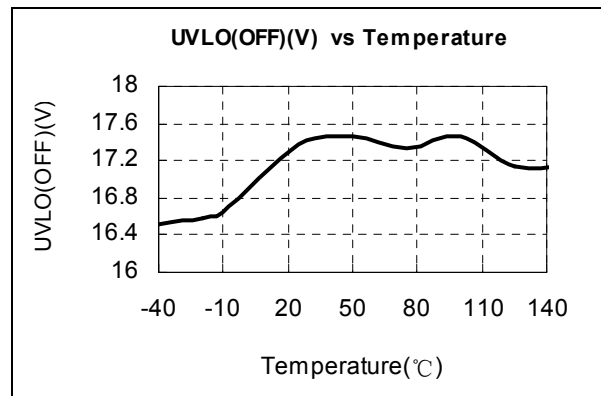| Pin Num	Pin Name	I/O	Description
1	GATE	O	Gate driver output
2	CS	I	Current sense input.
3	VDD	P	Power Supply
4	FB	I	Connected to resistor divider from primary winding or auxiliary winding to reflect output voltage.
5	RL	IO	Load regulation configuration pin
6	GND	P	Ground

BLOCK DIAGRAM
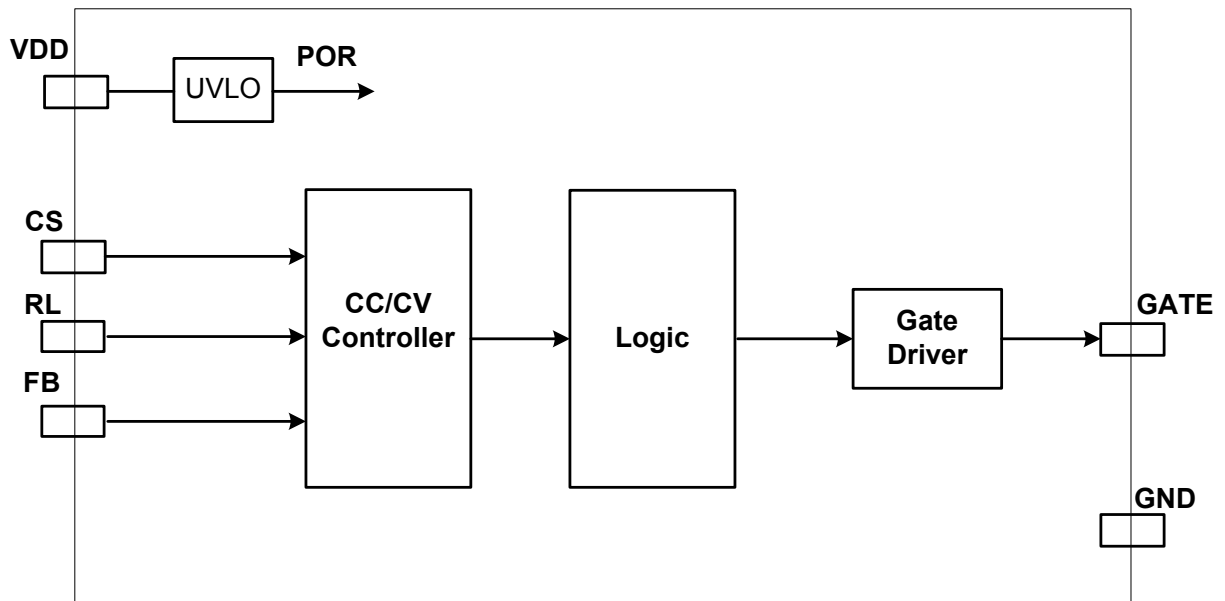
ELECTRICAL CHARACTERISTICS

(TA = 25℃, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD) Section						
$I_{startup}$	Startup Current	VDD=UVLO_OFF-1V		4	20	uA
$I_{DD\,op}$	Operation Current	Operation supply current FB=1V, CS=0V, VDD= 20V		0.65	1	mA
UVLO(ON)	VDD Under Voltage Lockout Enter	VDD falling	7.3	8.3	9.3	V
UVLO(OFF)	VDD Under Voltage Lockout Exit	VDD rising	15.5	16.5	17.5	V
V_{DD}_clamp	Maximum VDD operation voltage	I_{DD}=20mA		25		V
Current Sense Input Section						
TLEB	Leading edge blanking time			500		ns
Vth_oc	Over current threshold		492	500	508	mV
Td_oc	Over current protection propagation delay			100		ns
Frequency Section						
Freq_Max[Note 1]	IC Maximum frequency		103			KHz
Toff_min	Minimum Toff			4.0		us
F_min	Minimum frequency			1		KHz
Error Amplifier section						
Vref	Reference voltage for EA		1.164	1.2	1.236	V
Gain	DC gain of EA			40		
Vth_OVP	Load OVP threshold voltage			1.4		V
On chip Over temperature Section						
T_otp	latched over temperature protection trigger point			155		℃
Gate Driver Section						
VOL	Output low level @ VDD=14V, Io=5mA				1	V
VOH	Output high level @ VDD=14V, Io=20mA		6			V
V_clamping	Output clamp voltage			10		V
T_r	Output rising time 1V~ 9V@ CL=500pF			95		ns
T_f	Output falling time 9V~1V@ CL=500pF			50		ns

Note:

Freq_Max indicates IC internal maximum clock frequency. In system application, the maximum operation frequency of 103KHz nominal occurs at maximum output power or the transition point from CV to CC.

CHARACTERIZATION PLOTS

Vdd(V) vs Ivdd(uA)

Istartup(uA) vs Temperature

UVLO(ON)(V) vs Temperature

UVLO(OFF)(V) vs Temperature

Vref(V) vs Temperature

Vth_oc(mV) vs Temperature
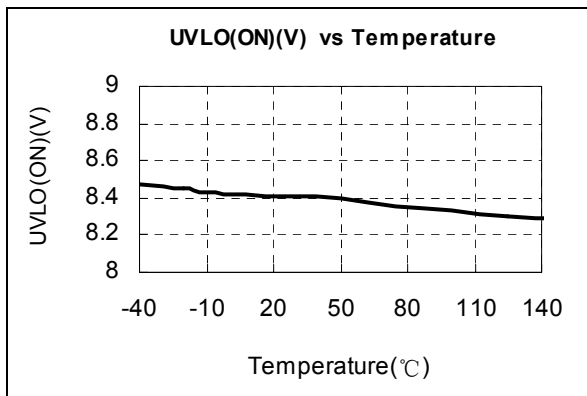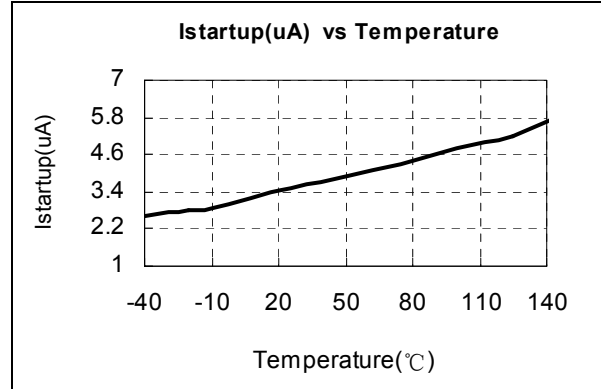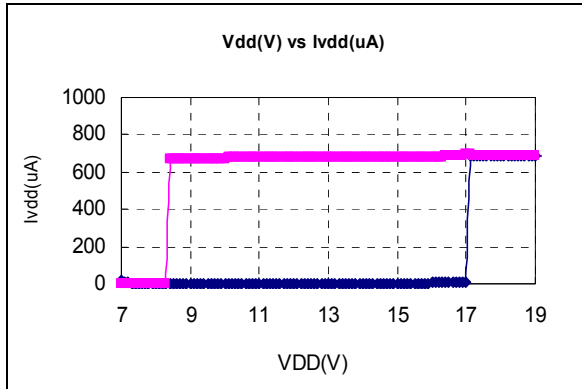
OPERATION DESCRIPTION

OB3399 is a cost effective PWM controller optimized for off-line LED lighting applications. Based on flyback converter topology working in DCM mode, It operates in primary side sensing and regulation, thus opto-coupler and TL431 are not required. Proprietary built-in CC control can achieve high precision LED current meeting LED lighting application requirements.

Startup Current and Start up Control

Startup current of OB3399 is designed to be very low so that VDD could be charged up above UVLO threshold and starts up quickly. A large value startup resistor can therefore be used to minimize the power loss in application.

Operating Current

The Operating current of OB3399 is as low as 0.45mA(Typ.). Typical good efficiency is achieved with the low operating current together with 'Multi-mode' control features.

Principle of CC Operation

To support OB3399 proprietary CC control, system needs to be designed in DCM mode for flyback system (Refer to Typical Application Diagram on page1). The LED output current I_{LED} is given by:

$$I_{LED} = \frac{1}{2} L_P \cdot F_{SW} \cdot I_{PK}^2 \cdot \eta \Big/ V_O \qquad (1)$$

Where Lp indicates the inductance of primary winding, Ipk is the peak current of primary winding.

Refer to the equation 1, the change of the primary winding inductance results in the change of the constant output current. To compensate the change from variations of primary winding inductance, the switching frequency is locked by an internal loop such that the switching frequency is
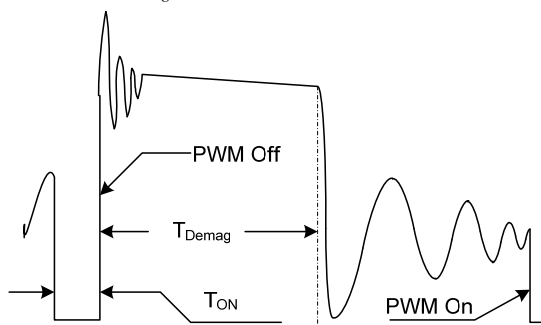
$$F_{SW} = \frac{1}{2T_{Demag}} \qquad (2)$$

Figure.1 Primary voltage waveform

Since T_{Demag} is inversely proportional to the inductance, as a result, the product *Lp* and *fsw* is constant, thus output current will not change as primary winding inductance changes. Up to $\pm 7\%$ variation of the primary winding inductance can be compensated.

The output LED current is

$$I_{LED} = \frac{1}{4} \cdot N \cdot \frac{V_{th\_oc}}{R_s} \qquad (3)$$

Where N is the ratio of transformer between primary winding and secondary winding.

Adjustable CC point and Output Power

In OB3399, the CC point and maximum output power can be externally adjusted by external current sense resistor Rs at CS pin as illustrated in Typical Application Diagram.   The output power is adjusted through CC point change.   The larger Rs, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.2.
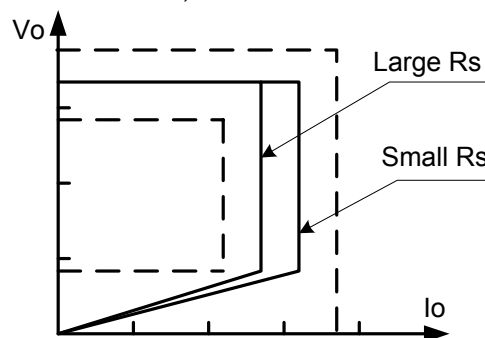

Figure.2 Adjustable output power by changing Rs

Operation switching frequency

The switching frequency of OB3399 is adaptively controlled according to the load conditions and the operation modes. No external frequency setting components are required. The operation switching frequency at maximum output power is set to 103K Hz internally.

For flyback operating in DCM, The maximum output power is given by

$$P_{O\max} = \frac{1}{2} \eta L_P F_{SW} I_{pk}^2 \qquad (4)$$

Where Lp indicate the inductance of primary winding and Ipk is the peak current of primary winding.

The principle of CC operation sets the product *Lp* and *fsw* to be a constant, thus the maximum output power and constant current in CC mode will not change as primary winding inductance changes. Up to +/-7% variation of the primary winding inductance can be compensated.

CV/OVP Mode

When LED string is open, an output voltage condition is monitored independently by the voltage at FB pin. During normal operation, the voltage at FB pin is regulated at 1.2V (typ.), with dummy load over P_{min}.
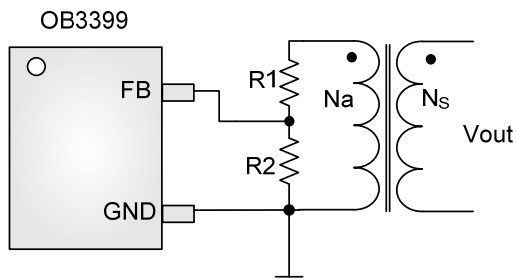
OB3399

Figure.3 FB Section Circuit

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R1 + R2}{R2} \times V_{ref\_CV}$$

R1 —the value suggested is 50~200Kohms
R2 —the value suggested is 3~10Kohms

$$P_{min} = \frac{1}{2} \times \left(\frac{Vth\_oc}{R_{CS}} \right)^2 F_{min} L_{priamry}$$

V_{th_oc} — Over current protection threshold voltage

F_{min} — Minimum switching frequency, which is 1KHz (typ.)

If the dummy load is less than P_{min}, the output voltage rises up. If the voltage at FB pin exceeds a threshold of approximately 1.4V (typical), the over-voltage protection function is activated and the switching is turned off immediately.

$$V_{OVP} = \frac{N_S}{N_A} \times \frac{R1 + R2}{R2} \times V_{vth\_OVP}$$

CC Line Regulation

Adjust the R1 for better CC line regulation, while driving different type MOSFET. The larger MOSFET, the smaller R1 needed. R1 allow the change from 50K to 200K ohms to cover all the applications. If the resistance is too large, it causes the interference due to the floating ground, too small resistance results the efficiency decreased at HV AC line.

CV Load Compensation

OB3399 features load compensation function to achieve good CV load regulation. It can be programmed by adjusting the resistance of R3 at RL pin to compensate the output voltage deviation as shown in Figure 4.

The percentage of maximum compensation is

$$\frac{\Delta V}{Vout} = \frac{(1/R3) \times (R1//R2) \times 10^{-6}}{1.2} \times 100\%$$

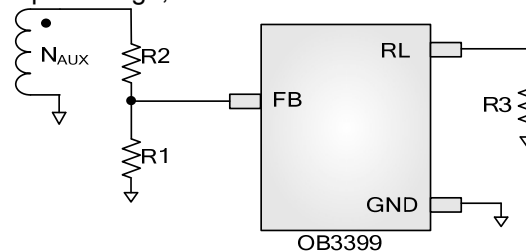ΔV is load compensation voltage and Vout is output voltage;

Figure.4 CV load compensation

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB3399. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET. The PWM duty cycle is determined by the current sense input voltage and the EA output voltage.

Protection Control

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), VDD clamp, on-chip OTP, and Under Voltage Lockout on VDD (UVLO).

Latched Over Temperature Protection

Over temperature protection is offered in OB3399. When temperature of the device rises over 155℃ (typical), the switching frequency will decrease to half. And the state will be kept until the device restarts.

VDD is supplied by transformer primary winding output. The output of OB3399 is shut down when VDD drops below UVLO (ON) limit and the power converter enters power on start-up sequence thereafter.

PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS
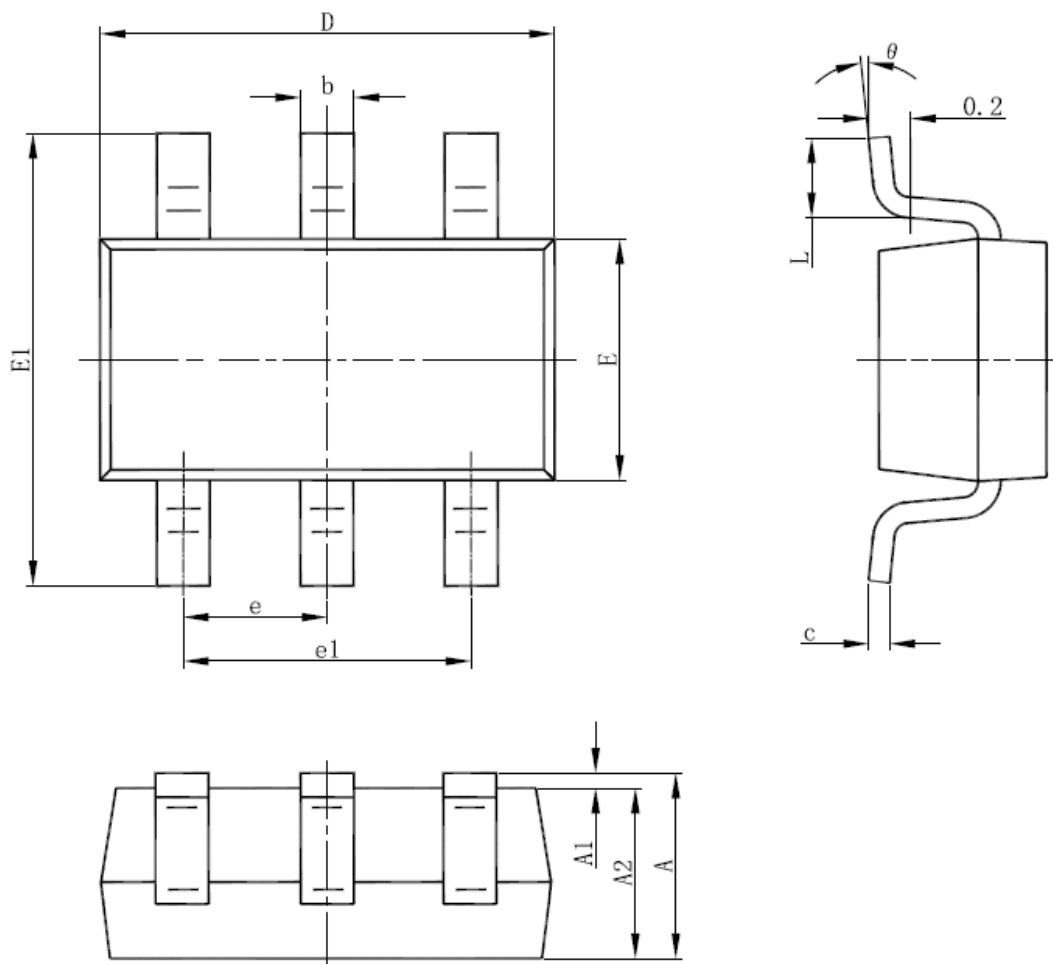
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0º	8º	0º	8º

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