Product List

OB38S003W20,

Description

The OB38S003 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 8KB embedded program memory, and executes all ASM51 instructions fully compatible with MCS-51.

OB38S003 contains 512B on-chip RAM, up to 18 GPIOs (20L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB38S003 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB38S003 ihhkL
YWW
i: process identifier { W = 2.4V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: Year Code
WW: Week Code (01-52)

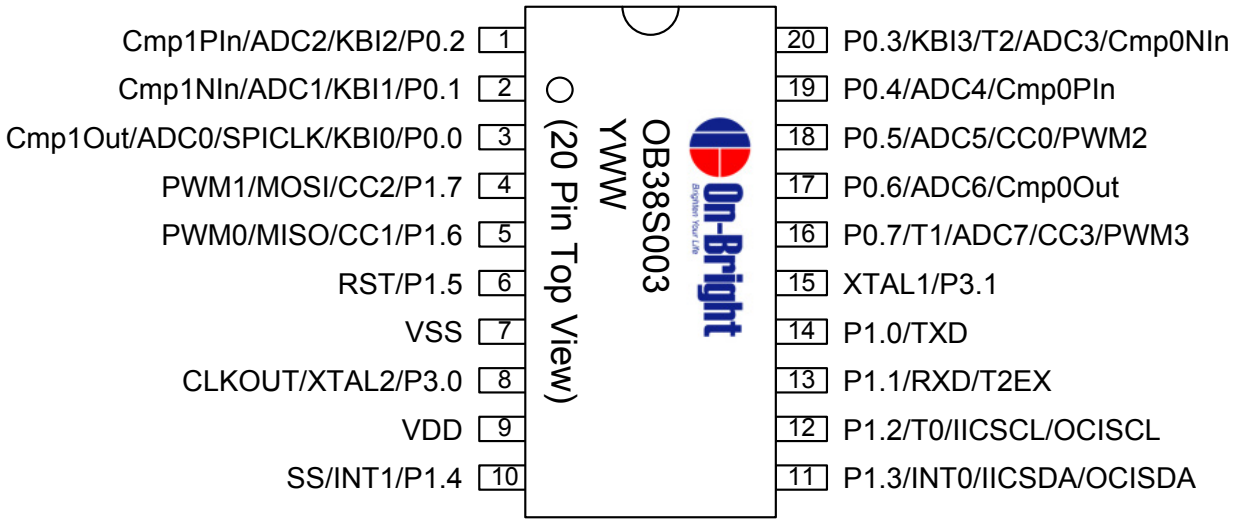
Postfix	Package
E	TSSOP(173mil)

Features

- Operating Voltage: 2.4V ~ 5.5V
- High speed architecture of 1 clock/machine cycle runs up to 16MHz.
- 1~8T can be switched on the fly.
- Instruction-set compatible with MCS-51.
- 16MHz Internal RC oscillator, with programmable clock divider
- 8KB on-chip program memory.
- 512B RAM as standard 8052,
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- One serial peripheral interfaces in full duplex mode.
- Additional Baud Rate Generator
- Three 16-bit Timer/Counters. (Timer 0,1,2）
- 8 ~18 GPIOs(10L ~ 20L package)
- External interrupt 0,1 with four priority levels
- Programmable watchdog timer.
- One IIC interface. (Master/Slave mode)
- One SPI interface (Master/Slave mode)
- 4-channel PWM
- 4-channel 16-bit PCA for compare(PWM) / capture / reload functions
- 8-channel 12-bit analog-to-digital converter (ADC)
- CMP x1 Set (2 devices)
- ISP/IAP/ICP functions.
- ISP service program space configurable in N*128 byte (N=0 to 8) size.
- EEPROM function.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- Keyboard interface (KBI) for four more interrupts.
- LVI/LVR (LVR deglitch 500ns)
- IO PAD ESD over 4KV
- Enhance user code protection.
- Power management unit for IDLE and power down modes.

Pin Configuration

20 Pin TSSOP



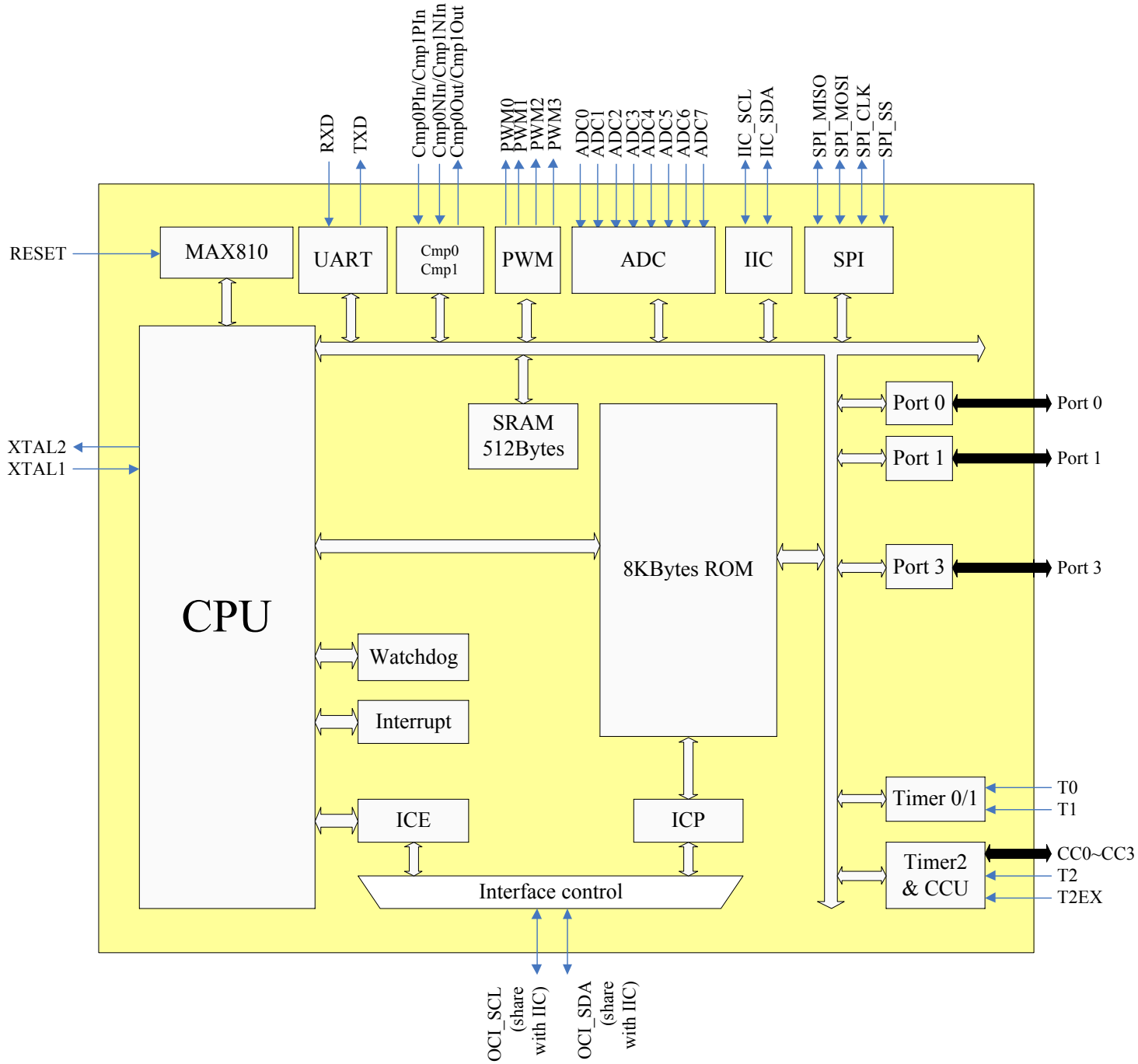
Notes：

(1) The pin Reset/P1.5 factory default is GPIO (P1.5). User can configure it to Reset by a programmer.

(2) To avoid accidentally entering ISP-Mode(refer to section 18.4), care must be taken not asserting pulse signal at RXD P1.1 during power-up while P1.6 are set to high.

(3) To apply ICP function, OSI_SDA/P1.3 and OCI_SCL/P1.2 must be set to Bi-direction mode if they are configured as GPIO in system.

Block Diagram



Pin Description

20L	Symbol	I/O	Description
1	P0.2/KBI2/ADC2/ CMP1PIn	I/O	Bit 2 of port 0 & KBI interrupt 2 & ADC input channel 2 & Cmp1 Positive Input
2	P0.1/KBI1/ADC1/ CMP1NIn	I/O	Bit 1 of port 0 & KBI interrupt 1 & ADC input channel 1 & Cmp1 Negative Input
3	P0.0/KBI0/SPICLK/ADC0/ CMP1Out	I/O	Bit 0 of port 0 & KBI interrupt 0 & SPI interface Clock pin & ADC input channel 0 & Cmp1 output
4	P1.7/CC2/MOSI/PWM1	I/O	Bit 7 of port 1 & Timer 2 compare/capture Channel 2 & SPI interface Serial Data Master Output or Slave Input pin & PWM Channel 1
5	P1.6/CC1/MISO/PWM0	I/O	Bit 6 of port 1 & Timer 2 compare/capture Channel 1 & SPI interface Serial Data Master Input or Slave Output pin & PWM Channel 0
6	P1.5/RST	I/O	Bit 5 of port 1 & Reset pin
7	VSS	I	Power supply
8	P3.0/XTAL2/CLKOUT	I/O	Bit 0 of port 3 & Crystal output & Clock Output
9	VDD	I	Power supply
10	P1.4/INT1/SS	I/O	Bit 4 of port 1 & External interrupt 1 & SPI interface Slave Select pin
11	P1.3/INT0/IICSDA/OCISDA	I/O	Bit 3 of port 1 & External interrupt 0 & IIC SDA pin & On-Chip Instrumentation Command and data I/O pin synchronous to OCI_SCL in ICE and ICP functions
12	P1.2/T0/IICSCL/OCISCL	I/O	Bit 2 of port 1 & Timer 0 external input & IIC SCL pin & On-Chip Instrumentation Clock I/O pin of ICE and ICP functions
13	P1.1/RXD/T2EX	I/O	Bit 1 of port 1 & Serial interface channel 0 receive/transmit data & Timer 2 capture trigger
14	P1.0/TXD	I/O	Bit 0 of port 1 & Serial interface channel 0 transmit data or receive clock in mode 0
15	P3.1/XTAL1	I/O	Bit 1 of port 3 & Crystal input
16	P0.7/T1/ADC7/CC3/PWM3	I/O	Bit 7 of port 0 & Timer 1 external input & ADC input channel 7& Timer 2 compare/capture Channel 3& PWM Channel 3
17	P0.6/ADC6/CMP0Out	I/O	Bit 6 of port 0 & ADC input channel 6 & Cmp0 Output
18	P0.5/ADC5/CC0/PWM2	I/O	Bit 5 of port 0 & ADC input channel 5 & Timer 2 compare/capture Channel 0& PWM Channel 2
19	P0.4/ADC4/CMP0PIn	I/O	Bit 4 of port 0 & ADC input channel 4 & Cmp0 Positive Input
20	P0.3/KBI3/T2/ADC3/CMP0NIn	I/O	Bit 3 of port 0 & KBI interrupt 3 & Timer 2 external input clock & ADC input channel 3 & Cmp0 Negative Input

Special Function Register (SFR)

A map of the Special Function Registers is shown as below：

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IICS	IICCTL	IICA1	IICA2	IICRWD	IICEBT	CMP0CON	CMP1CON	FF
F0	B	SPIC1	SPIC2	SPITXD	SPIRXD	SPIS	OPPIN	TAKEY	F7
E8				ISPFDH			INTDEG	ADCSH	EF
E0	ACC	ISPFAH	ISPFAL	ISPFDL	ISPFC	ENHIT	LVC	SWRES	E7
D8		PFCON	P3M0	P3M1					DF
D0	PSW	CCEN2	P0M0	P0M1	P1M0	P1M1			D7
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2	PWMMDH	PWMMDL	CF
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	C7
B8	IEN1	IP1	SRELH		PWMD0H	PWMD0L	PWMD1H	PWMD1L	BF
B0	P3	PWMD2H	PWMD2L	PWMD3H	PWMD3L	PWMC	WDTC	WDTK	B7
A8	IEN0	IP0	SRELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	AF
A0		RSTS							A7
98	SCON	SBUF	IEN2						9F
90	P1	AUX		KBLS	KBE	KBF	KBD	IRCON2	97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	8F
80	P0	SP	DPL	DPH	DPL1	DPH1		PCON	87
Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex

Note: Special Function Registers reset values and description for OB38S003

Register	Location	Reset value	Description
SYSTEM			
SP	81h	07h	Stack Pointer
ACC	E0h	00h	Accumulator
PSW	D0h	00h	Program Status Word
B	F0h	00h	B Register
DPL	82h	00h	Data Pointer 0 low byte
DPH	83h	00h	Data Pointer 0 high byte
DPL1	84h	00h	Data Pointer 1 low byte
DPH1	85h	00h	Data Pointer 1 high byte
AUX	91h	00h	Auxiliary register
PCON	87h	00h	Power Control
CKCON	8Eh	10h	Clock control register
INTERRUPT & PRIORITY			
IRCON	C0h	00h	Interrupt Request Control Register
IRCON2	97h	00h	Interrupt Request Control Register 2
IEN0	A8h	00h	Interrupt Enable Register 0
IEN1	B8h	00h	Interrupt Enable Register 1

Register	Location	Reset value	Description
IEN2	9Ah	00h	Interrupt Enable Register 2
IP0	A9h	00h	Interrupt Priority Register 0
IP1	B9h	00h	Interrupt Priority Register 1
ENHIT	E5h	07h	ENHance Interrupt Type Register
INTDEG	EEh	00h	External Interrupt Deglitch Register
KBI			
KBLS	93h	00h	Keyboard level selector Register
KBE	94h	00h	Keyboard input enable Register
KBF	95h	00h	Keyboard interrupt flag Register
KBD	96h	00h	Keyboard interface De-bounce control register
UART			
PCON	87h	00h	Power Control
AUX	91h	00h	Auxiliary register
SCON	98h	00h	Serial Port, Control Register
SBUF	99h	00h	Serial Port, Data Buffer
SRELL	AAh	00h	Serial Port, Reload Register, low byte
SRELH	BAh	00h	Serial Port, Reload Register, high byte
PFCON	D9h	00h	Peripheral Frequency control register
ADC			
ADCC1	ABh	00h	SADC Control 1 Register
ADCC2	ACh	0Fh	SADC Control 2 Register
ADCDH	ADh	00h	SADC data high byte
ADCDL	AEh	00h	SADC data low byte
ADCCS	AFh	00h	SADC clock select
ADCSH	EFh	00h	SADC Sample and Hold Time
WDT			
RSTS	A1h	00h	Reset status register
WDTC	B6h	04h	Watchdog timer control register
WDTK	B7h	00h	Watchdog timer refresh key.
TAKEY	F7h	00h	Time Access Key register
PWM			
PWMC	B5h	00h	PWM control register
PWMD0H	BCh	00h	PWM channel 0 data high byte
PWMD0L	BDh	00h	PWM channel 0 data low byte
PWMD1H	BEh	00h	PWM channel 1 data high byte
PWMD1L	BFh	00h	PWM channel 1 data low byte
PWMD2H	B1h	00h	PWM channel 2 data high byte
PWMD2L	B2h	00h	PWM channel 2 data low byte
PWMD3H	B3h	00h	PWM channel 3 data high byte
PWMD3L	B4h	00h	PWM channel 3 data low byte
PWMMDH	CEh	00h	PWM Max Data Register, high byte.

Register	Location	Reset value	Description
PWMMDL	CFh	FFh	PWM Max Data Register, low byte.
TIMER0/TIMER1			
TCON	88h	00h	Timer/Counter Control
TMOD	89h	00h	Timer Mode Control
TL0	8Ah	00h	Timer 0, low byte
TL1	8Bh	00h	Timer 1, low byte
TH0	8Ch	00h	Timer 0, high byte
TH1	8Dh	00h	Timer 1, high byte
PFCON	D9h	00h	Peripheral Frequency control register
PCA(TIMER2)			
CCEN	C1h	00h	Compare/Capture Enable Register
CCL1	C2h	00h	Compare/Capture Register 1, low byte
CCH1	C3h	00h	Compare/Capture Register 1, high byte
CCL2	C4h	00h	Compare/Capture Register 2, low byte
CCH2	C5h	00h	Compare/Capture Register 2, high byte
CCL3	C6h	00h	Compare/Capture Register 3, low byte
CCH3	C7h	00h	Compare/Capture Register 3, high byte
T2CON	C8h	00h	Timer 2 Control
CCCON	C9h	00h	Compare/Capture Control
CRCL	CAh	00h	Compare/Reload/Capture Register, low byte
CRCH	CBh	00h	Compare/Reload/Capture Register, high byte
TL2	CCh	00h	Timer 2, low byte
TH2	CDh	00h	Timer 2, high byte
CCEN2	D1h	00h	Compare/Capture Enable 2 register
GPIO			
P0	80h	FFh	Port 0
P1	90h	FFh	Port 1
P3	B0h	FFh	Port 3
P0M0	D2h	00h	Port 0 output mode 0
P0M1	D3h	00h	Port 0 output mode 1
P1M0	D4h	00h	Port 1 output mode 0
P1M1	D5h	00h	Port 1 output mode 1
P3M0	DAh	00h	Port 3 output mode 0
P3M1	DBh	00h	Port 3 output mode 1
ISP/IAP/EEPROM			
IFCON	8Fh	00h	Interface control register
ISPFAH	E1h	FFh	ISP Address-High register
ISPFAL	E2h	FFh	ISP Address-Low register
ISPFDL	E3h	FFh	ISP Data High register
ISPFDH	E3h	FFh	ISP Data Low register
ISPFC	E4h	00h	ISP control register

Register	Location	Reset value	Description
TAKEY	F7h	00h	Time Access Key register
LVI/LVR/SOFTRESET			
RSTS	A1h	00h	Reset status register
LVC	E6h	20h	Low voltage control register
SWRES	E7h	00h	Software Reset register
TAKEY	F7h	00h	Time Access Key register
SPI			
AUX	91h	00h	Auxiliary register
SPIC1	F1h	08h	SPI control register 1
SPIC2	F2h	00h	SPI control register 2
SPITXD	F3h	00h	SPI transmit data buffer
SPIRXD	F4h	00h	SPI receive data buffer
SPIS	F5h	40h	SPI status register
IIC			
AUX	91h	00h	Auxiliary register
IICS	F8h	00h	IIC status register
IICCTL	F9h	04h	IIC control register
IICA1	FAh	A0h	IIC channel 1 Address 1 register
IICA2	FBh	60h	IIC channel 1 Address 2 register
IICRWD	FCh	00h	IIC channel 1 Read / Write Data buffer
IICEBT	FDh	00h	IIC Enable Bus Transaction register
OPA			
OPPIN	F6h	00H	Comparator Pin Select register
CMP0CON	FEh	00h	Comparator 0 Control register
CMP1CON	FFh	00h	Comparator 1 Control register

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