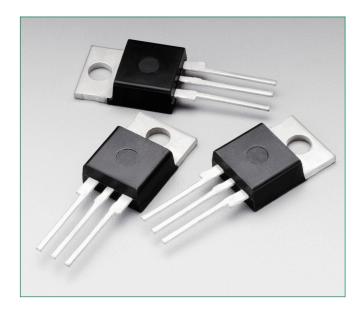
## 2N6400





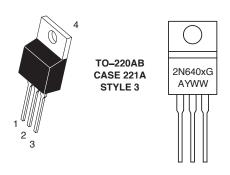
#### **Description**

Designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

#### **Features**

- Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 V
- These are Pb-Free devices

#### **Pin Out**



#### **Functional Diagram**



#### Additional Information







Resources



Samples

## **Thyristors**

#### **Maximum Ratings** † $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

Rating	Part Number	Symbol	Value	Unit
	2N6400		50	
	2N6401		100	
Peak Repetitive Off-State Voltage (Note 1)	2N6402	V <sub>DRM,</sub>	200	V
$(T_{_{\rm J}} = -40 \text{ to } 110^{\circ}\text{C}, \text{ Sine Wave, } 50 \text{ to } 60 \text{ Hz, Gate Open)}$	2N6403	$V_{RRM}$	400	V
	2N6404		600	
	2N6405		800	
On-State RMS Current (180° Conduction Angles; T <sub>C</sub> = 100°C)		I <sub>T (RMS)</sub>	16	А
Average On-State RMS Current (180° Conduction Angles; T <sub>c</sub> = 100°C)			10	А
Peak Non–Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 90$ °C)			160	А
Circuit Fusing Considerations (t = 8.3 ms)			145	A²s
Forward Peak Gate Power (Pulse Width ≤ 1.0 µs, T <sub>C</sub> = 100°C)			20	W
Forward Average Gate Power (t = 8.3 ms, T <sub>c</sub> = 100°C)	P <sub>G(AV)</sub>	0.5	W	
Forward Peak Gate Current (Pulse Width $\leq$ 1.0 $\mu$ s, $T_{c}$ = 100	l <sub>GM</sub>	2.0	А	
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C	
Storage Temperature Range	T <sub>stg</sub>	-40 to +125	°C	

<sup>†</sup>Indicates JEDEC Registered Data

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### **Maximum Ratings** † $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R <sub>eJC</sub>	1.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

<sup>†</sup> Indicates JEDEC Registered Data

<sup>1.</sup> V<sub>DRM</sub> and V<sub>RRM</sub> for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

# **Thyristors**

### **Electrical Characteristics** - **OFF** (T<sub>c</sub> = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
†Peak Repetitive Blocking Current $(V_{AK} = V_{DRM} = V_{RRM}; Gate Open)$	T <sub>J</sub> = 25°C	l <sub>DRM</sub> ,	-	-	1.0	μΑ
	T <sub>J</sub> = 125°C	I <sub>RRM</sub>	-	-	2.0	mA

#### **Electrical Characteristics - ON**

Characteristic			Min	Тур	Max	Unit
†Peak Forward On–State Voltage (I <sub>TM</sub> = 32 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)			-	_	1.7	V
†Gate Trigger Voltage (Continuous DC), All Quadrants	$T_{\rm C} = 25^{\circ}{\rm C}$		-	9.0	30	
(Continuous dc) ( $V_D = 12 \text{ Vdc}, R_L = 100 \Omega$ )	T <sub>C</sub> = -40°C	GT GT	-	-	60	mA
+Cata Trigger Voltage (Continuous de) (V 12)/de D 100 0)	$T_{\rm C} = 25^{\circ}{\rm C}$	V	_	0.7	1.5	V
†Gate Trigger Voltage (Continuous dc) ( $V_D = 12 \text{ Vdc}, R_L = 100 \Omega$ )	T <sub>C</sub> = -40°C	V <sub>GT</sub>	_	_	2.5	
Gate Non-Trigger Voltage ( $V_D = 12 \text{ Vdc}, R_L = 100 \Omega$ )	$T_{\rm C} = +125^{\circ}{\rm C}$	$V_{\rm GD}$	0.2	-	-	V
t Holding Current (V = 12 Vda Initiating Current = 200 mA Cata Open)	$T_{\rm C} = 25^{\circ}{\rm C}$		_	18	40	mA
†Holding Current ( $V_D$ = 12 Vdc, Initiating Current = 200 mA, Gate Open)	T <sub>C</sub> = -40°C	I I <sub>H</sub>	_	_	60	IIIA
Turn-On Time ( $I_{TM} = 12 \text{ A}$ , $I_{GT} = 40 \text{ mAdc}$ , $V_D = \text{Rated } V_{DRM}$ )			-	1.0	-	μs
Turn Off Time (I = 16 A IP = 16 A VD = Pated V )	$T_{\rm C} = 25^{\circ}{\rm C}$		-	15	_	
Turn-Off Time ( $I_{TM} = 16 \text{ A}$ , $IR = 16 \text{ A}$ , $VD = Rated V_{DRM}$ )	T <sub>J</sub> = +125°C	t <sub>q</sub>	-	35	_	μs

<sup>†</sup>Indicates JEDEC Registered Data

#### **Dynamic Characteristics**

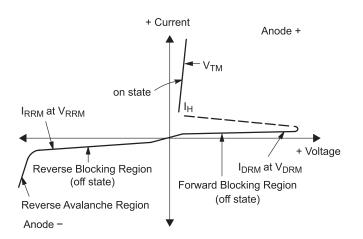
Characteristic		Symbol	Min	Тур	Max	Unit
Critical Rate-of-Rise of Off-State Voltage $(V_D = Rated V_{DRM'} Exponential Waveform)$	T <sub>J</sub> = +125°C	dv/dt(c)	-	50	-	V/µs

**Thyristors** 

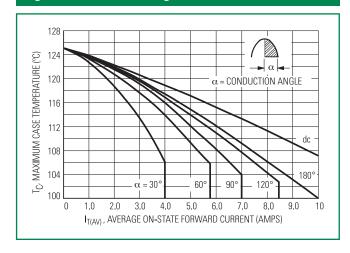


#### **Voltage Current Characteristic of SCR**

Symbol	Parameter
$V_{DRM}$	Peak Repetitive Forward Off State Voltage
I <sub>DRM</sub>	Peak Forward Blocking Current
V <sub>RRM</sub>	Peak Repetitive Reverse Off State Voltage
I <sub>RRM</sub>	Peak Reverse Blocking Current
V <sub>TM</sub>	Maximum On State Voltage
I <sub>H</sub>	Holding Current



#### **Figure 1. Current Derating**



#### Figure 2. Maximum On-State Power Dissipation

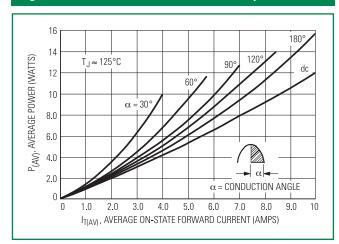


Figure 3. On-State Characteristics

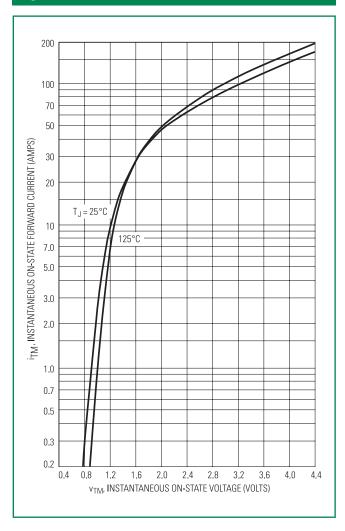


Figure 4. Maximum Non-Repetitive Surge Current

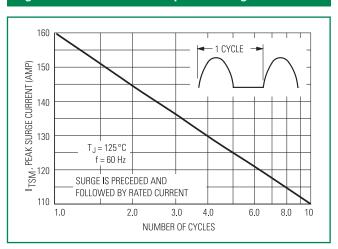
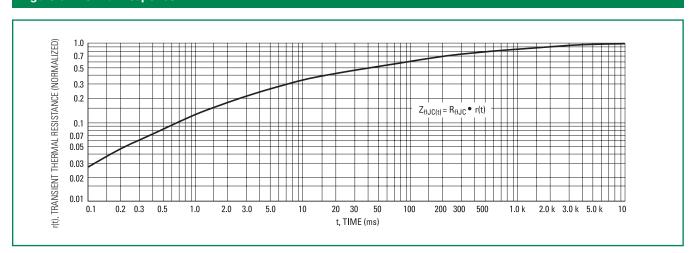


Figure 5. Thermal Response





### Surface Mount -50 - 800V > 2N6400

#### **Typical Characteristics**

Figure 6. Typical Gate Trigger Current vs. Pulse Width

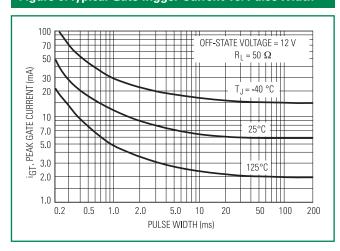


Figure 7. Typical Gate Trigger Current vs. Junction Temperature

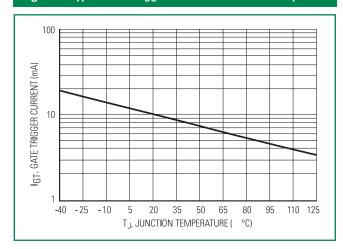


Figure 8. Typical Gate Trigger Voltage vs. Junction Temperature

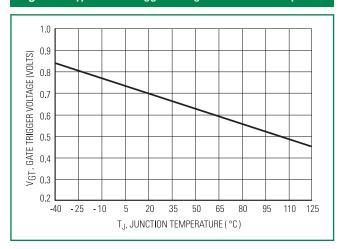
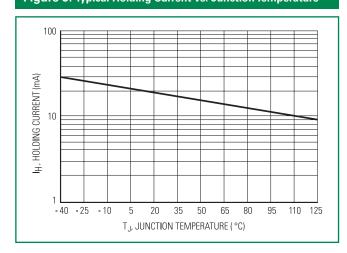
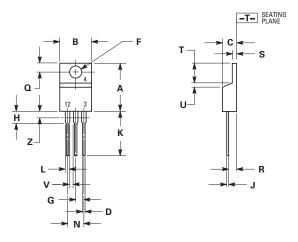


Figure 9. Typical Holding Current vs. Junction Temperature



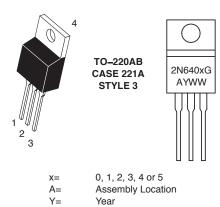
#### **Dimensions**



5.	Inches		Millim	neters
Dim	Min	Max	Min	Max
А	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045		1.15	
Z		0.080		2.04

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

#### **Part Marking System**



Pin Assignment	
1	Cathode
2	Anode

= Work Week Pb-Free Package

WW

G=

**Ordering Information** 

Pin Assignment	
1	Cathode
2	Anode
3	Gate
4	Anode

<u> </u>					
Device	Package	Shipping			
2N6400G					
2N6401G		FOO Unito / Pay			
2N6402G	TO-220AB (Pb-Free)	500 Units / Box			
2N6403G					
2N6403TG		50 Units / Rail			
2N6404G		FOO Unito / Pay			
2N6405G		500 Units / Box			

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