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November 1988 Revised July 2003

## 74AC138 • 74ACT138 1-of-8 Decoder/Demultiplexer

## **General Description**

The AC/ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three AC/ACT138 devices or a 1-of-32 decoder using four AC/ACT138 devices and one inverter.

## **Features**

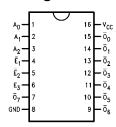
- I<sub>CC</sub> reduced by 50%
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- ACT138 has TTL-compatible inputs

## **Ordering Code:**

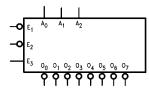
Order Number	Package Number	Package Description					
74AC138SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow					
74AC138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74AC138MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74AC138PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide					
74ACT138SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow					
74ACT138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74ACT138PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide					

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## **Connection Diagram**

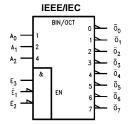


## **Logic Symbols**



## **Pin Descriptions**

Pin Names	Description
A <sub>0</sub> -A <sub>2</sub>	Address Inputs
$\overline{E}_1 - \overline{E}_2$	Enable Inputs
E <sub>3</sub>	Enable Input
$\overline{O}_0 - \overline{O}_7$	Outputs



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## **Truth Table**

	Inputs								Out	puts			
Ē <sub>1</sub>	Ē <sub>2</sub>	E <sub>3</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	$\overline{O}_3$	O <sub>4</sub>	O <sub>5</sub>	<u>o</u> 6	<u>0</u> 7
Н	Х	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	Н	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	Х	L	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	L	L	Н	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

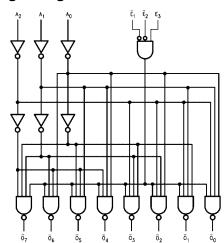
H = HIGH Voltage Level

L = LOW Voltage Level X = Immaterial

## **Functional Description**

The AC/ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs  $(A_0,\ A_1,\ A_2)$  and, when enabled, provides eight mutually exclusive active-LOW outputs  $(\overline{O}_0-\overline{O}_7)$ . The AC/ACT138 features three Enable inputs, two active-LOW  $(\overline{E}_1,\ \overline{E}_2)$  and one active-HIGH  $(E_3)$ . All outputs will be HIGH unless  $\overline{E}_1$  and  $\overline{E}_2$  are LOW and  $E_3$  is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four AC/ACT138 devices and one inverter (see Figure 1). The AC/ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

## **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

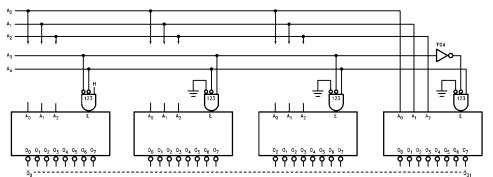


FIGURE 1. Expansion to 1-of-32 Decoding

## **Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0V

DC Input Diode Current (I<sub>IK</sub>)

 $\begin{array}{c} \text{V}_{\text{I}} = -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{I}} = \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \\ \text{DC Input Voltage (V_{\text{I}})} & -0.5 \text{V to V}_{\text{CC}} + 0.5 \text{V} \end{array}$ 

DC Output Diode Current (I<sub>OK</sub>)

$$\begin{split} \text{V}_{\text{O}} &= -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{\text{O}} &= \text{V}_{\text{CC}} + 0.5 \text{V} & +20 \text{ mA} \end{split}$$

DC Output Voltage ( $V_O$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source

or Sink Current ( $I_O$ )  $\pm 50 \text{ mA}$ 

DC V<sub>CC</sub> or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}$ C to  $+150^{\circ}$ C

Storage Temperature ( $T_{STG}$ )  $-65^{\circ}C$ Junction Temperature ( $T_{J}$ )

PDIP 140°C

# Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>)

 $\begin{array}{ccc} AC & 2.0 \text{V to } 6.0 \text{V} \\ ACT & 4.5 \text{V to } 5.5 \text{V} \\ \text{Input Voltage (V_I)} & 0 \text{V to } \text{V}_{\text{CC}} \\ \end{array}$ 

Output Voltage ( $V_O$ ) 0V to  $V_{CC}$ Operating Temperature ( $T_A$ ) -40°C to +85°C

Minimum Input Edge Rate  $(\Delta V/\Delta t)$ 

AC Devices

 $V_{\mbox{\footnotesize{IN}}}$  from 30% to 70% of  $V_{\mbox{\footnotesize{CC}}}$ 

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)

**ACT Devices** 

 $V_{\text{IN}}$  from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/r

140°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## **DC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub>	$V_{CC}$ $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
		(V)	Тур	Gu	aranteed Limits	Oilles	Conditions	
V <sub>IH</sub>	Minimum HIGH Level	3.0	1.5	2.1	2.1		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	3.15	3.15	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level	3.0	1.5	0.9	0.9		V <sub>OUT</sub> = 0.1V	
	Input Voltage	4.5	2.25	1.35	1.35	V	or V <sub>CC</sub> – 0.1V	
		5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level	3.0	2.99	2.9	2.9			
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		$I_{OH} = -24 \text{ mA (Note 2)}$	
V <sub>OL</sub>	Maximum LOW Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
							$V_{IN} = V_{IL}$ or $V_{IH}$	
		3.0		0.36	0.44		$I_{OL} = 12 \text{ mA}$	
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA } 0$	
		5.5		0.36	0.44		I <sub>OL</sub> = 24 mA (Note 2)	
I <sub>IN</sub>	Maximum Input	5.5		±0.1	±1.0	μА	$V_1 = V_{CC}$ , GND	
(Note 4)	Leakage Current	5.5		±0.1	±1.0	μΛ	VI = VCC, GIVD	
I <sub>OLD</sub>	Minimum Dynamic	5.5			75	mA	V <sub>OLD</sub> = 1.65V Max	
I <sub>OHD</sub>	Output Current (Note 3)	5.5			-75	mA	V <sub>OHD</sub> = 3.85V Min	
I <sub>CC</sub> (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μА	V <sub>IN</sub> = V <sub>CC</sub> or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

#### **DC Electrical Characteristics for ACT** $\textbf{T}_{\textbf{A}} = +25^{\circ}\textbf{C}$ $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $v_{cc}$ Units Conditions Symbol Parameter **Guaranteed Limits** (V) Тур Minimum HIGH Level 4.5 1.5 2.0 $V_{OUT} = 0.1V$ 5.5 1.5 2.0 2.0 or V<sub>CC</sub> – 0.1V Maximum LOW Level $V_{\mathsf{IL}}$ 4.5 1.5 0.8 0.8 $V_{OUT} = 0.1V$ Input Voltage 5.5 1.5 0.8 0.8 or $V_{CC} - 0.1V$ Minimum HIGH Level 4.49 4.4 $V_{OH}$ 4.5 4.4 $I_{OUT} = -50 \mu A$ Output Voltage 5.4 5.4 5.5 5.49 $V_{IN} = V_{IL}$ or $V_{IH}$ 3.86 4.5 3.76 V $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 5)}$ 5.5 4.86 4.76 $V_{OL}$ Maximum LOW Level 4.5 0.1 0.1 $I_{OUT} = 50 \, \mu A$ Output Voltage $V_{IN} = V_{IL}$ or $V_{IH}$ 4.5 0.36 0.44 I<sub>OL</sub> 24 mA I<sub>OL</sub>.= 24 mA (Note 5) 5.5 0.36 0.44 Maximum Input $I_{IN}$ 5.5 ±1.0 $V_I = V_{CC}$ , GND μΑ Leakage Current I<sub>CCT</sub> Maximum 5.5 0.6 1.5 $V_I = V_{CC} - 2.1 V$ mΑ I<sub>CC</sub>/Input $V_{OLD} = 1.65V \text{ Max}$ 75 Minimum Dynamic 5.5 $I_{OLD}$ mΑ Output Current (Note 6) 5.5 -75 V<sub>OHD</sub> = 3.85V Min $I_{\text{OHD}}$ mΑ Maximum Quiescent $I_{CC}$ 4.0 40.0 $V_{IN} = V_{CC}$ or GND Supply Current

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

## **AC Electrical Characteristics for AC**

	Parameter	V <sub>CC</sub>		T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°	Units		
Symbol		(V)		$C_L = 50 \ pF$		$C_L = 50 pF$			
		(Note 7)	Min	Тур	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	8.5	13.0	1.5	15.0	ns	
	$A_n$ to $\overline{O}_n$	5.0	1.5	6.5	9.5	1.5	10.5	ns	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	8.0	12.5	1.5	14.0	ns	
	$A_n$ to $\overline{O}_n$	5.0	1.5	6.0	9.0	1.5	10.5		
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	11.0	15.0	1.5	16.0	ns	
	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.5	8.0	11.0	1.5	12.0	115	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	9.5	13.5	1.5	15.0	ns	
	$\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.5	7.0	9.5	1.5	10.5		
t <sub>PLH</sub>	Propagation Delay	3.3	1.5	11.0	15.5	1.5	16.5		
	$E_3$ to $\overline{O}_n$	5.0	1.5	8.0	11.0	1.5	12.5	ns	
t <sub>PHL</sub>	Propagation Delay	3.3	1.5	8.5	13.0	1.5	14.0	ns	
	$E_3$ to $\overline{O}_n$	5.0	1.5	6.0	8.0	1.0	9.5	115	

Note 7: Voltage Range 3.3 is  $3.3V \pm 0.3V$ 

Voltage Range 5.0 is 5.0V  $\pm\,0.5\text{V}$ 

# AC Electrical Characteristics for ACT

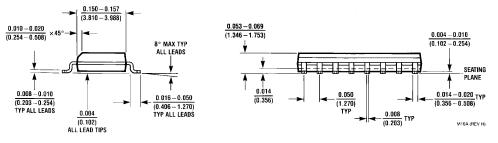
		V <sub>CC</sub>		T <sub>A</sub> = +25°C		$T_{A} = -40^{\circ}$	C to +85°C	
Symbol	Parameter	(V)	C <sub>L</sub> = 50 pF			$C_L = 50 \text{ pF}$		Units
		(Note 8)	Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay $A_n$ to $\overline{O}_n$	5.0	1.5	7.0	10.5	1.5	11.5	ns
t <sub>PHL</sub>	Propagation Delay  A <sub>n</sub> to $\overline{O}_{n}$	5.0	1.5	6.5	10.5	1.5	11.5	ns
t <sub>PLH</sub>	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	2.5	8.0	11.5	2.0	12.5	ns
t <sub>PHL</sub>	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	2.0	7.5	11.5	2.0	12.5	ns
t <sub>PLH</sub>	Propagation Delay E <sub>3</sub> to $\overline{O}n$	5.0	2.5	8.0	12.0	2.0	13.0	ns
t <sub>PHL</sub>	Propagation Delay E <sub>3</sub> to $\overline{O}n$	5.0	2.0	6.5	10.5	1.5	11.5	ns

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

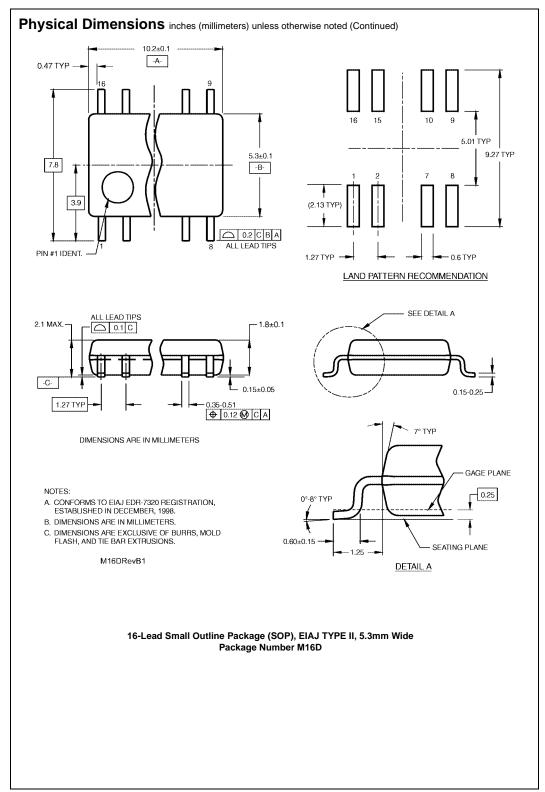
## Capacitance

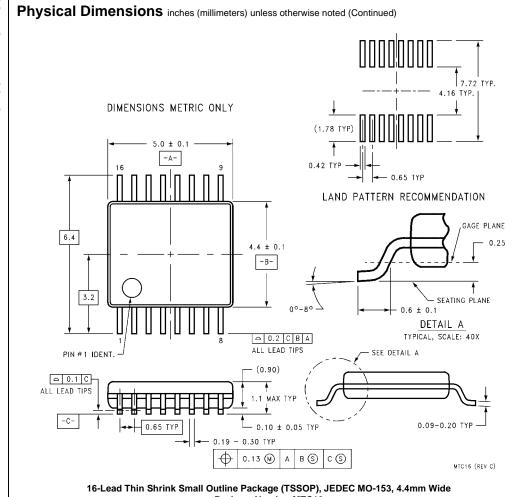
Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
CPD	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$

# 



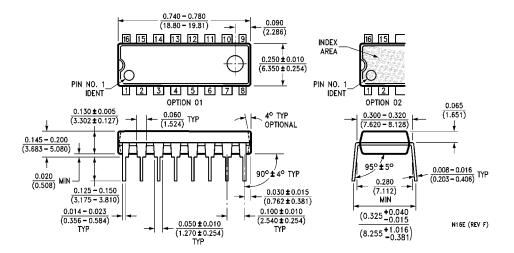
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A





16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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