

74F11

Triple 3-Input AND Gate

General Description

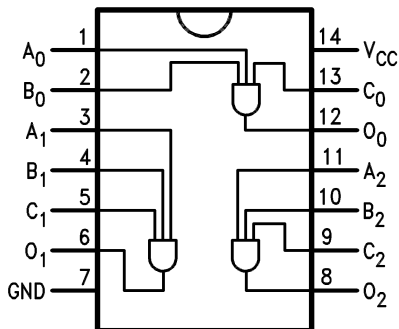
This device contains three independent gates, each of which performs the logic AND function.

Ordering Information

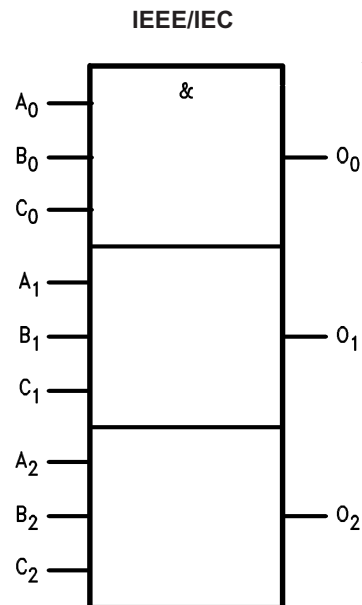
Order Number	Package Number	Package Description
74F11SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F11SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

Connection Diagram



Logic Symbol



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} , Output I_{OH}/I_{OL}
A_n, B_n, C_n	Inputs	1.0 / 1.0	20 μ A / -0.6mA
O_n	Outputs	50 / 33.3	-1 mA / 20 mA

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	-65°C to $+150^{\circ}\text{C}$
T_A	Ambient Temperature Under Bias	-55°C to $+125^{\circ}\text{C}$
T_J	Junction Temperature Under Bias	-55°C to $+150^{\circ}\text{C}$
V_{CC}	V_{CC} Pin Potential to Ground Pin	-0.5V to $+7.0\text{V}$
V_{IN}	Input Voltage ⁽¹⁾	-0.5V to $+7.0\text{V}$
I_{IN}	Input Current ⁽¹⁾	-30mA to $+5.0\text{mA}$
V_O	Voltage Applied to Output in HIGH State (with $V_{CC} = 0\text{V}$)	
	Standard Output	-0.5V to V_{CC}
	3-STATE Output	-0.5V to 5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	0°C to $+70^{\circ}\text{C}$
V_{CC}	Supply Voltage	$+4.5\text{V}$ to $+5.5\text{V}$

DC Electrical Characteristics

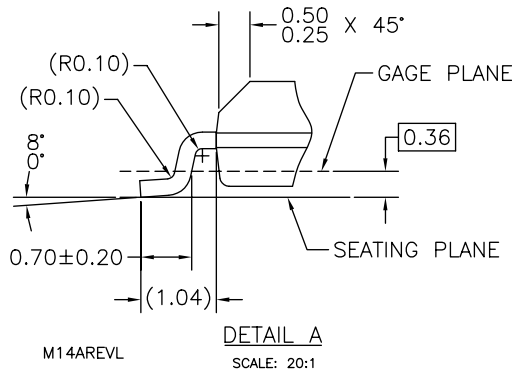
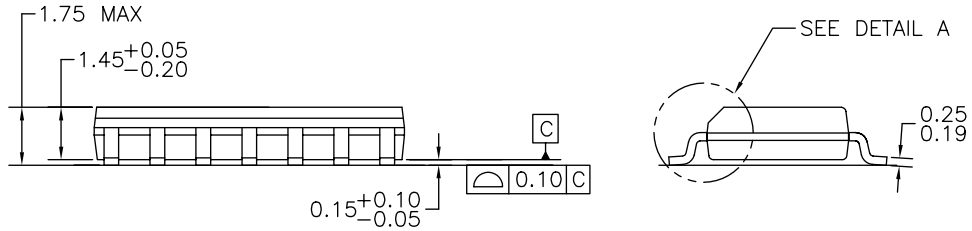
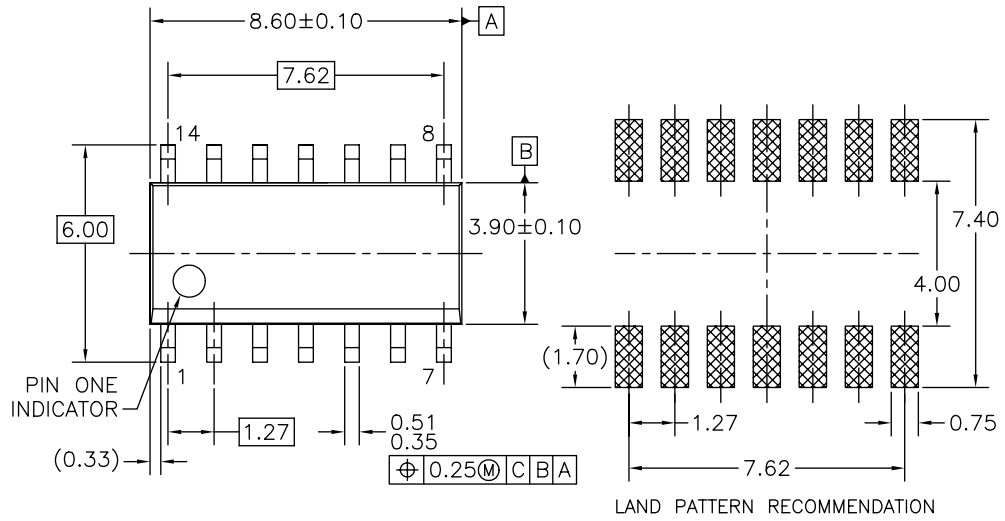
Symbol	Parameter	V_{CC}	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		Recognized as a HIGH Signal	2.0			V
V_{IL}	Input LOW Voltage		Recognized as a LOW Signal			0.8	V
V_{CD}	Input Clamp Diode Voltage	Min.	$I_{IN} = -18\text{mA}$			-1.2	V
V_{OH}	Output HIGH Voltage	10% V_{CC}	Min. $I_{OH} = -1\text{mA}$	2.5			V
		5% V_{CC}		$I_{OH} = -1\text{mA}$	2.7		
V_{OL}	Output LOW Voltage	10% V_{CC}	Min. $I_{OL} = 20\text{mA}$			0.5	V
I_{IH}	Input HIGH Current	Max.	$V_{IN} = 2.7\text{V}$			5.0	μA
I_{BVI}	Input HIGH Current Breakdown Test	Max.	$V_{IN} = 7.0\text{V}$			7.0	μA
I_{CEX}	Output HIGH Leakage Current	Max.	$V_{OUT} = V_{CC}$			50	μA
V_{ID}	Input Leakage Test	0.0	$I_{ID} = 1.9\mu\text{A}$, All other pins grounded	4.75			V
I_{OD}	Output Leakage Circuit Current	0.0	$V_{IOD} = 150\text{mV}$, All other pins grounded			3.75	μA
I_{IL}	Input LOW Current	Max.	$V_{IN} = 0.5\text{V}$			-0.6	mA
I_{OS}	Output Short-Circuit Current	Max.	$V_{OUT} = 0\text{V}$	-60		-150	mA
I_{CCH}	Power Supply Current	Max.	$V_O = \text{HIGH}$		4.1	6.2	mA
I_{CCL}	Power Supply Current	Max.	$V_O = \text{LOW}$		6.5	9.7	mA

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $C_L = 50\text{pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $C_L = 50\text{pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $C_L = 50\text{pF}$		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, A_n, B_n, C_n to O_n	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns
t_{PHL}		2.5	4.1	5.5	2.0	7.5	2.5	6.5	

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



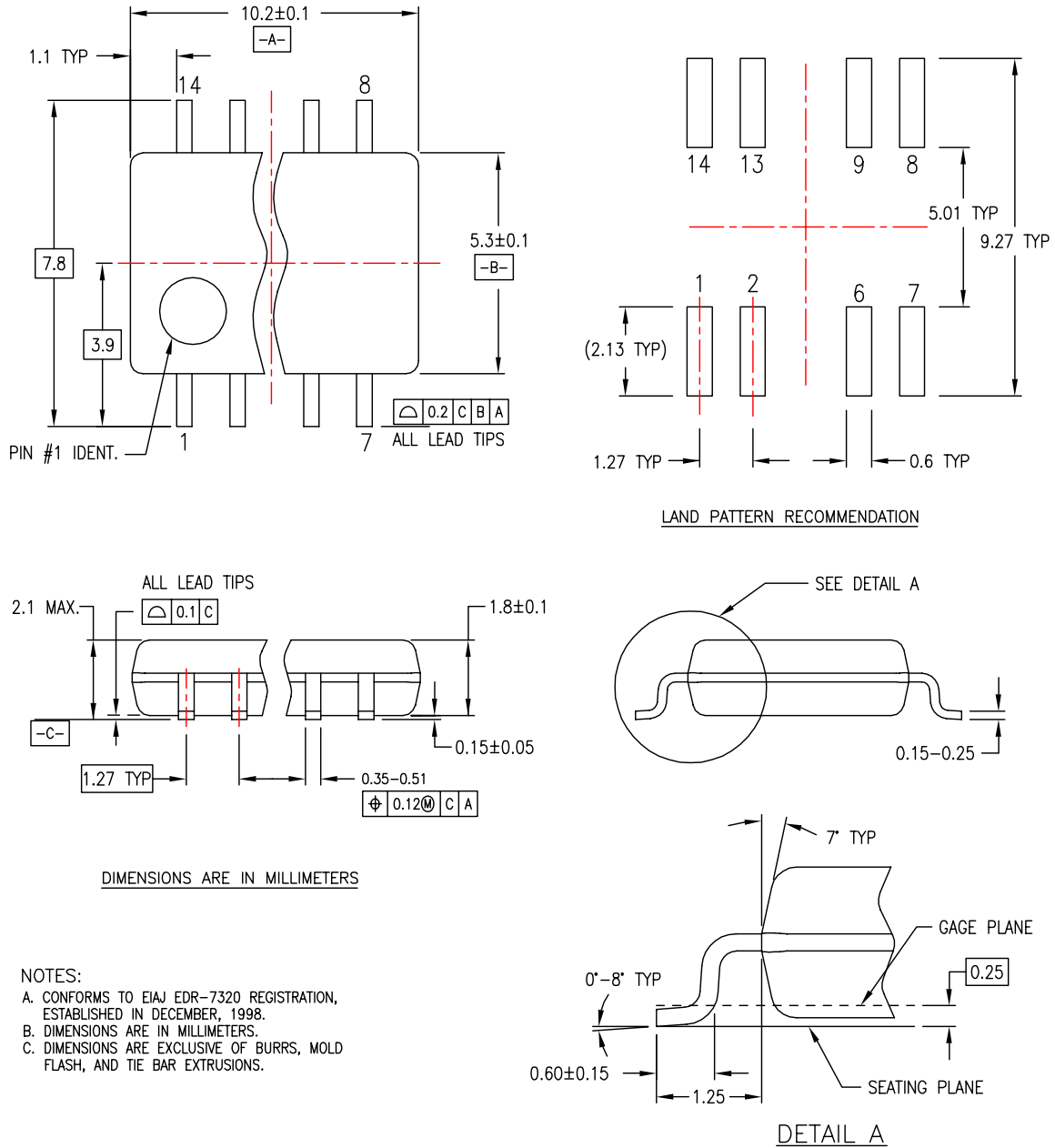
NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D



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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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