FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR™

May 2002
Revised June 2005

74LCXH16245
Low Voltage 16-Bit Bidirectional Transceiver with Bushold

General Description

The LCXH16245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The device is byte controlled. Each byte has separate control inputs which could be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B Ports by placing them in a high impedance state.

The LCXH16245 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The LCXH16245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 2.3V–3.6V V_{CC} specifications provided
- 4.5 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max
- Power-down high impedance outputs
- Bushold on inputs eliminates the need for external pull-up/pull-down resistors
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance conforms to the requirements of JESD78
- ESD performance:
    Human body model > 2000V
    Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

Order Number	Package Number	Package Description
74LCXH16245G (Note 1) (Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCXH16245MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: Ordering Code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
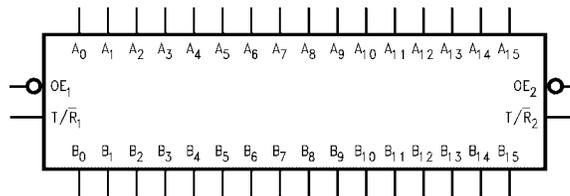
Connection Diagrams

Pin Assignment for SSOP and TSSOP

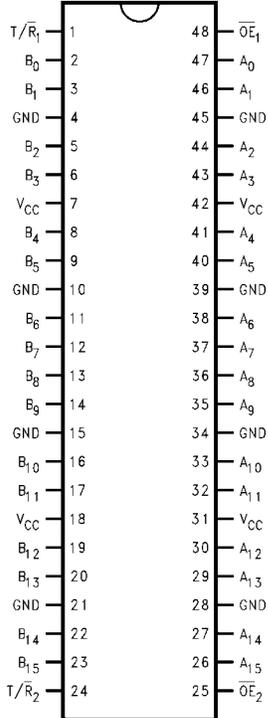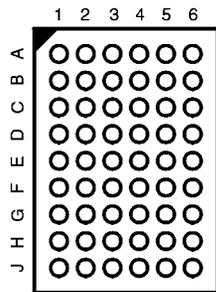|			
$T/\overline{R}_1$	1	48	$\overline{OE}_1$
B_0	2	47	A_0
B_1	3	46	A_1
GND	4	45	GND
B_2	5	44	A_2
B_3	6	43	A_3
V_{CC}	7	42	V_{CC}
B_4	8	41	A_4
B_5	9	40	A_5
GND	10	39	GND
B_6	11	38	A_6
B_7	12	37	A_7
B_8	13	36	A_8
B_9	14	35	A_9
GND	15	34	GND
B_{10}	16	33	A_{10}
B_{11}	17	32	A_{11}
V_{CC}	18	31	V_{CC}
B_{12}	19	30	A_{12}
B_{13}	20	29	A_{13}
GND	21	28	GND
B_{14}	22	27	A_{14}
B_{15}	23	26	A_{15}
$T/\overline{R}_2$	24	25	$\overline{OE}_2$

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs or 3-STATE Outputs (Bushold)
B_0–B_{15}	Side B Inputs or 3-STATE Outputs (Bushold)

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CC}	V_{CC}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CC}	V_{CC}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH Z State on A_0–A_7, B_0–B_7

Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH Z State on A_8–A_{15}, B_8–B_{15}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 5)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	V_{CC}	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused control inputs must be HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter		Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
					Min	Max	
V_{IH}	HIGH Level Input Voltage			2.3 – 2.7	1.7		V
				2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage			2.3 – 2.7		0.7	V
				2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage		I_{OH} = −100 μA	2.3 – 3.6	V_{CC} − 0.2		V
			I_{OH} = −8 mA	2.3	1.8		
			I_{OH} = −12 mA	2.7	2.2		
			I_{OH} = −18 mA	3.0	2.4		
			I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage		I_{OL} = 100 μA	2.3 – 3.6		0.2	V
			I_{OL} = 8mA	2.3		0.6	
			I_{OL} = 12 mA	2.7		0.4	
			I_{OL} = 16 mA	3.0		0.4	
			I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	Data	V_I = V_{CC} or GND	2.3 – 3.6		±5.0	μA
		Control	O ≤ V_I ≤ 5.5	2.3 – 3.6		±5.0	

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	V_{IN} = 0.7V	2.3	45		μA
		V_{IN} = 1.7V	2.3	−45		
		V_{IN} = 0.8V	3.0	75		
		V_{IN} = 2.0V	3.0	−75		
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State	(Note 6)	2.7	300		μA
		(Note 7)	2.7	−300		
		(Note 6)	3.6	450		
		(Note 7)	3.6	−450		
I_{OZ}	3-STATE I/O Leakage	$V_O = V_{CC}$ or GND	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.3–3.6		20	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC}$ −0.6V	2.3–3.6		500	μA

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Electrical Characteristics

Symbol	Parameter	T_A = −40°C to +85°C, R_L = 500Ω V_{CC} = 3.3V ± 0.3V C_L = 50 pF Min	Max	V_{CC} = 2.7V C_L = 50 pF Min	Max	V_{CC} = 2.5V ± 0.2V C_L = 30 pF Min	Max	Units
t_{PHL}	Propagation Delay	1.0	4.5	1.0	5.2	1.0	5.4	ns
t_{PLH}	A_n to B_n or B_n to A_n	1.0	4.5	1.0	5.2	1.0	5.4	
t_{PZL}	Output Enable Time	1.0	6.5	1.0	7.2	1.0	8.5	ns
t_{PZH}		1.0	6.5	1.0	7.2	1.0	8.5	
t_{PLZ}	Output Disable Time	1.0	6.4	1.0	6.9	1.0	7.7	ns
t_{PHZ}		1.0	6.4	1.0	6.9	1.0	7.7	
t_{OSHL}	Output to Output Skew (Note 8)		1.0					ns
t_{OSLH}			1.0					

Note 8: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	−0.8	V
		C_L = 30 pF, V_{IH} = 2.5V, V_{IL} = 0V	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, f = 10 MHz	20	pF

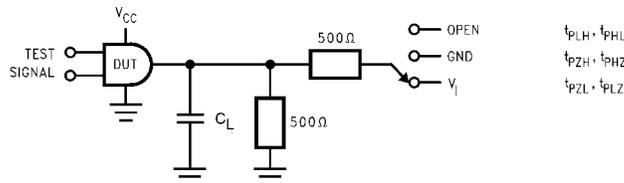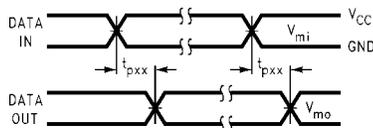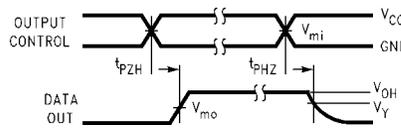# AC LOADING and WAVEFORMS Generic for LCX Family

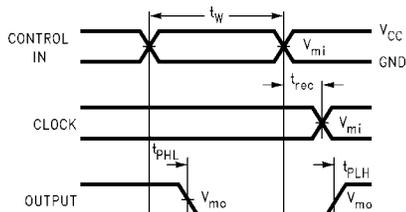FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

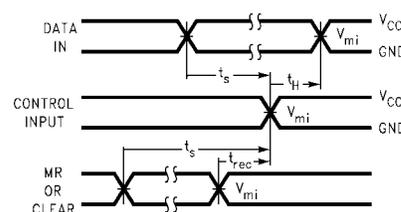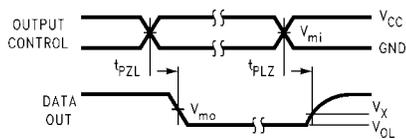| Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 ± 0.3V, 2.7V and V_{CC} x 2 at V_{CC} = 2.5 ± 0.2V
t_{PZH}, t_{PHZ}	GND

Waveform for Inverting and Non-Inverting Functions

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic

3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}
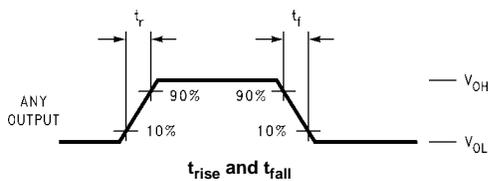
FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, t_r = t_f = 3ns)

Symbol	V_{CC}		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V_{mi}	1.5V	1.5V	V_{CC}/2
V_{mo}	1.5V	1.5V	V_{CC}/2
V_x	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V
V_y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V

Schematic Diagram Generic for LCX Family

input stage

P1

Data

ESD

D2 N+/P−

N1

P2

N2

input stage

P3

Enable

ESD

D4 N+/P−

N3

P4

N4

GTO™

V_CC

P5

X1

V_DD

Output

D6
N+/P−

N5

Physical Dimensions inches (millimeters) unless otherwise noted
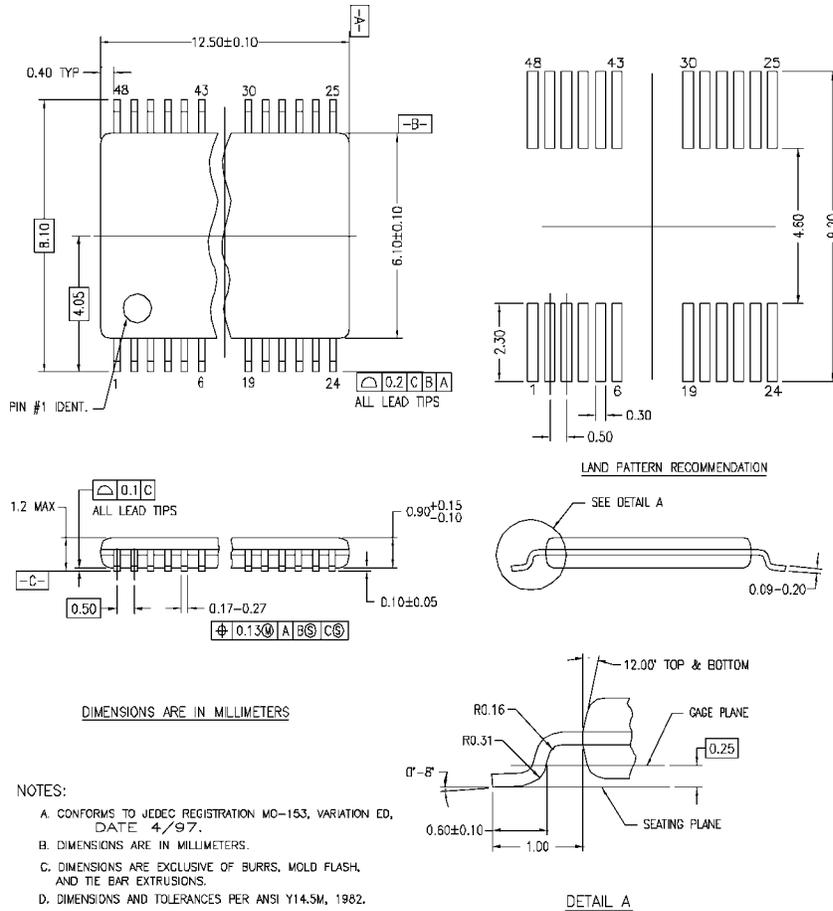

Top
View

PIN ONE

Bottom
View

54X 0.5 +0.05 -0.05
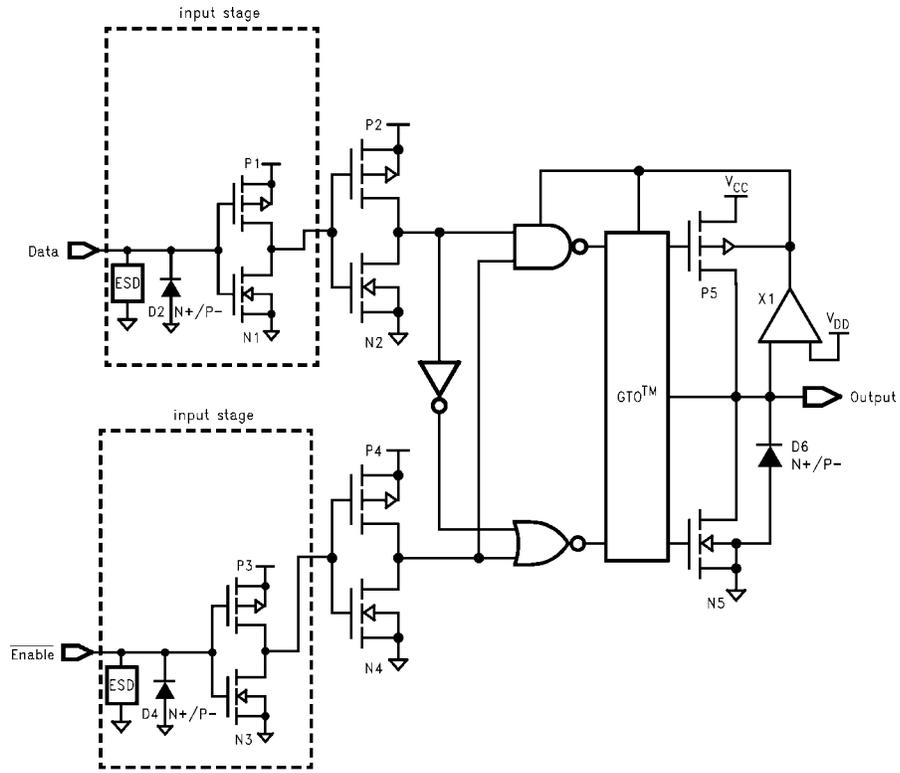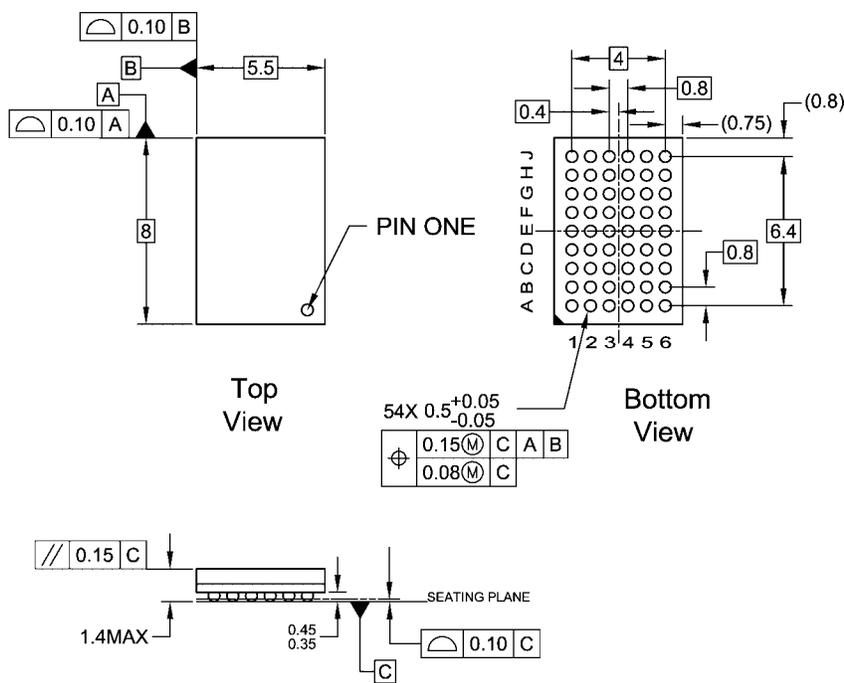
NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.50±0.10

0.40 TYP

-A-

-B-

48 43 30 25

8.10

4.05

6.10±0.10

PIN #1 IDENT.

1   6   19   24

△ 0.2 C B A
ALL LEAD TIPS

48 43   30 25

4.60   9.20

2.30

1   6   19   24

0.30

0.50

LAND PATTERN RECOMMENDATION

△ 0.1 C
ALL LEAD TIPS

1.2 MAX

-C-

0.50

0.17–0.27

0.90 +0.15 −0.10

0.10±0.05

⊕ 0.13Ⓜ A BⓈ CⓈ

SEE DETAIL A

0.09–0.20

DIMENSIONS ARE IN MILLIMETERS

12.00° TOP & BOTTOM

R0.16

R0.31

GAGE PLANE

0.25

0°–8°

0.60±0.10

1.00

SEATING PLANE

DETAIL A

NOTES:
   A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED,
      DATE 4/97.
   B. DIMENSIONS ARE IN MILLIMETERS.
   C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
      AND TIE BAR EXTRUSIONS.
   D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

PUBLICATION ORDERING INFORMATION

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Bus Transceivers *category:*

Click to view products by ON Semiconductor *manufacturer:*

Other Similar products are found below :

74LS645N PI74LVCC3245AS 5962-8683401DA 5962-8968201LA 5962-8953501KA 5962-86834012A 5962-7802002MFA

TC74VCX164245(EL,F MC74LCX245MNTWG TC7WPB8306L8X,LF(S MM74HC245AMTCX 74LVX245MTC 74ALVC16245MTDX

74LCXR162245MTX 74LVXC3245MTCX 74VHC245M 74VHC245MX JM38510/65553BRA FXL2TD245L10X 74LVC1T45GM,115

74LVC245ADTR2G TC74AC245P(F) SNJ54LS245FK 74LVT245BBT20-13 74AHC245D.112 74AHCT245D.112

SN74LVCH16952ADGGR CY74FCT16245TPVCT 74AHCT245PW.118 74LV245DB.118 74LV245D.112 74LV245PW.112

74LVC2245APW.112 74LVCH245AD.112 SN75138NSR AP54RHC506ELT-R AP54RHC506BLT-R 74LVCR162245ZQLR

SN74LVCR16245AZQLR MC100EP16MNR4G MC100LVEP16MNR4G 714100R 74HCT643N MC100EP16DTR2G 5962-9221403MRA

74ALVC164245PAG 74FCT16245ATPAG 74FCT16245ATPVG 74FCT16245ETPAG 74FCT245CTSOG