FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

74LVX04
Low Voltage Hex Inverter

Features

■ Input voltage level translation from 5V to 3V

■ Ideal for low power/low noise 3.3V applications

■ Guaranteed simultaneous switching noise level and dynamic threshold performance

General Description

The LVX04 contains six inverters. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Ordering Information

Order Number	Package Number	Package Description
74LVX04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Logic Symbol

IEEE/IEC
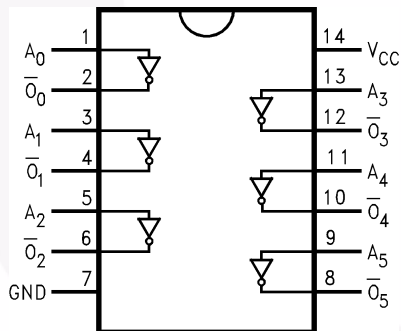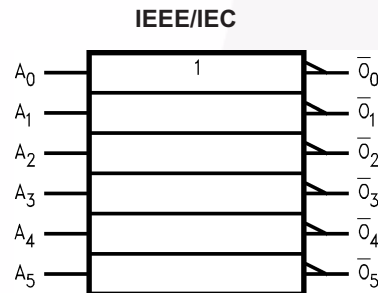
Pin Description

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current, V_I = –0.5V	–20mA
V_I	DC Input Voltage	–0.5V to 7V
I_{OK}	DC Output Diode Current	
	V_O = –0.5V	–20mA
	$V_O = V_{CC}$ + 0.5V	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±25mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
P	Power Dissipation	180mW

Recommended Operating Conditions[1]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 3.6V
V_I	Input Voltage	0V to 5.5V
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V$_{CC}$	Conditions	T$_A$ = +25°C			T$_A$ = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V$_{IH}$	HIGH Level Input Voltage	2.0		1.5			1.5		V
		3.0		2.0			2.0		
		3.6		2.4			2.4		
V$_{IL}$	LOW Level Input Voltage	2.0				0.5		0.5	V
		3.0				0.8		0.8	
		3.6				0.8		0.8	
V$_{OH}$	HIGH Level Output Voltage	2.0	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OH}$ = –50µA	1.9	2.0		1.9		V
		3.0	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OH}$ = –50µA	2.9	3.0		2.9		
			V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OH}$ = –4mA	2.58			2.48		
V$_{OL}$	LOW Level Output Voltage	2.0	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OL}$ = 50µA		0.0	0.1		0.1	V
		3.0	V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OL}$ = 50µA		0.0	0.1		0.1	
			V$_{IN}$ = V$_{IL}$ or V$_{IH}$, I$_{OL}$ = 4mA			0.36		0.44	
I$_{IN}$	Input Leakage Current	3.6	V$_{IN}$ = 5.5V or GND			±0.1		±1.0	µA
I$_{CC}$	Quiescent Supply Current	3.6	V$_{IN}$ = V$_{CC}$ or GND			2.0		20.0	µA

Noise Characteristics[2]

Symbol	Parameter	V$_{CC}$ (V)	C$_L$ (pF)	T$_A$ = 25°C		Units
				Typ.	Limit	
V$_{OLP}$	Quiet Output Maximum Dynamic V$_{OL}$	3.3	50	0.3	0.5	V
V$_{OLV}$	Quiet Output Minimum Dynamic V$_{OL}$	3.3	50	–0.3	–0.5	V
V$_{IHD}$	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V$_{ILD}$	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

Note:

2. Input t$_r$ = t$_f$ = 3ns

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = +25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7	15		5.4	10.1	1.0	12.5	ns
			50		7.9	13.6	1.0	16.0	
		3.3 ± 0.3	15		4.1	6.2	1.0	7.5	
			50		6.6	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew[3]	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

Note:

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

Capacitance

Symbol	Parameter	T_A = +25°C			T_A = –40°C to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance[4]		18				pF

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
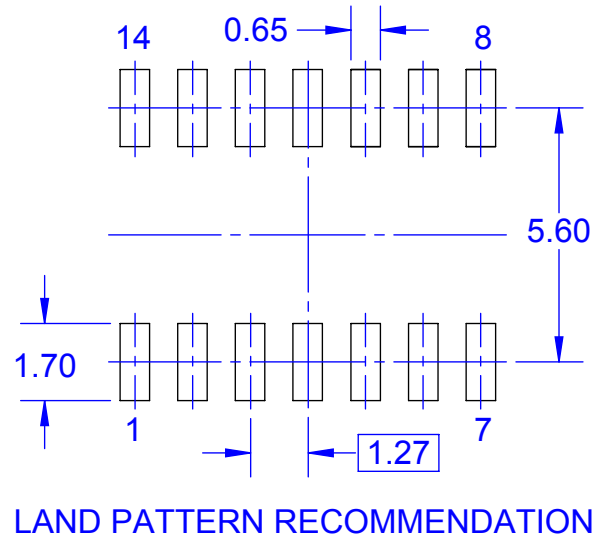
Average operating current can be obtained by the eqation: $I_{CC(opr.)} = \dfrac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{6\,(\text{per Gate})}$

TOP VIEW

5.00±0.10 [A]

0.43TYP

14   8

[B]

6.4

4.40±0.10

3.2

PIN#1 IDENT

1   TOP VIEW   7

⌒ 0.2 C B A
ALL LEAD TIPS

RECOMMENDED LAND PATTERN

0.65

6.10

1.65

0.45

RECOMMENDED LAND PATTERN

FRONT VIEW

1.2 MAX

0.90 +0.15 −0.10

0.10±0.05

ALL LEAD TIPS

⌒ 0.1 C

0.65

0.30
0.19

[C]

⊕ 0.13Ⓜ A BⓈ CⓈ

FRONT VIEW

DETAIL A

SEE DETAIL A

0.20
0.09

12.00° TOP & BOTTOM

0.09 MIN

GAGE PLANE

0.09 MIN

0.25

0°- 8°

0.6±0.1

1.00

SEATING PLANE

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153,
   VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI
   Y14.5M, 2009.
E. LANDPATTERN STANDARD: SOP65P640X110-14M.
F. DRAWING FILE NAME: MKT-MTC14rev7.

FAIRCHILD.

TOP VIEW

8.75
8.50
A

7.62
14 8
B

6.00

4.00
3.80

PIN #1
IDENT.
1 7

1.27
0.51
0.35

(0.33)

TOP VIEW

⊕ | 0.25 Ⓜ | C | B | A

LAND PATTERN RECOMMENDATION

14 0.65 8

5.60

1.70

1 7

1.27

LAND PATTERN RECOMMENDATION

FRONT VIEW

1.75 MAX

C

1.50
1.25

0.25
0.10

△ | 0.10 | C

FRONT VIEW

SIDE VIEW

A

0.25
0.19

SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012,
   VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS
D. LAND PATTERN STANDARD:
   SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14

FAIRCHILD ™

DETAIL A

0.50
0.25 X 45°

R0.10

GAGE
PLANE

R0.10

0.36

8°
0°

0.90
0.50

SEATING PLANE

(1.04)

DETAIL A
SCALE 16 : 1

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC   www.onsemi.com

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for ON Semiconductor *manufacturer:*

Other Similar products are found below :

1.5SMC82AT3G 74LCX574WM STK621-068C-E KAF-0402-ABA-CD-B2 NBXSBA017LN1TAG KAF-3200-ABA-CP-B2 STK621-728S-E AMIS30621AUA STK531U340A-E STK760-304-E FJAF6810DTU DBD250G STK621-713-E TIP115 LB11847-E NBXHBA017LN1TAG LV8736V-MPB-H NCP694H12HT1G LA4631VC-XE CAT1025WI-25-G NDF04N60ZG-001 LA78040B-S-E NGTB30N120IHLWG LA6584M-MPB-E NVB60N06T4G LA6245P-CL-TLM-E STK621-043D-E BTA30H-600CW3G P6SMB100AT3G NCP1129AP100G LV8406T-TLM-E MC100EL13DWG NGTB30N60SWG FW217A-TL-2WX FGPF4533 MC33201DG KA78L05AZTA KA378R33TU FST3126MX LV4904V-MPB-E STK672-400 SBM30-03-TR-E NCP1398BDR2G BTA25H-600CW3G LC89057W-VF4A-E NGB8206ANTF4G CPH6531-TL-E NCP4683DSQ28T1G MC78L08ACP SA5230DR2G