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## 74VCX86

### Low Voltage Quad 2-Input Exclusive-OR Gate with 3.6V Tolerant Inputs and Outputs

#### General Description

The VCX86 contains four 2-input exclusive OR gates. This product is designed for low voltage (1.2V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V

The 74VCX86 is fabricated with an advanced CMOS technology to achieve high-speed operation while maintaining low CMOS power dissipation.

#### Features

- 1.2V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$   
3.0 ns max for 3.0V to 3.6V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Static Drive ( $I_{OH}/I_{OL}$ )  
 $\pm 24$  mA @ 3.0V  $V_{CC}$
- Uses proprietary noise/EMI reduction circuit
- Latchup performance exceeds JEDEC 78 conditions
- ESD performance:  
Human body model > 2000V  
Machine model > 250V
- Leadless Pb-Free DQFN package

#### Ordering Code:

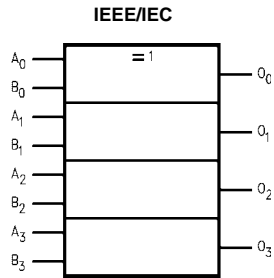
Order Number	Package Number	Package Description
74VCX86M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VCX86BQX (Note 1)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74VCX86MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** DQFN package available in Tape and Reel only.

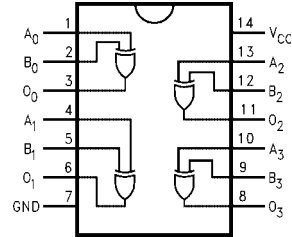
74VCX86 Low Voltage Quad 2-Input Exclusive-OR Gate with 3.6V Tolerant Inputs and Outputs

**Logic Symbol**



**Connection Diagrams**

**Pin Assignments for SOIC and TSSOP**

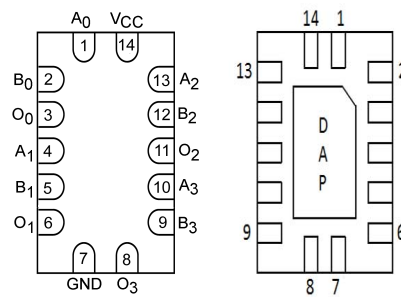


**Pin Descriptions**

Pin Names	Description
A <sub>n</sub> , B <sub>n</sub>	Inputs
O <sub>n</sub>	Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

**Pad Assignments for DQFN**



**(Top View)**

**(Bottom View)**

**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
HIGH or LOW State (Note 3)	-0.5V to $V_{CC}$ +0.5V
$V_{CC} = 0V$	-0.5V to +4.6V
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	±50 mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or Ground)	±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 4)

Power Supply	
Operating	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
HIGH or LOW State	0V to $V_{CC}$
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	±24 mA
$V_{CC} = 2.3V$ to 2.7V	±18 mA
$V_{CC} = 1.65V$ to 2.3V	±6 mA
$V_{CC} = 1.4V$ to 1.6V	±2 mA
$V_{CC} = 1.2V$	±100 $\mu$ A
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
			2.3 - 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
			1.2	$0.65 \times V_{CC}$		
$V_{IL}$	LOW Level Input Voltage		2.7 - 3.6		0.8	V
			2.3 - 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
			1.2			
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -12 mA$ $I_{OH} = -18 mA$ $I_{OH} = -24 mA$	2.7 - 3.6	$V_{CC} - 0.2$		V
			2.7	2.2		
			3.0	2.4		
			3.0	2.2		
		2.3 - 2.7	$V_{CC} - 0.2$			
			2.3	2.0		
			2.3	1.8		
			2.3	1.7		
		1.65 - 2.3	$V_{CC} - 0.2$			
			1.65	1.25		
		1.4 - 1.6	$V_{CC} - 0.2$			
			1.4	1.05		
		1.2	$V_{CC} - 0.2$			

### DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7 - 3.6		0.2	V
		I <sub>OL</sub> = 12 mA	2.7	0.4		
		I <sub>OL</sub> = 18 mA	3.0	0.4		
		I <sub>OL</sub> = 24 mA	3.0	0.55		
		I <sub>OL</sub> = 100 μA	2.3 - 2.7	0.2		
		I <sub>OL</sub> = 12 mA	2.3	0.4		
		I <sub>OL</sub> = 18 mA	2.3	0.6		
		I <sub>OL</sub> = 100 μA	1.65 - 2.3	0.2		
		I <sub>OL</sub> = 6 mA	1.65	0.3		
		I <sub>OL</sub> = 100 μA	1.4 - 1.6	0.2		
I <sub>OL</sub> = 2 mA	1.4	0.35				
I <sub>OL</sub> = 100 μA	1.2	0.05				
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 3.6V	1.2 - 3.6		±5.0	μA
I <sub>OFF</sub>	Power-OFF Leakage Current	0 ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND V <sub>CC</sub> ≤ (V <sub>I</sub> )	1.2 - 3.6		20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.7 - 3.6		750	μA

### AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Figure Number
				Min	Max		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3	0.6	3.0	ns	Figures 1, 2
			2.5 ± 0.2	0.8	3.9		
			1.8 ± 0.15	1.0	7.8		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1	1.0	15.6		Figures 3, 4
1.2	1.5	39					
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 6)	C <sub>L</sub> = 30 pF, R <sub>L</sub> = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ	1.5 ± 0.1		1.5		
		1.2		1.5			

**Note 5:** For C<sub>L</sub> = 50 pF, add approximately 300 ps to the AC maximum specification.

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSSL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

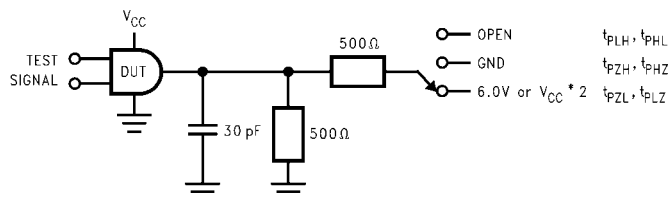
## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	0.25	V
			2.5	0.6	
			3.3	0.8	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	-0.25	V
			2.5	-0.6	
			3.3	-0.8	
V <sub>OHV</sub>	Quiet Output Dynamic Valley V <sub>OH</sub>	C <sub>L</sub> = 30 pF, V <sub>IH</sub> = V <sub>CC</sub> , V <sub>IL</sub> = 0V	1.8	1.5	V
			2.5	1.9	
			3.3	2.2	

## Capacitance

Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C	Units
			Typical	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 1.8, 2.5V or 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	7	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz, V <sub>CC</sub> = 1.8V, 2.5V or 3.3V	20	pF

## AC Loading and Waveforms (V<sub>CC</sub> 3.3V ± 0.3V to 1.8V ± 0.15V)



TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open

FIGURE 1. AC Test Circuit

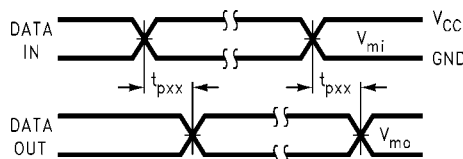
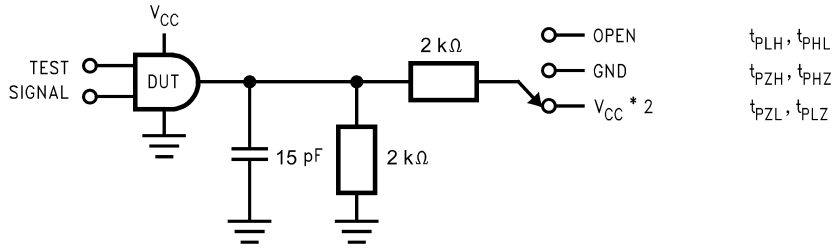


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

Symbol	V <sub>CC</sub>		
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V
V <sub>mi</sub>	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
V <sub>mo</sub>	1.5V	V <sub>CC</sub> /2	V <sub>CC</sub> /2

AC Loading and Waveforms ( $V_{CC} 1.5V \pm 0.1V$  to  $1.2V$ )



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{CC} \times 2$ at $V_{CC} = 1.5 \pm 0.1V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 3. AC Test Circuit

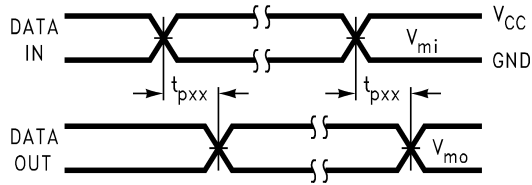


FIGURE 4. Waveform for Inverting and Non-Inverting Functions

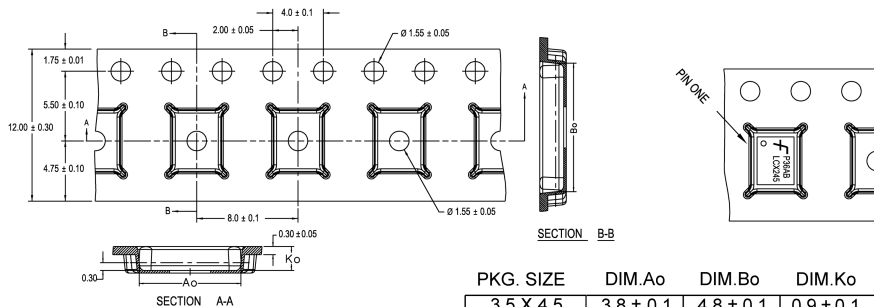
Symbol	$V_{CC}$
	$1.5V \pm 0.1V$
$V_{mi}$	$V_{CC}/2$
$V_{mo}$	$V_{CC}/2$

## Tape and Reel Specification

### Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### TAPE DIMENSIONS inches (millimeters)



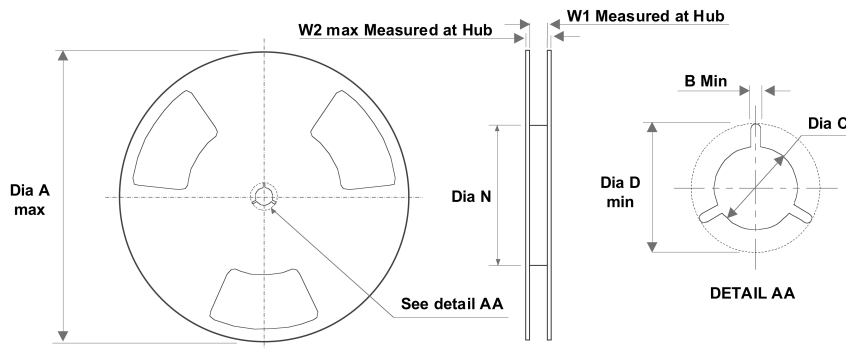
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

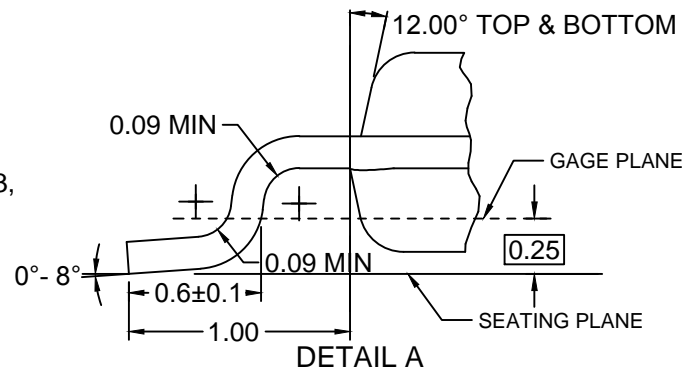
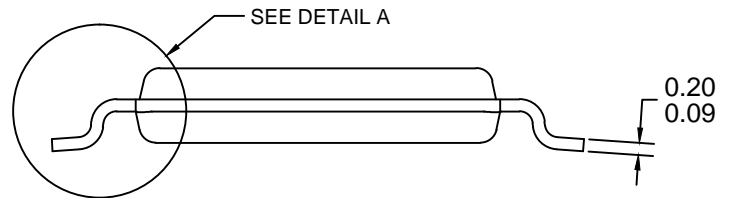
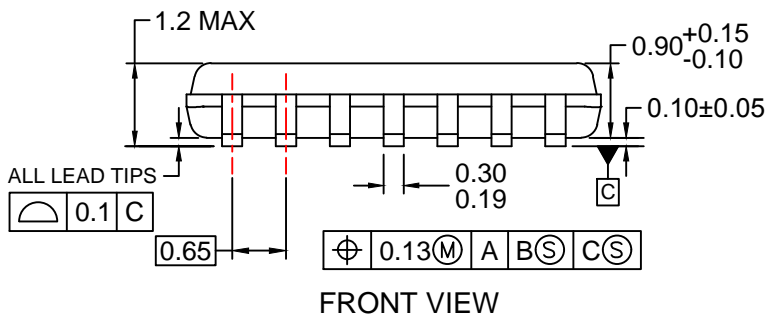
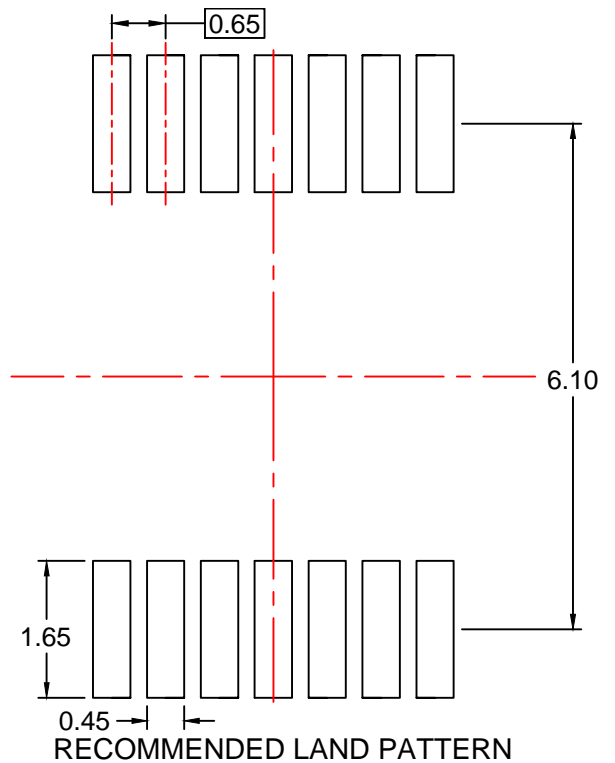
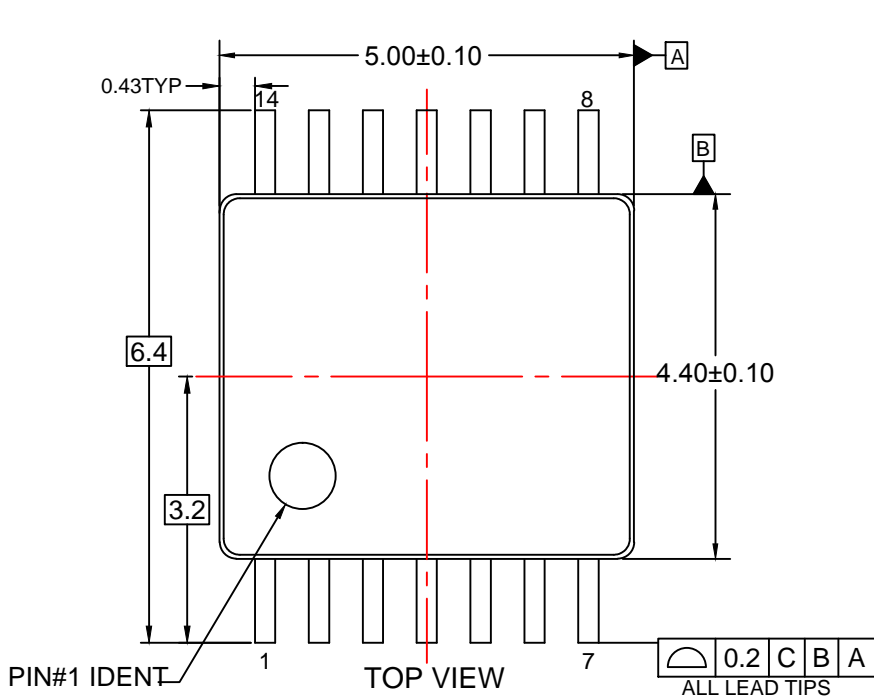
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is  $\pm 0.002[0.05]$  for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

### REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

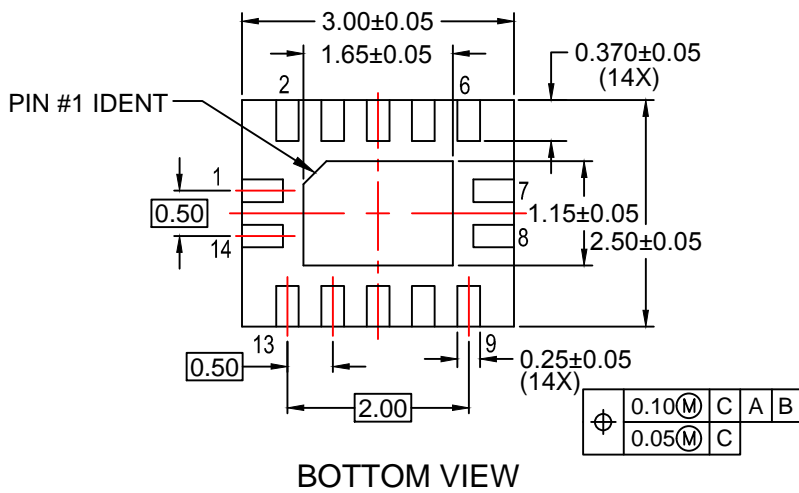
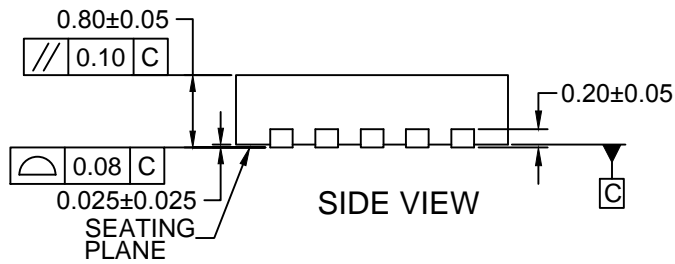
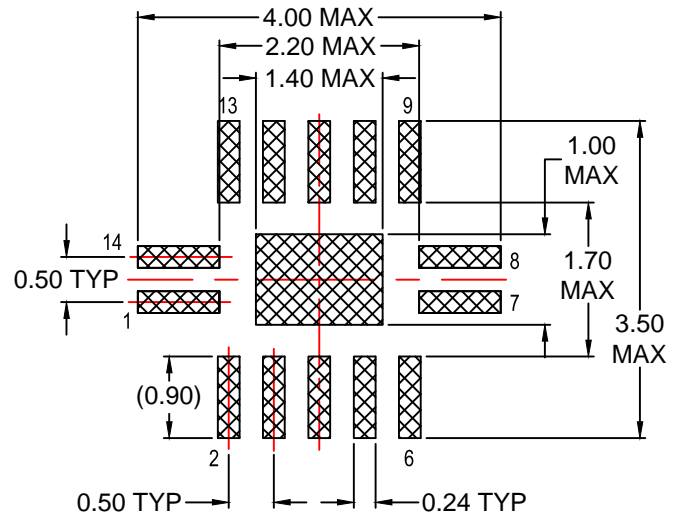
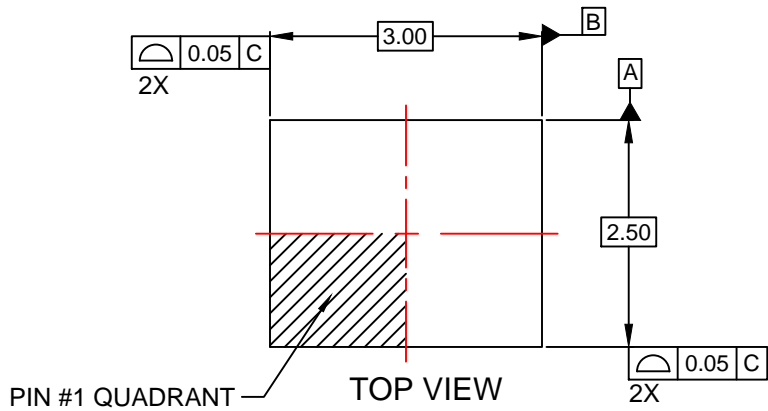




**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
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- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
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- E. LANDPATTERN STANDARD: SOP65P640X110-14M.
- F. DRAWING FILE NAME: MKT-MTC14rev7.





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[74HC85N](#) [NLU1G32AMUTCG](#) [NLV7SZ58DFT2G](#) [CD4068BE](#) [NL17SG32P5T5G](#) [NL17SG86DFT2G](#) [NLV14001UBDR2G](#)

[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [74LS38](#) [74LVC32ADTR2G](#) [MC74HCT20ADTR2G](#) [NLV17SZ00DFT2G](#) [NLV17SZ02DFT2G](#)

[NLV74HC02ADR2G](#) [74HC32S14-13](#) [74LS133](#) [74LVC1G32Z-7](#) [M38510/30402BDA](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#)

[NLV74HC08ADTR2G](#) [NLV74HC14ADR2G](#) [NLV74HC20ADR2G](#) [NLX2G86MUTCG](#) [5962-8973601DA](#) [74LVC2G02HD4-7](#)

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[NLX1G99DMUTWG](#) [NLVVHC1G00DFT2G](#) [NLVHC1G08DFT2G](#) [NLV7SZ57DFT2G](#) [NLV74VHC04DTR2G](#) [NLV27WZ86USG](#)

[NLV27WZ00USG](#) [NLU1G86CMUTCG](#) [NLU1G08CMUTCG](#) [NL17SZ32P5T5G](#) [NL17SZ00P5T5G](#) [NL17SH02P5T5G](#) [74AUP2G00RA3-7](#)

[NLV74HC02ADTR2G](#) [NLX1G332CMUTCG](#) [NL17SG86P5T5G](#) [NL17SZ05P5T5G](#)