



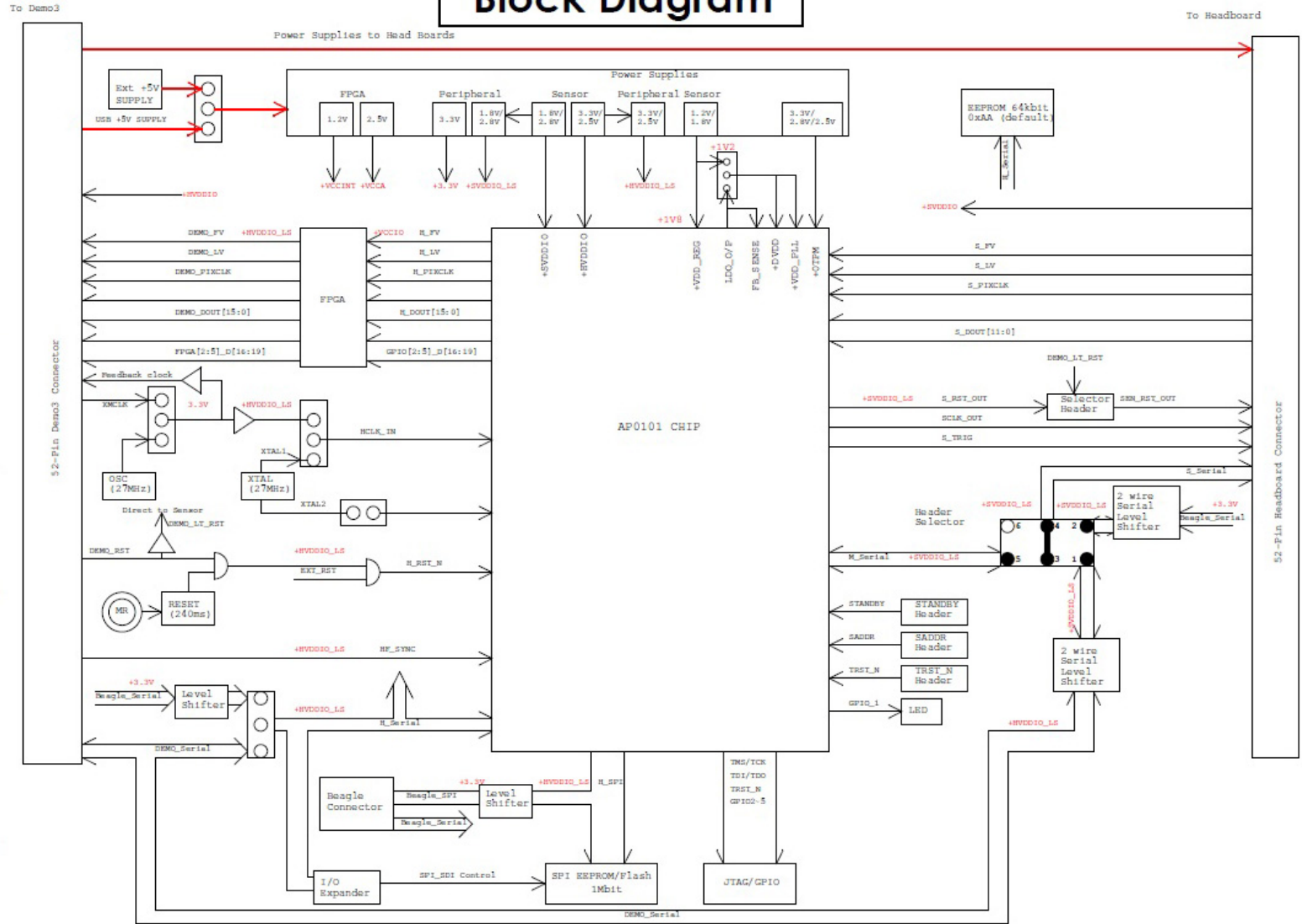
Schematic for the AP0101AT2L00XPGAH3-GEVB Evaluation Board

AP0101 HEADBOARD DEMO3 Card

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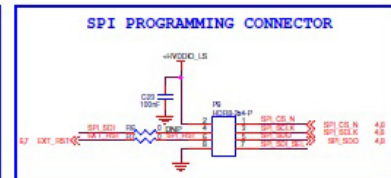
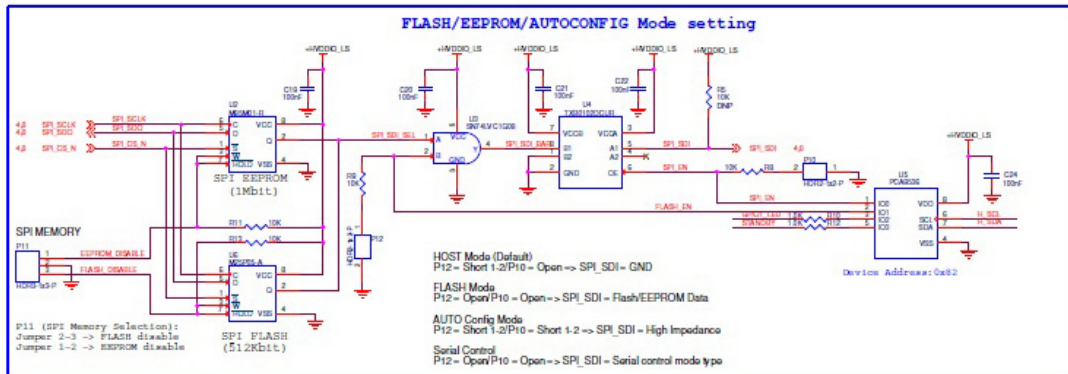
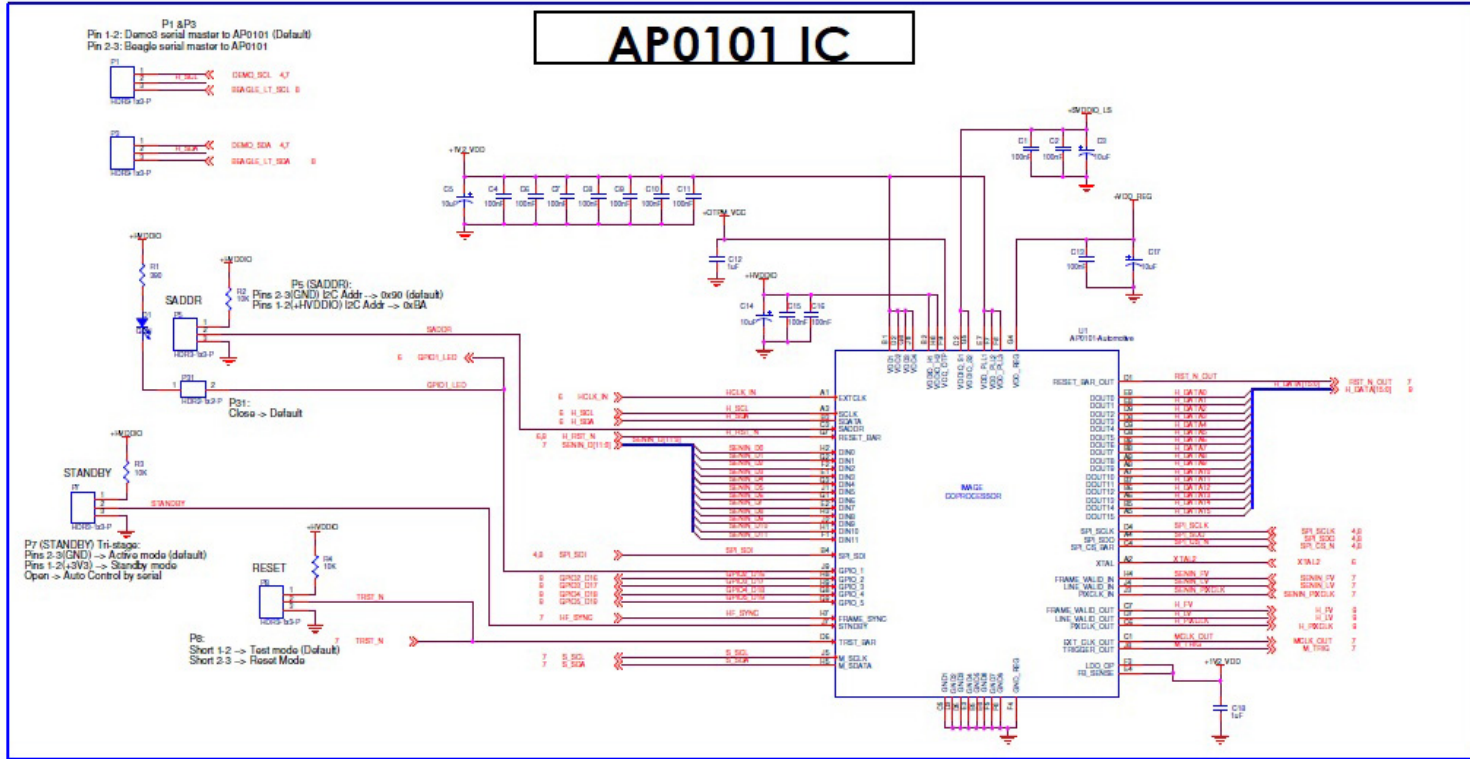
Rev	Who	Date	Description
Rev 0.0	skumar	06/02/15	Initial.Modified from AP0101_HEADBOARD Demo2
Rev 0.1	skumar	06/25/15	1. Added U58 Level shifter between Beagle and AP0101 2. Removed Header P62&P63 and replaced back with resistor R57&R58 3. Updated Block diagram
Rev 0.2	skumar	07/15/15	Deleted P2 and P4 (Removed the provision of external VDD supply for ISP) Text update and feedback clock connected to demo3 base board connector

Block Diagram



AP0101 IC PINOUT

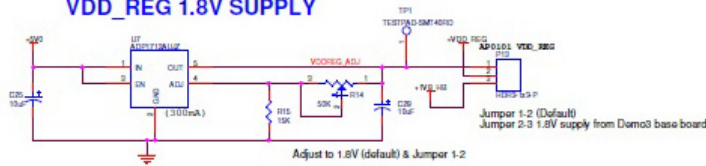
	1	2	3	4	5	6	7	8	9
A	EXTCLK	XTAL	SCLK	SPI_SDO	DOUT[15]	DOUT[13]	DOUT[10]	DOUT[9]	DOUT[8]
B	VDD	VDDIO_H	SDATA	SPI_SDI	DOUT[14]	DOUT[12]	DOUT[11]	DOUT[7]	DOUT[6]
C	EXT_CLK_OUT	VDDIO_S	SADDR	SPI_CS_BAR	GND	PIXCLK_OUT	FV_OUT	DOUT[5]	DOUT[4]
D	RESET_BAR_OUT	VDD	GND	SPI_SCLK	GND	TRST_BAR	LV_OUT	DOUT[3]	DOUT[2]
E	DIN[3]	DIN[7]	GND	FB_SENSE	GND	GND	VDD_PLL	DOUT[1]	DOUT[0]
F	DIN[11]	DIN[2]	LDO_OP	GND_REG	GND	GND	VDD_PLL	VDD_PLL	VDDIO_OTPM
G	DIN[6]	DIN[1]	DIN[4]	VDD_REG	VDDIO_S	VDD	RESET_BAR	GPIO[4]	GPIO[5]
H	DIN[10]	DIN[0]	DIN[8]	FV_IN	M_SDATA	VDDIO_H	FRAME_SYNC	GPIO[2]	GPIO[3]
J	DIN[5]	DIN[9]	PIXCLK_IN	LV_IN	M_SCLK	VDD	STANDBY	TRIGGER_OUT	GPIO[1]



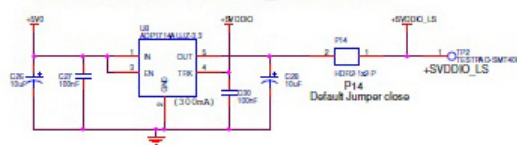
5	-VDD_REG	-VDDIO_REG
5.7	+VDDIO	+VDDIO
5.6	+VDD	+VDD
5.5	+VDDIO_LS	+VDDIO_LS
5.7.5.5	+VDDIO_LS	+VDDIO_LS
5	-VDDIO_VDD	-VDDIO_VDD

Power

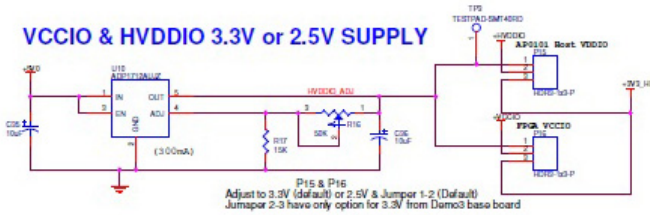
VDD_REG 1.8V SUPPLY



PERIPHERAL SVDDIO_LS SUPPLY



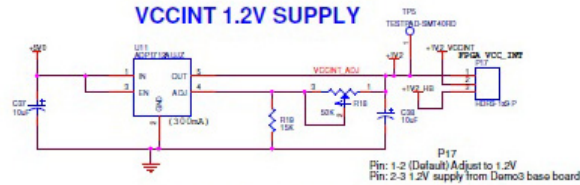
VCCIO & HVDDIO 3.3V or 2.5V SUPPLY



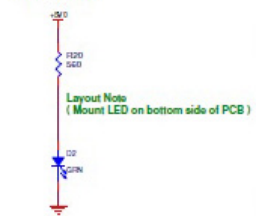
PERIPHERAL HVDDIO_LS SUPPLY



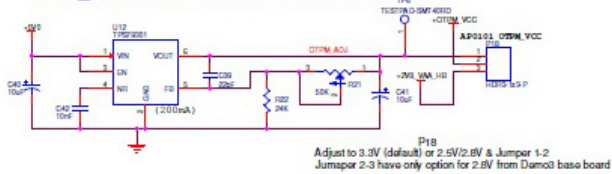
VCCINT 1.2V SUPPLY



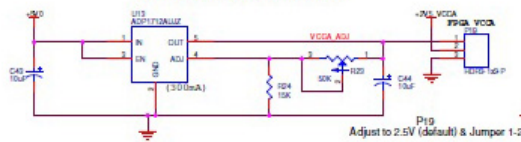
5V LED



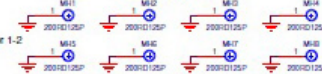
VDD_OTPM 3.3V, 2.8V or 2.5V SUPPLY



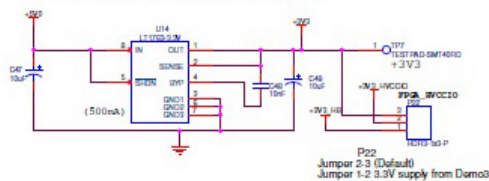
VCCA 2.5V SUPPLY



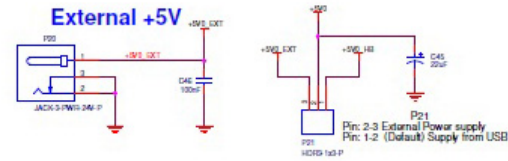
Mounting Holes



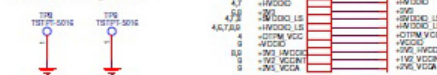
PERIPHERAL 3.3V SUPPLY



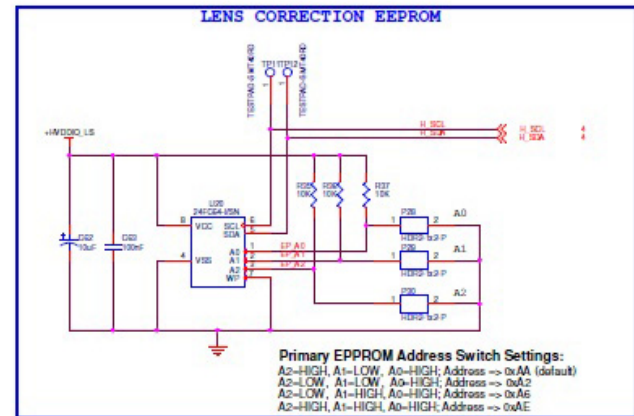
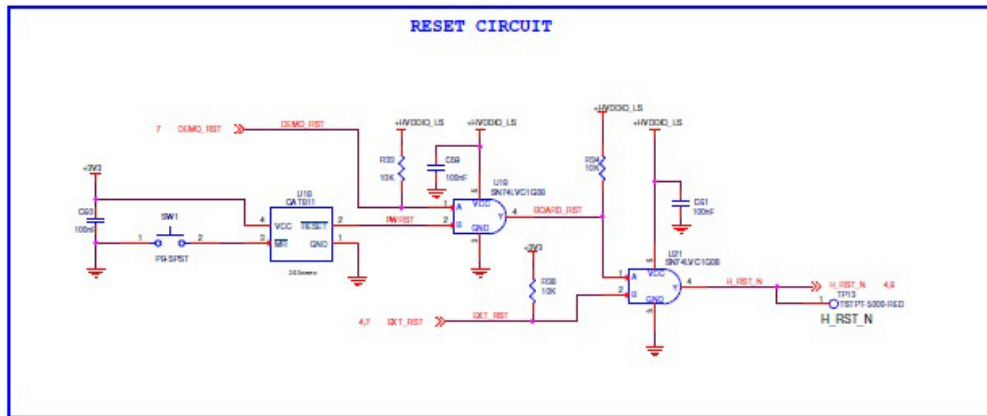
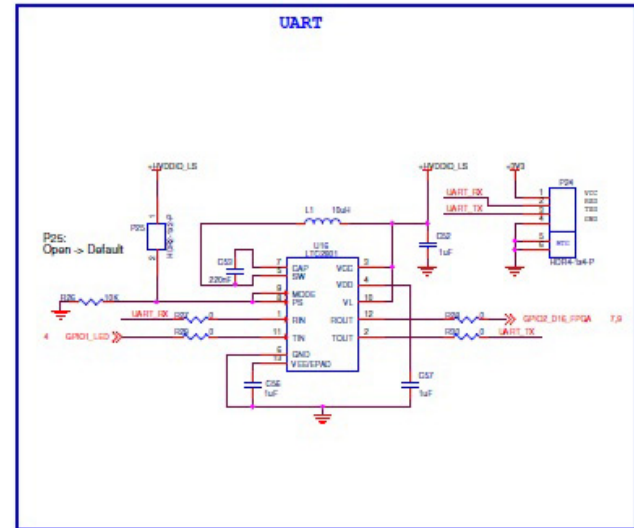
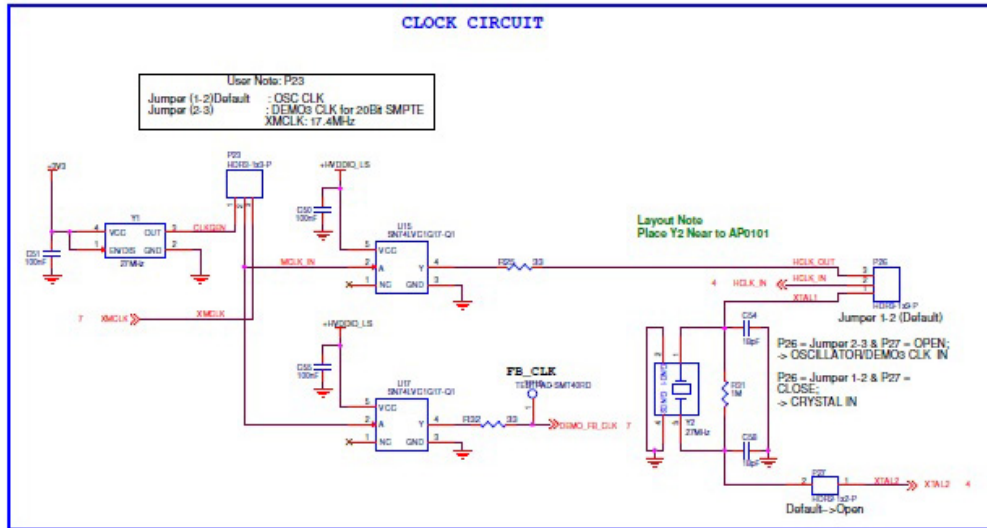
External +5V



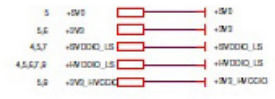
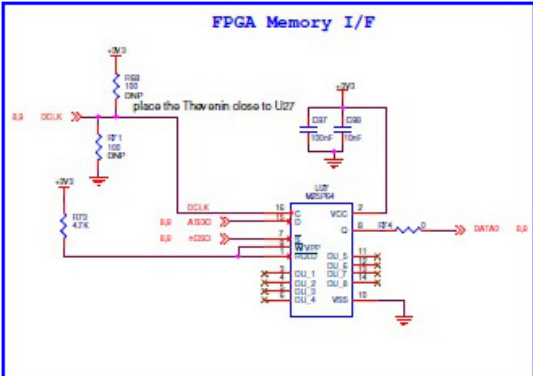
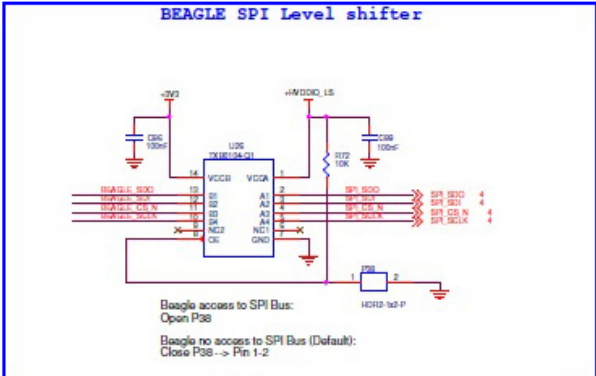
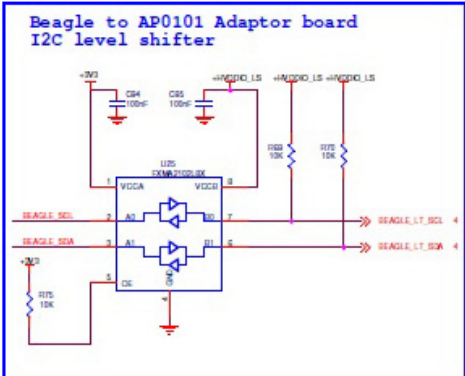
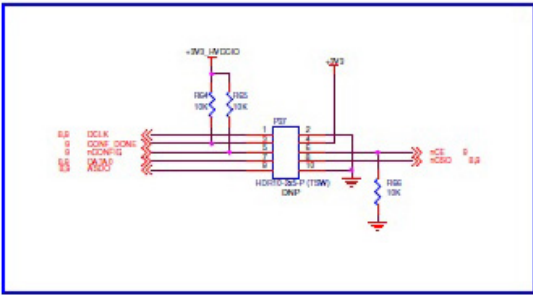
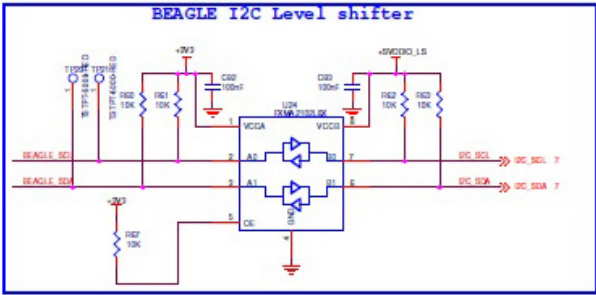
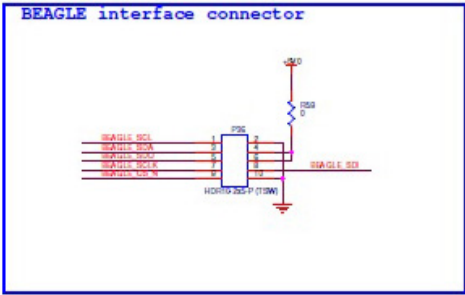
Ground Testpoints



Clock/Reset/UART



BEAGLE/FPGA EXT I/F



FPGA Interface





Configuration Setting

Beagle Serial configuration						
Header	Pin condition				Signal condition	Remark
	P33	P34	P1	P3		
P33/P34 &P1/P3	Short 1-3	Short 1-3	Short 1-2	Short 1-2	DEMO3_Serial -> Sensor_Serial/AP0101_Serial	Demo3 Master control ISP & headboard sensor
	Short 1-2	Short 1-2	Short 2-3	Short 2-3	Beagle_Serial -> Sensor_Serial/AP0101_Serial	Beagle Master control ISP & headboard sensor
	Short 3-5	Short 3-5	N/A	N/A	AP0101_Serial -> Sensor_Serial	AP0101 Master control headboard sensor
Auto configuration						
Header	Pin condition				Signal condition	Remark
P3B	Short 1-2				Disable U26	Beagle no access to SPI Bus
P12/P10	P12-Short 1-2/P10-Open				HOST Mode(SPI_SDI->GND)	
	P12-Open 1-2/P10-Open				Flash Mode(SPI_SDI-Flash/EEPROM Data)	
	P12-Short 1-2/P10-Short 1-2				Auto-Config(SPI_SDI-High Impedance)	

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