AP1302CSSL00SMGAH-GEVB

AP1302CS Evaluation Board User's Manual

ON Semiconductor®

EVAL BOARD USER'S MANUAL

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of image sensors products from ON Semiconductor. This headboard is intended to plug directly into the Demo 3 system. Test points and jumpers on the board provide access to the clock, I/Os, and other miscellaneous signals.

Features

- Clock Input
  - Default – 27 MHz Crystal Oscillator
  - Optional Demo 3 Controlled MClk
- Two Wire Serial Interface
  - Selectable Base Address
- Parallel Interface
- MIPI Interface
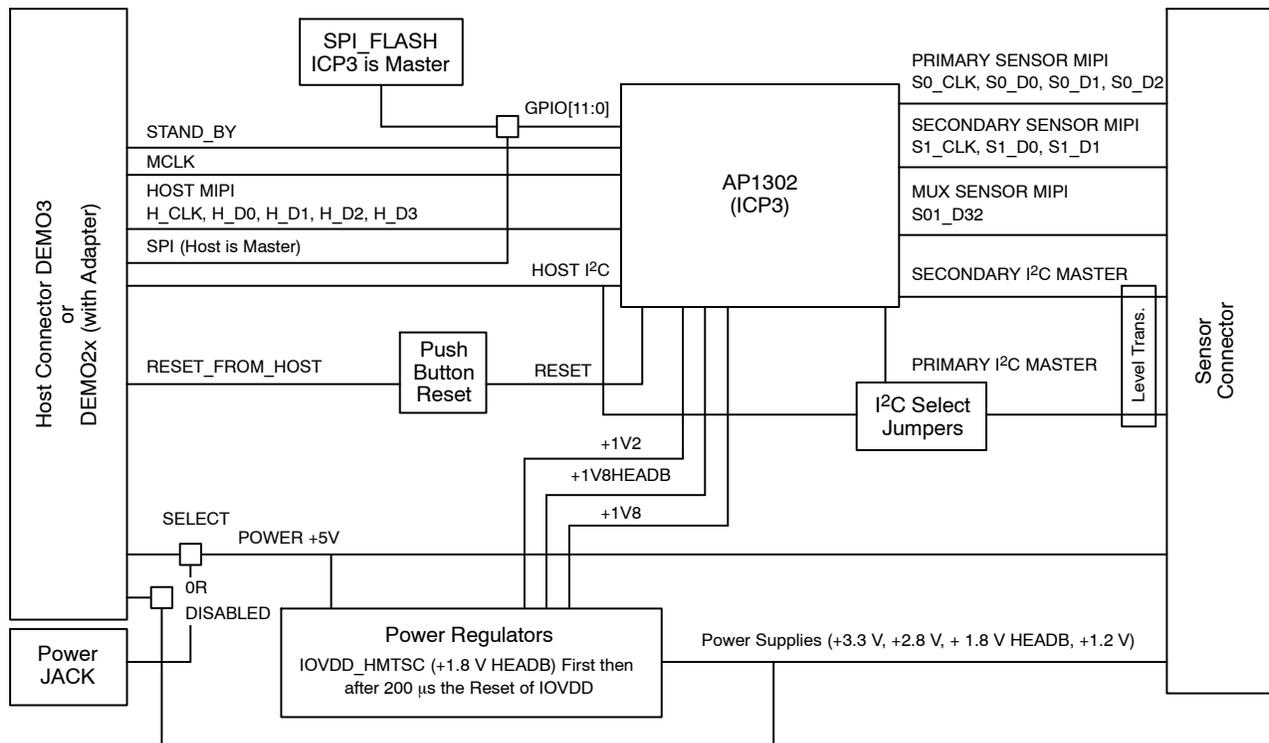- ROHS Compliant

Block Diagram

Figure 1. AP1302CS Evaluation Board

Figure 2. Block Diagram of AP1302CSSL00SMGAH−GEVB

AP1302CSSL00SMGAH−GEVB

Top View

CLK_SELECT **P3**
VBLOW **P15**

RESET Switch **SW1**
PRI_I2C_SCL **P6**
PRI_I2C_SDA **P5**

+5V0 Select **P1**
SPI_LS_EN **P24**
SPI Debug **P23**
I²C Debug **P4**
SEC_I2C_SCL **P12**
SEC_I2C_SDA **P13**

+1V8S **P8**
+1V2S **P7**
I2C_ID Select **P10**

+VDDIO_HB0_SENSE **P14**

+VDDIO_HB1_SENSE **P17**
+VDDIO_HEAD Select **P16**

Headboard Connector **P11**
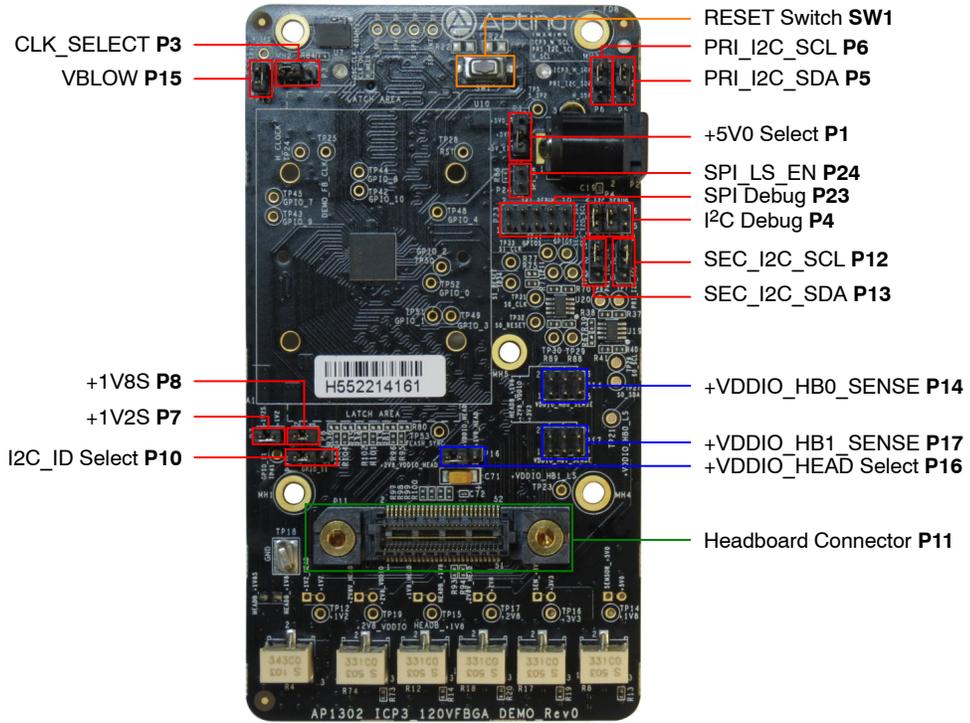
Figure 3. Top View of the Board – Default Jumpers

Bottom View

Baseboard Connector **J1**

+HEADB_1V8S **P9**
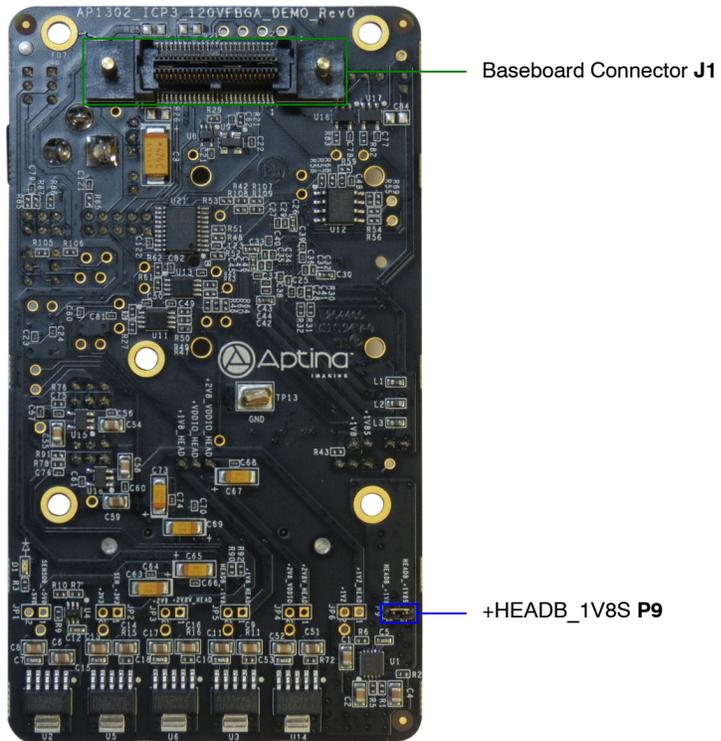
Figure 4. Bottom View of the Board – Connectors

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.
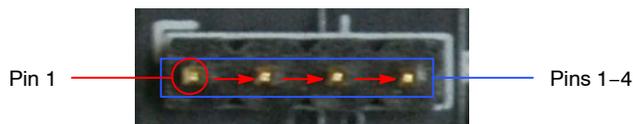

Figure 5. Pin Locations for a Single Jumper. Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right
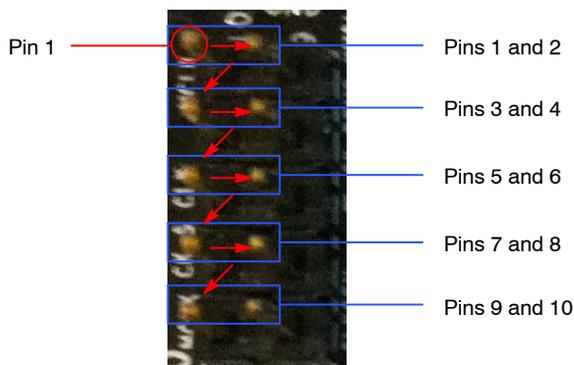

**Figure 6. Pin Locations and Assignments of Grouped Jumpers.
Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture**

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

Jumper/Header No.	Jumper/Header Name	Pins	Description
P1	+5V0 Select	1−2 (Default)	Use +5V Supply Source from External Power Adapter
		2−3	Use +5V Supply Source from Demo 3 Baseboard
P3	CLK_SELECT	2−3 (Default)	Select On-board 48 MHz Oscillator Clock
		1−2	Select Clock from Demo 3 Baseboard
P4	I^{2}C Debug	1−2 & 3−4 (Default)	Connect to Demo 3 Baseboard I^{2}C Interface
		Open	For Connection to External I^{2}C Debugger Interface
P5	PRI_I2C_SCL	1−2 (Default)	Connect to ICP3 Master SCL
		2−3	Connect to Host SCL
P6	PRI_I2C_SCL	1−2 (Default)	Connect to ICP3 Master SDA
		2−3	Connect to Host SDA
P7	+1V2S	Closed (Default)	Normal Operation
P8	+1V8S	Closed (Default)	Normal Operation
P9	+HEADB_1V8S	Closed (Default)	Normal Operation
P10	I2C_ID Select	1−2 (Default)	ICP3 I^{2}C Address Set to 0x78
		2−3	ICP3 I^{2}C Address Set to 0x7A
P12	SEC_I2C_SCL	1−2 (Default)	Connect to ICP3 GPIO6 (2ND_I2C_SCL)
		2−3	Connect to PRI_I2C_SCL
P13	SEC_I2C_SDA	1−2 (Default)	Connect to ICP3 GPIO6 (2ND_I2C_SDA)
		2−3	Connect to PRI_I2C_SDA

Table 1. JUMPERS AND HEADERS (continued)

Jumper/Header No.	Jumper/Header Name	Pins	Description
P14	+VDDIO_HB0_SENSE	1−2 (Default)	Sets Voltage to +1.8 V (Normal Operation)
		3−4	Sets Voltage to +2.8 V
		5−6	Sets Voltage to +3.3 V
P15	VBLOW	Closed (Default)	Normal Operation
P16	+VDDIO_HEAD Select	2−3 (Default)	When using with the Demo 3 Headboard
		1−2	When using with the AP21057 Dual Adapter Board
P17	+VDDIO_HB1_SENSE	1−2 (Default)	Sets Voltage to +1.8 V (Normal Operation)
		3−4	Sets Voltage to +2.8 V
		5−6	Sets Voltage to +3.3 V
P23	SPI Debug	Open (Default)	SPI Interface Disabled
		1−2, 3−4, 5−6, 7−8	SPI Interface Enabled
P24	SPI_LS_EN	Open (Default)	SPI Level-shifter Disabled
		1−2	SPI Level-shifter Enabled
SW1	RESET	N/A	When Pushed, 240 ms Reset Signal will be Sent to AP1302

Interfacing to ON Semiconductor Demo 3 Baseboard

The ON Semiconductor Demo 3 baseboard has a similar 52-pin connector which mates with J1 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

Shorted Jumpers for Power Measurement

Different supplies to the evaluation board are provided by trace shorted jumper, for any voltage and power measurements. To conduct current for current measurement on a given power rail, cut the trace between the two pins of their respective JP, and insert an ammeter prior to powering up the system. The figure below shows where the trace to cut is located.
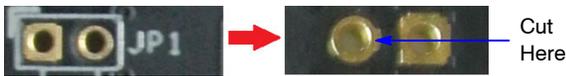
Figure 7. Top and Bottom View of Shorted Jumper. The Bottom View Shows the Trace Location to Cut for Current Measurement

Table 2. SHORTED JUMPERS FOR POWER MEASUREMENT

Jumper	Voltage (V)
P1, Pin 1 (+5V0_EXT)	5.0
P1, Pin 2 (+5V0)	5.0
P1, Pin 3 (+5V0_HOST)	5.0
TP12 (+1V2)	1.2
TP14 (+1V8)	1.8
TP15 (+HEAD_1V8)	1.8
TP16 (+3V3)	3.3
TP17 (+2V8_VAA)	2.8
TP19 (+2V8_VDDIO)	2.8
TP21 (+VDDIO_HB0_LS)	1.8/2.8/3.3
TP23 (+VDDIO_HB1_LS)	1.8/2.8/3.3

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