

AR0144_CSP_Demo3Head

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Rev	Who	Date	Description
Rev 0.0	Joe KK	05/07/12	Initial
Rev 0.1	skumar	10/26/15	Initial
Rev 0.2	skumar	11/04/15 11/09/15	- Replaced C&K switch (PTS635SL25SMTRLFS) with TE switch part 147873-2 - Swapped parallel data signal at RP1,RP2,RP3 and RP4

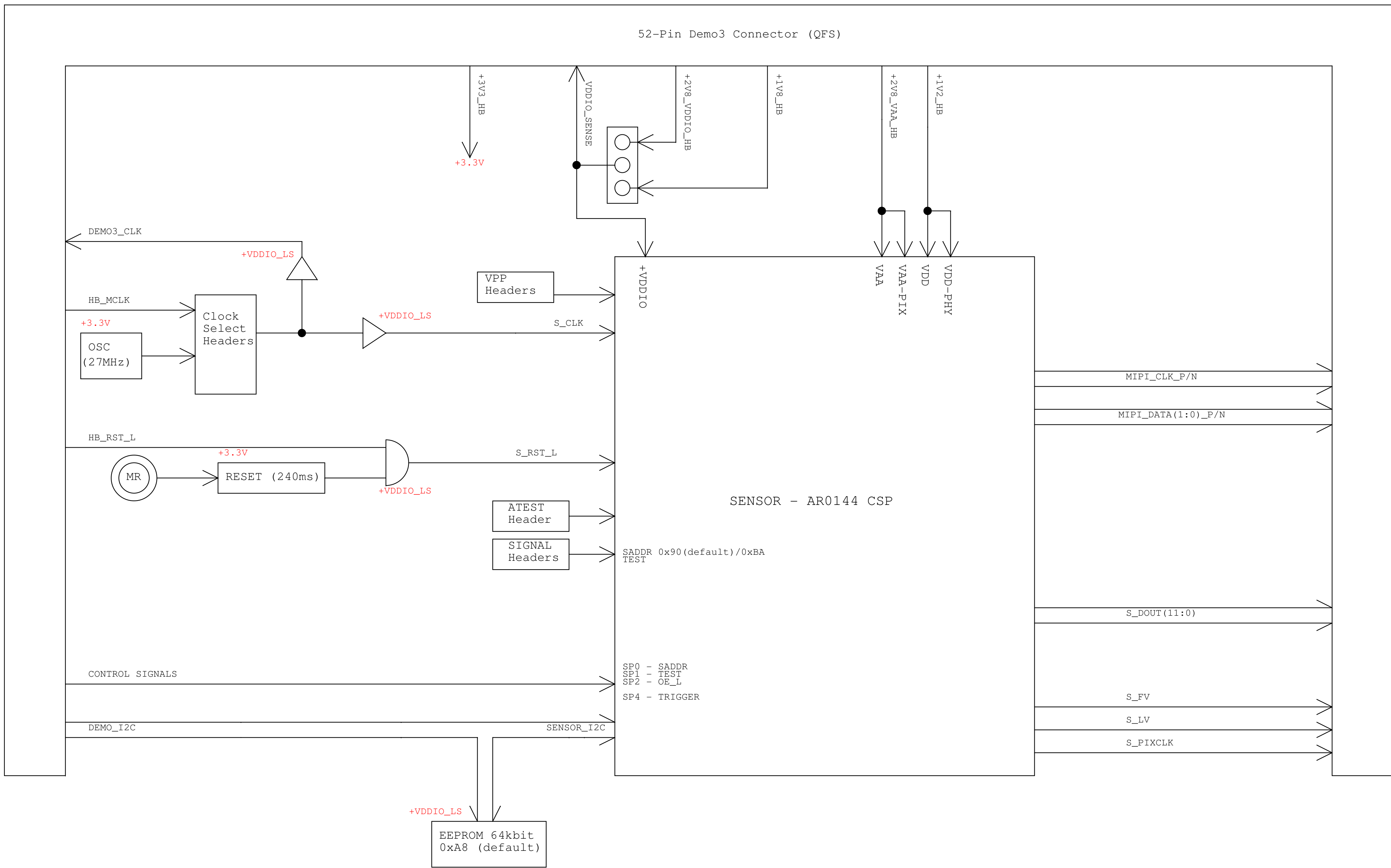



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Title
Title Page

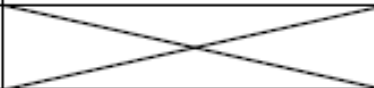
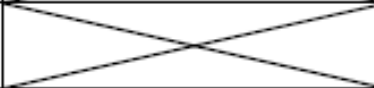
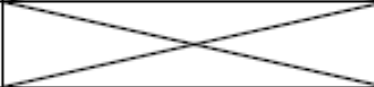
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Block Diagram



		
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Pinout

	1	2	3	4	5	6	7	8	9
A	DGND	VDDIO2V8R1V8	DVDD1V2	DATA1_P	CLK_P	DATA0_P	SHUTTER	TEST	
B	LINE_VALID	DVDD1V2	EXTCLK	DATA1_N	CLK_N	DATA0_N	SADDR	VDDIO2V8R1V8	
C	DOUT11	VDDIO2V8R1V8	PIXCLK	FRAME_VALID	DVDD1V2PHY	DVDD1V2	SCL	VDDIO2V8R1V8	
D	DOUT7	DOUT8	DOUT9	DOUT10	DGND	DGND	OUTPUT_ENABLE_N	DVDD1V2	AGND
E	DOUT5	DOUT6	VDDIO2V8R1V8	DOUT4	DOUT3	SDA	TRIGGER	DGND	VAAHV_NPIX
F	DGND	DVDD1V2	DOUT2	DOUT1	DOUT0	FLASH	DGND	DGND	VAAPIX_2V8
G	RESET_N	VAA2V8	AGND	DVDD1V2	DVDD1V2	DVDD1V2	AGND	VAA2V8	ATEST
H	VAA2V8	VAA2V8	AGND	DGND	DGND	DGND	AGND	VAA2V8	VAA2V8

TOP SIDE VIEW

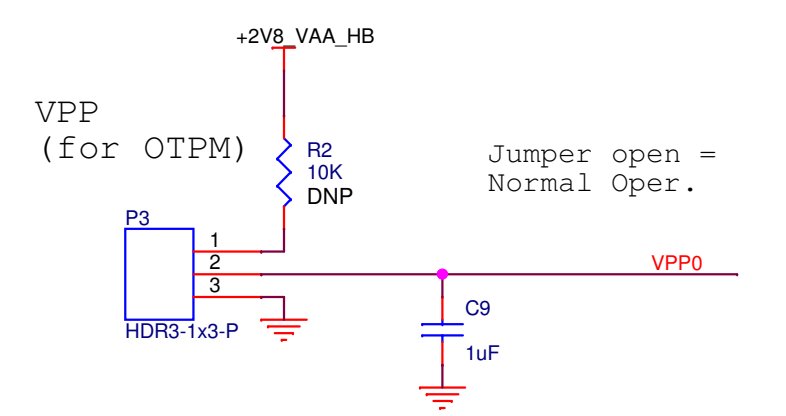
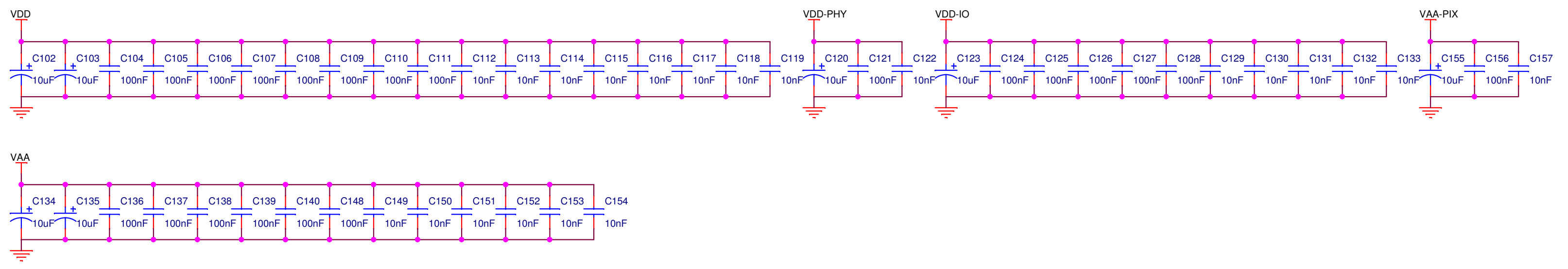


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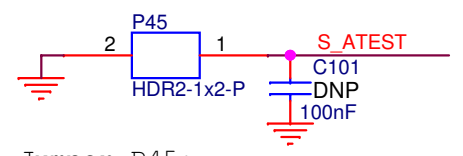
Sensor

+5V0		+5V0	5
+3V3		+3V3	5,6
+VDDIO_LS		+VDDIO_LS	5,6,7
5	VDD	VDD	
5	VDD-PHY	VDD-PHY	
5	VDD-IO	VDD-IO	
5	VAA	VAA	
5	VAA-PIX	VAA-PIX	

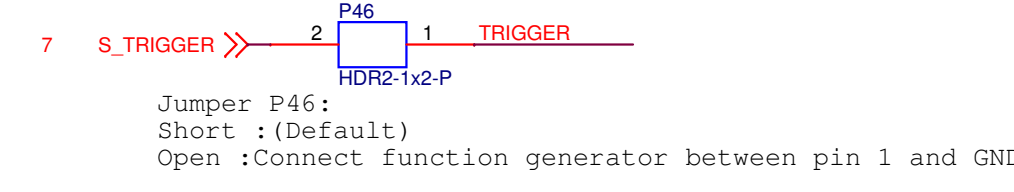


Layout Note

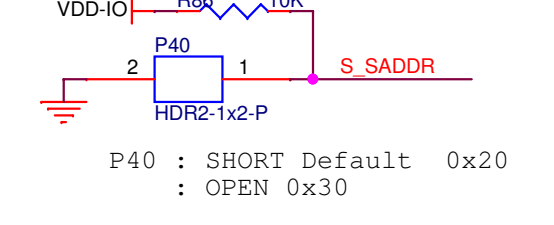
Place C101 near BGA Pin ATEST1



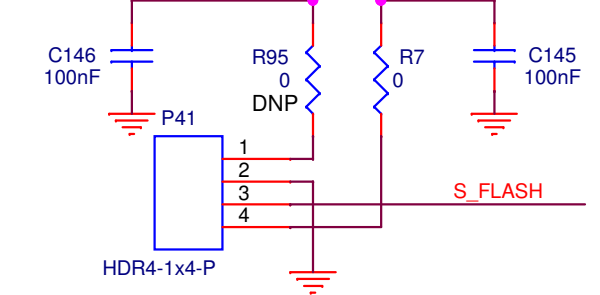
TRIGGER



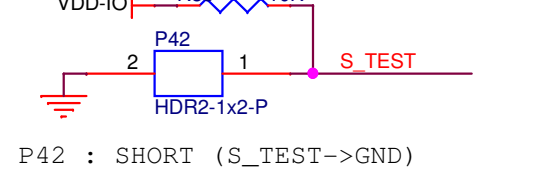
SADDR



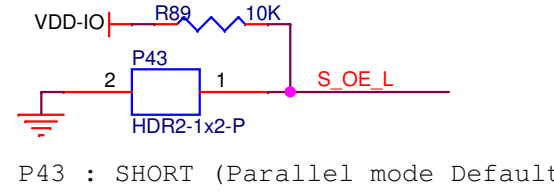
FLASH



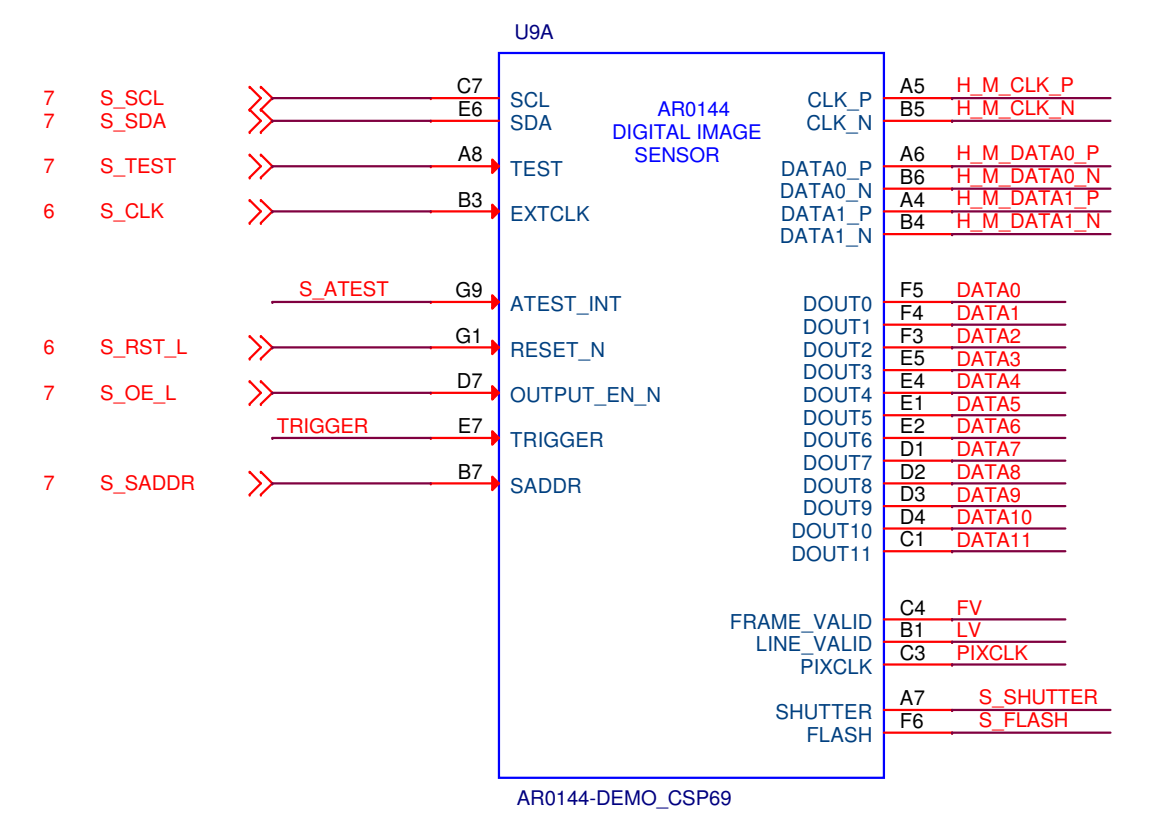
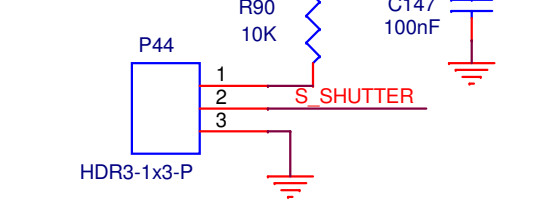
TEST



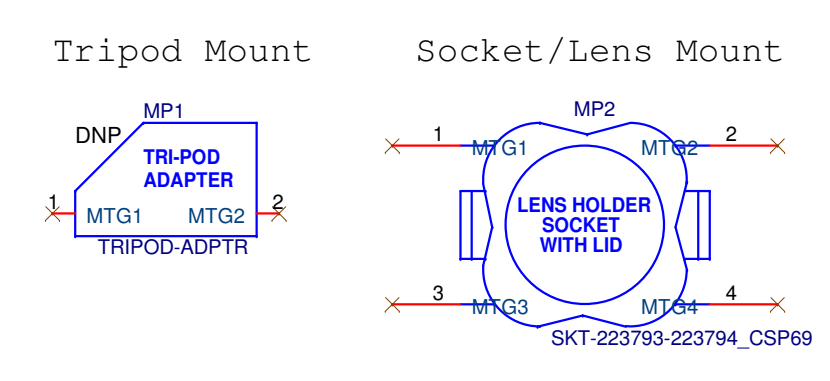
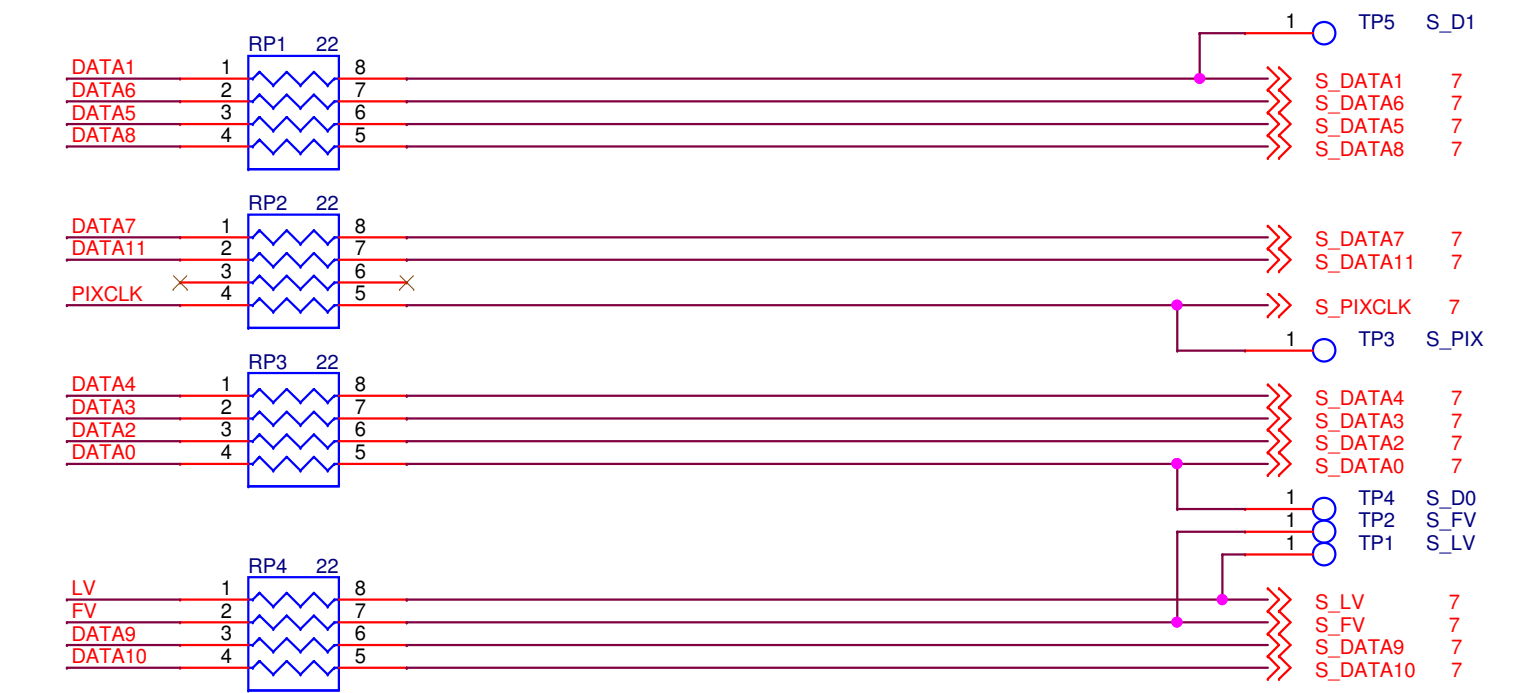
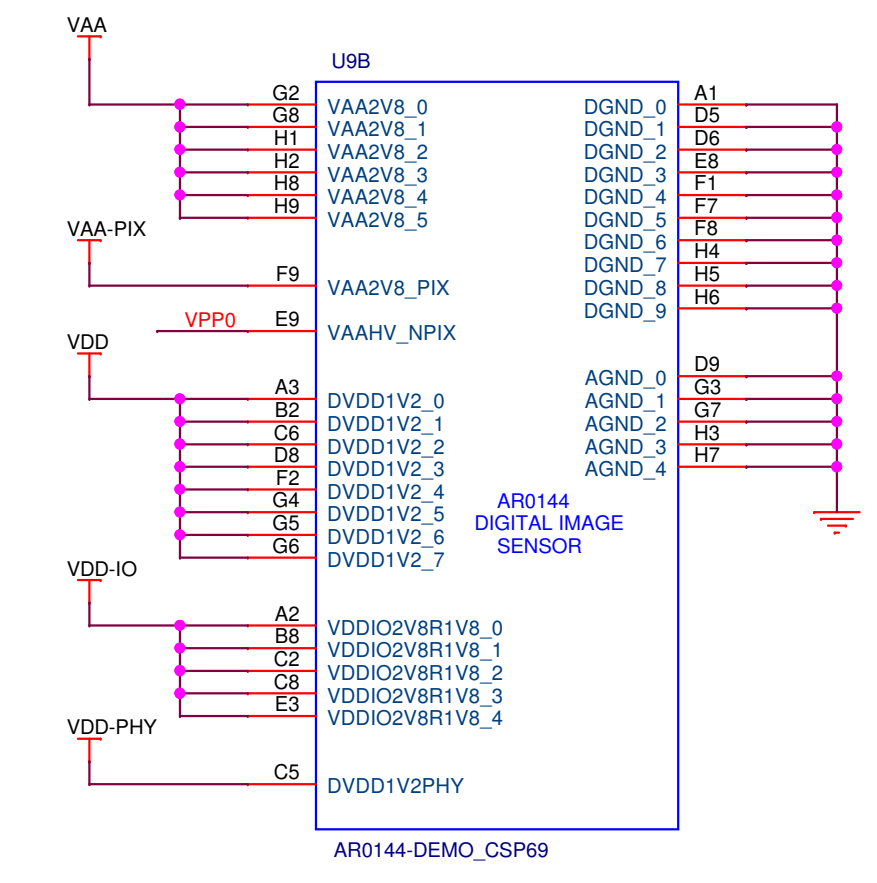
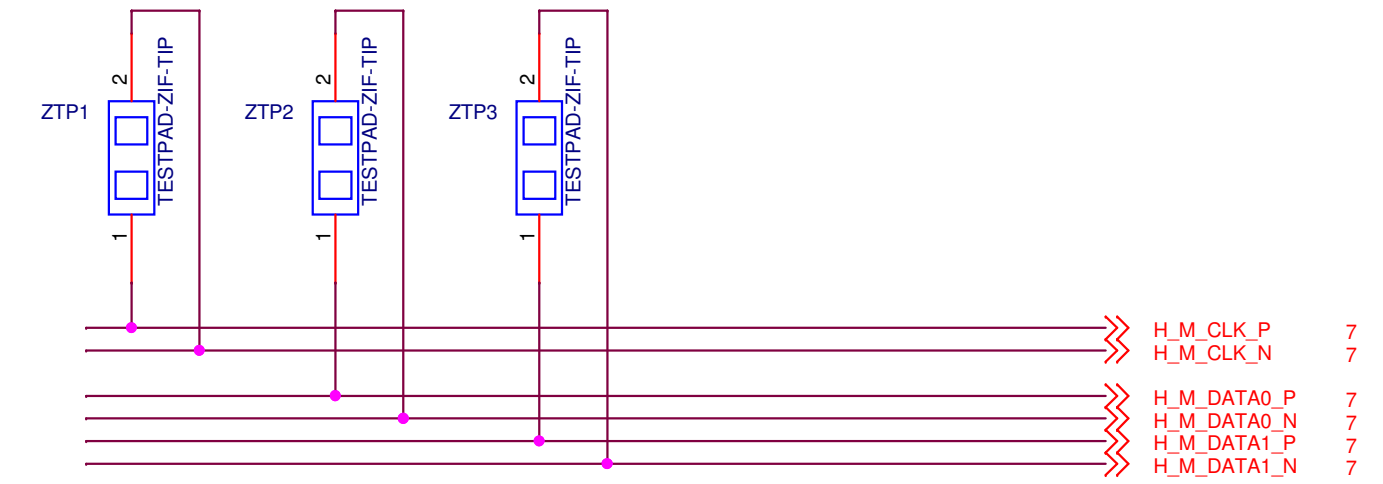
OE_L



SHUTTER



(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)



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Title: Sensor

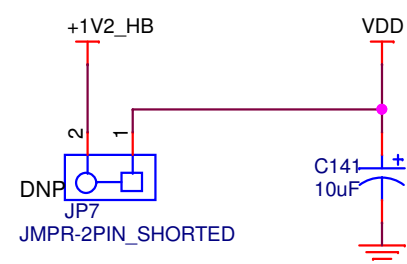
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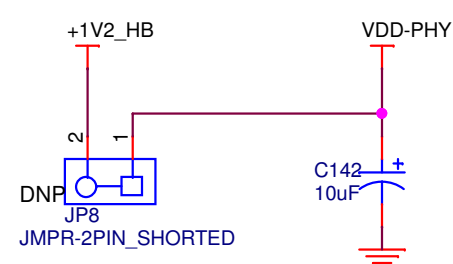
Debug Headers: Cut away the shorted trace and mount header for power debugging

Power

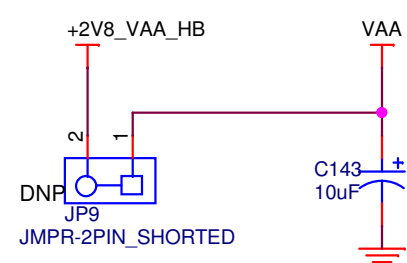
VDD 1.2V SUPPLY



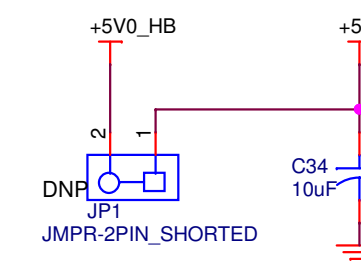
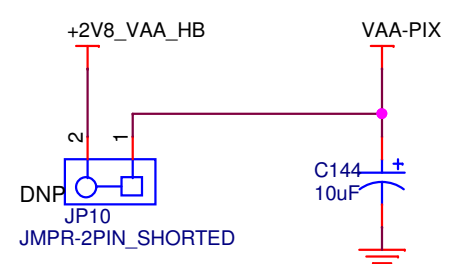
VDD-PHY 1.2V SUPPLY



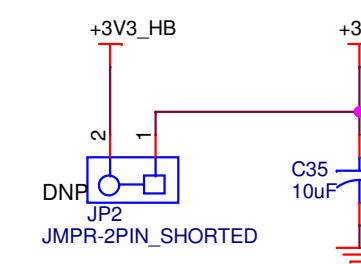
VAA 2.8V SUPPLY



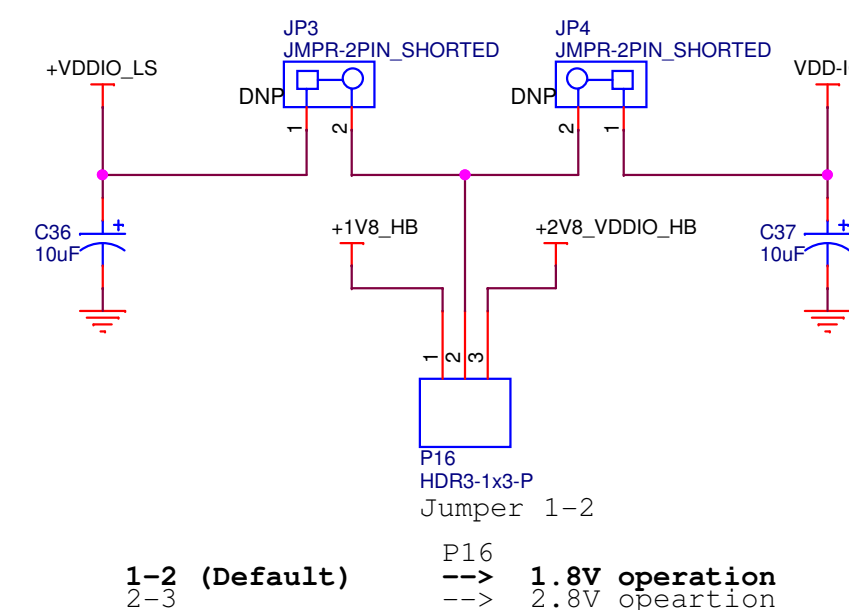
VAA-PIX 2.8V SUPPLY



PERIPHERAL 3.3V SUPPLY

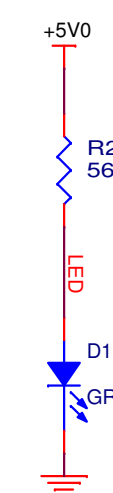


VDDIO & VDDIO_LS 1.8V/2.8V SUPPLY

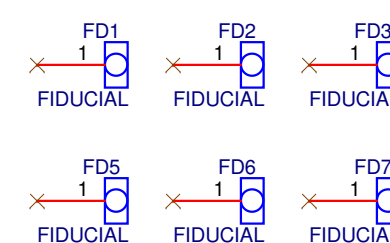


+5V0_HB	7	+5V0_HB	7
+3V3_HB	7	+3V3_HB	7
+2V8_VAA_HB	4,7	+2V8_VAA_HB	4,7
+2V8_VDDIO_HB	7	+2V8_VDDIO_HB	7
+1V8_HB	7	+1V8_HB	7
+1V2_HB	7	+1V2_HB	7
+5V0	4	+5V0	4
+3V3	4,6	+3V3	4,6
+VDDIO_LS	6,7	+VDDIO_LS	6,7
4	VDD	VDD	
4	VDD-PHY	VDD-PHY	
4	VDD-IO	VDD-IO	
4	VAA	VAA	
4	VAA-PIX	VAA-PIX	

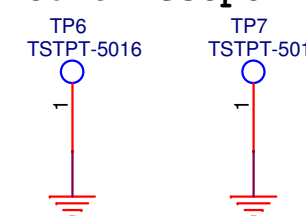
5V LED



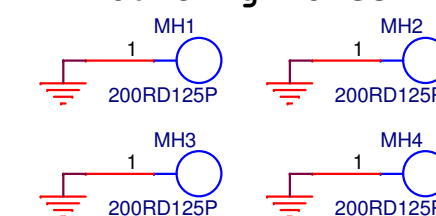
Layout Note
(Mount LED on
bottom side of PCB)




Ground Testpoints



Mounting Holes





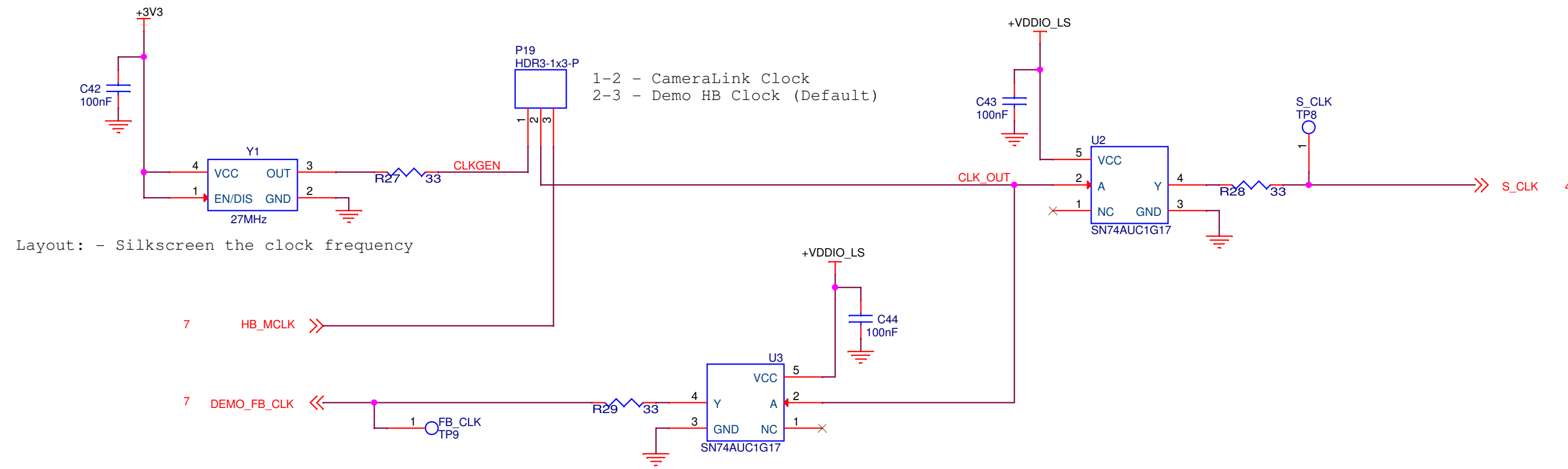
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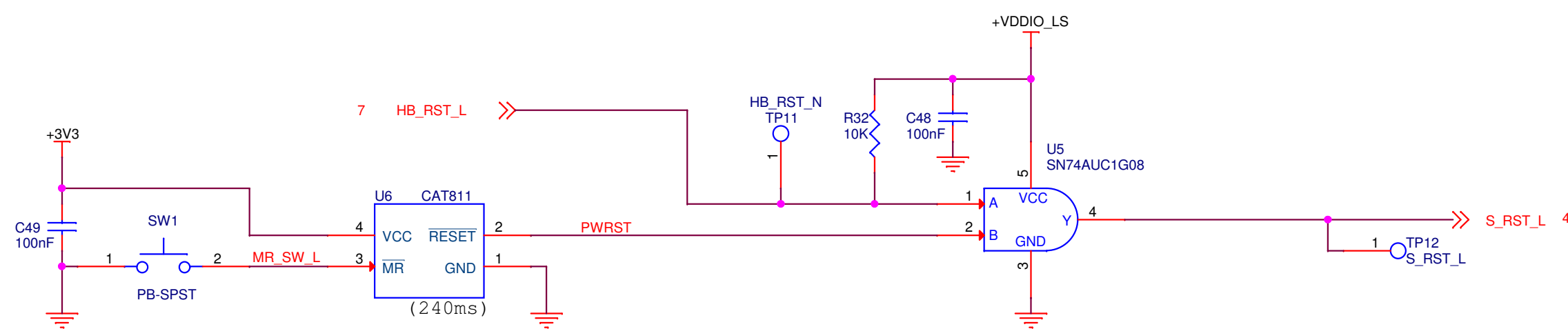
Clock and Reset

+5V0	4,5
+3V3	4,5
+VDDIO_LS	5,7

CLOCK CIRCUIT



RESET CIRCUIT



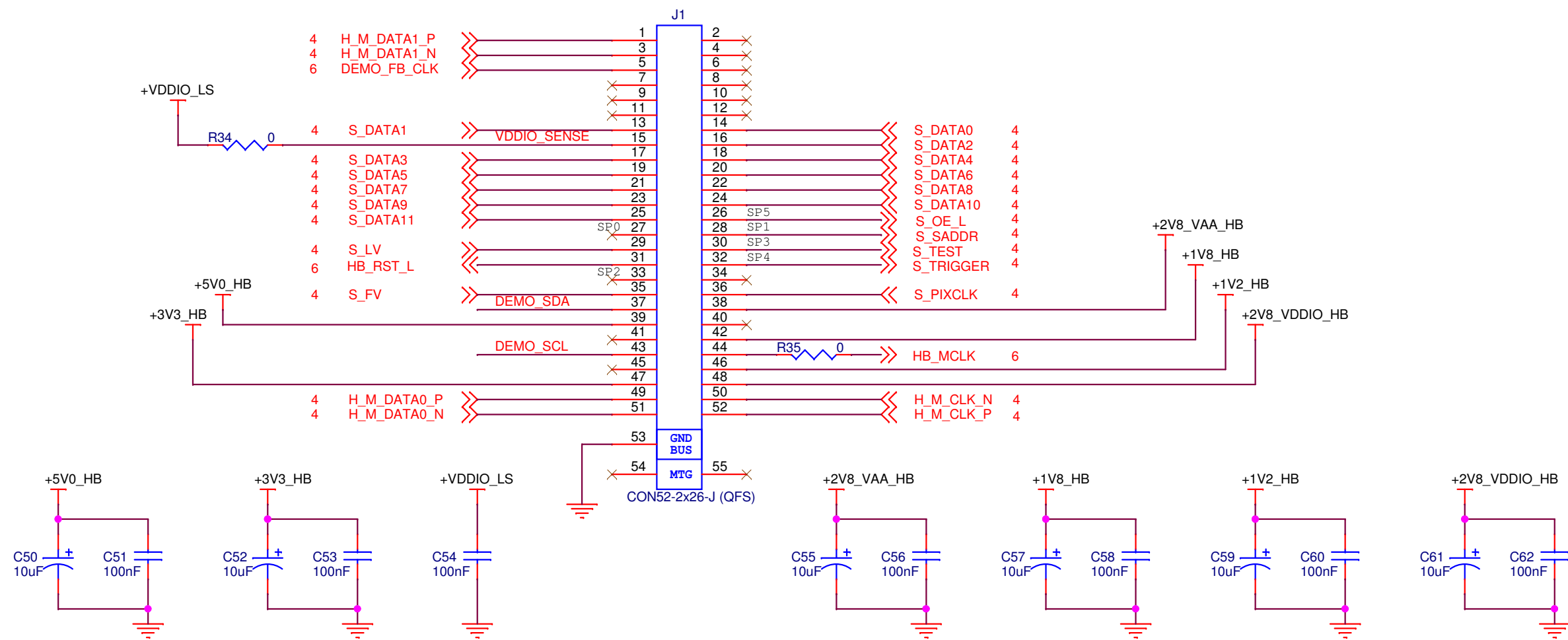
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Title Clock and Reset		
Size C	Document Name AR0144-CSP_Demo3Head	Rev 0.2
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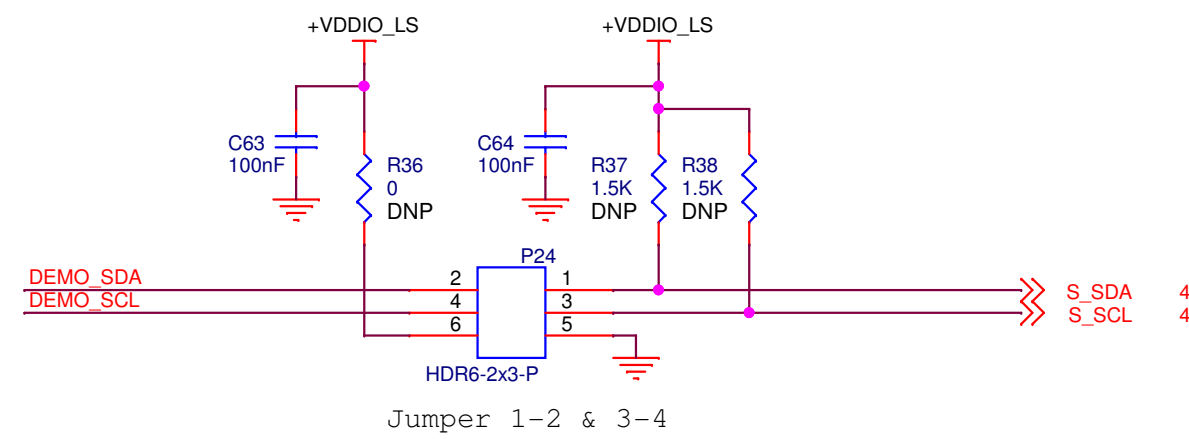
External Interface

+5V0_HB	5	+5V0_HB	5
+3V3_HB	5	+3V3_HB	5
+2V8_VAA_HB	4,5	+2V8_VAA_HB	4,5
+2V8_VDDIO_HB	5	+2V8_VDDIO_HB	5
+1V8_HB	5	+1V8_HB	5
+1V2_HB	5	+1V2_HB	5
+3V3_VDDIO_LS	4,5,6	+3V3_VDDIO_LS	4,5,6
+VDDIO_LS	5,6	+VDDIO_LS	5,6

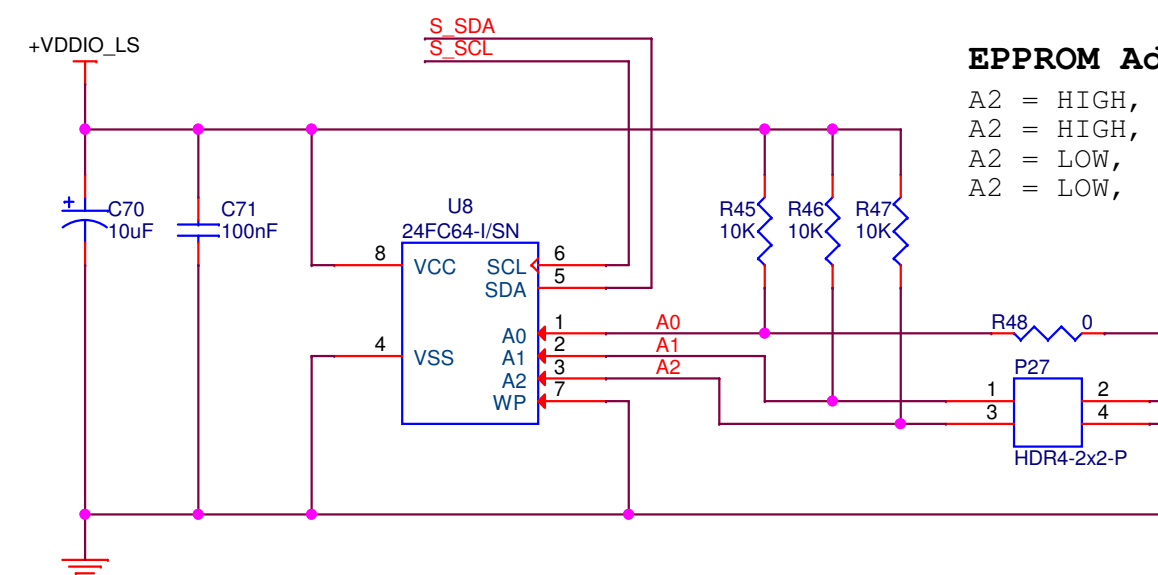
DEMO3 BASEBOARD I/F



I2C DEBUG



LENS CORRECTION EEPROM



EPPROM Address Switch Settings:
 A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
 A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
 A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
 A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0



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Title: External Interface		
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