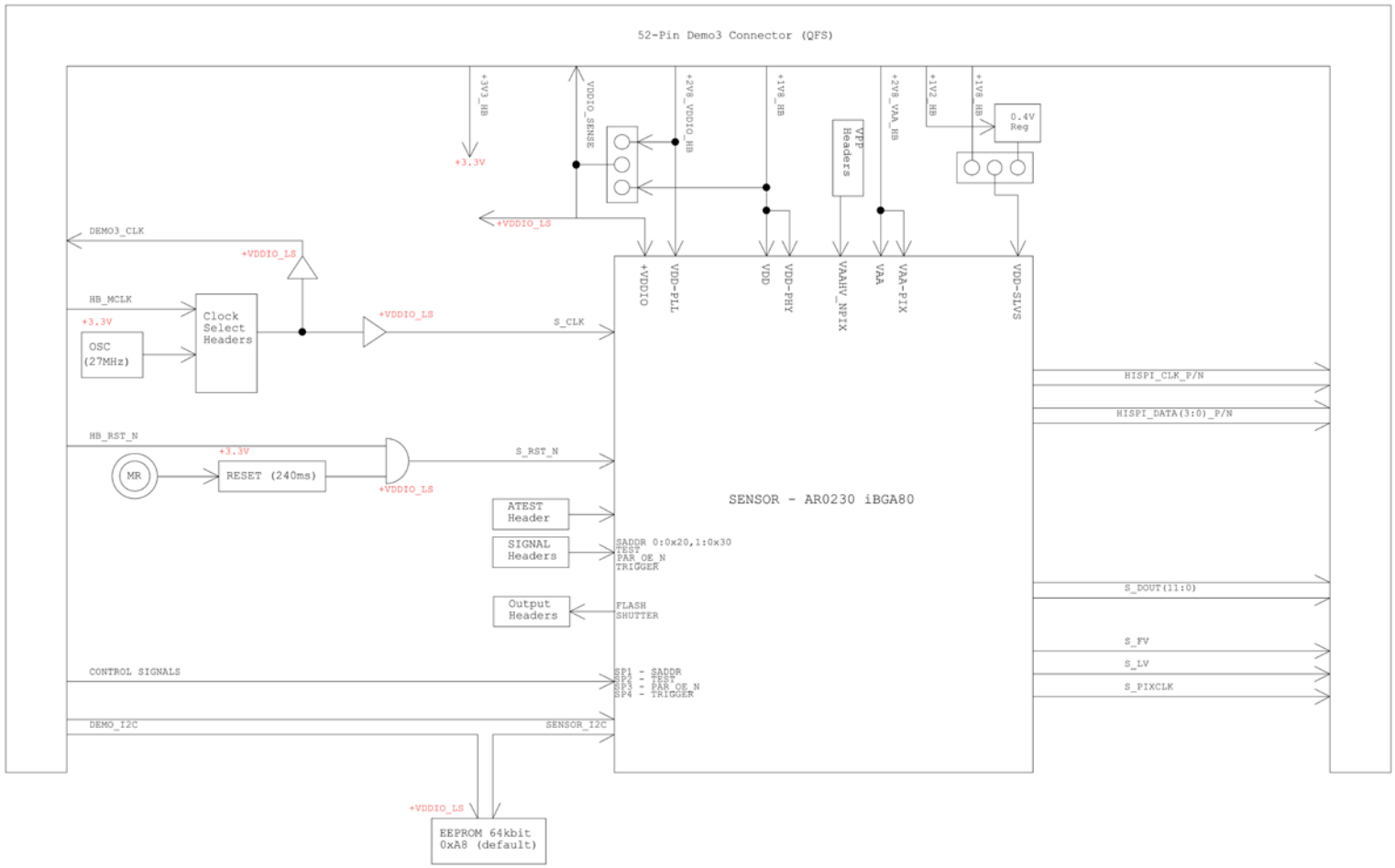
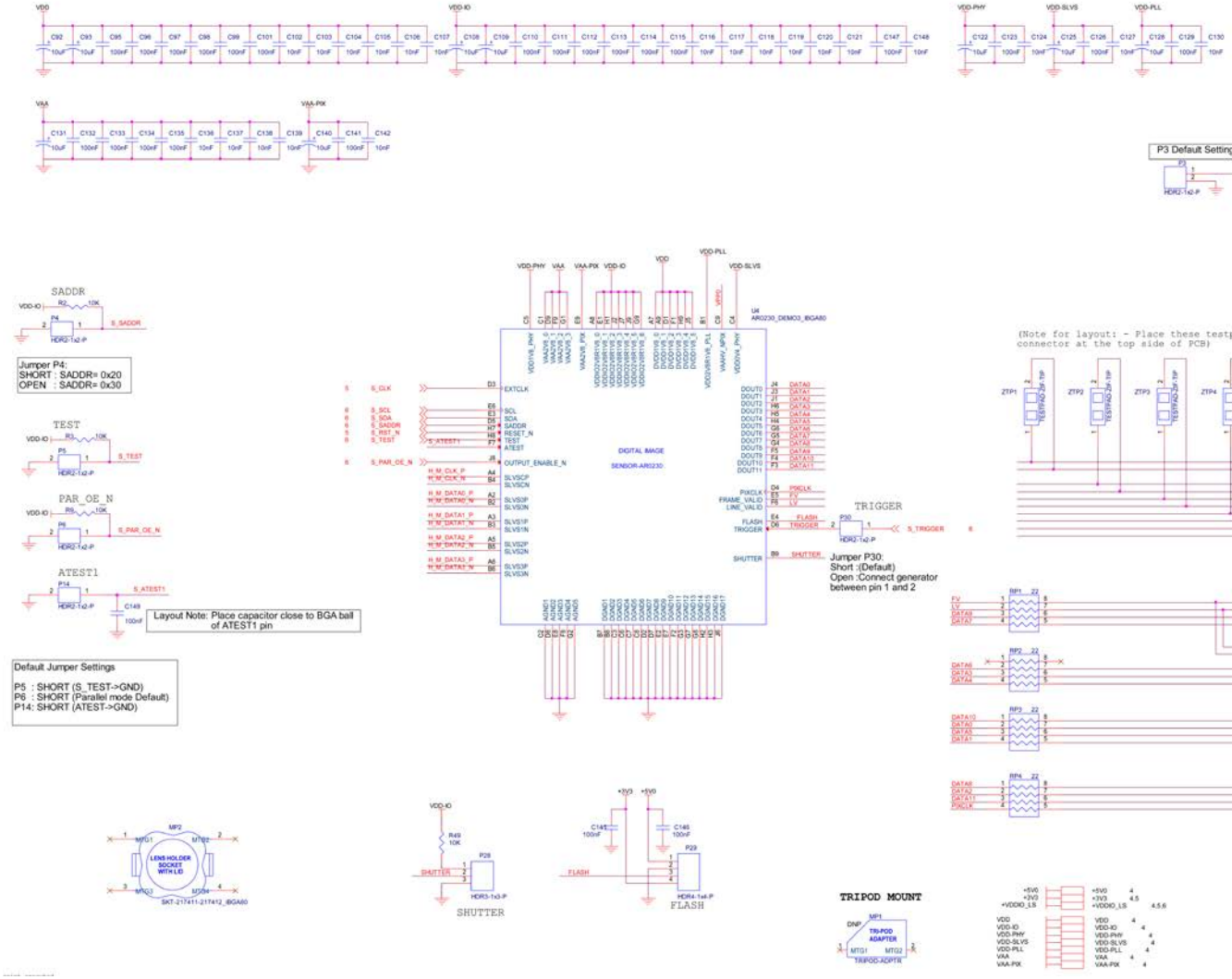
ON Semiconductor®

Schematic for the AR0230CSSC00SUEAH3-GEVB Evaluation Board

Block Diagram



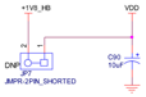
Sensor


P3 Default Setting: Open
SADDR
Jumper P4:
SHORT : SADDR= 0x20
OPEN : SADDR= 0x30
TEST
PAR_OE_N
ATEST1
Layout Note: Place capacitor close to BGA ball of ATEST1 pin
Default Jumper Settings
P5 : SHORT (S_TEST->GND)
P6 : SHORT (Parallel mode Default)
P14: SHORT (ATEST->GND)
(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)
TRIGGER
Jumper P30:
Short :(Default)
Open :Connect generator between pin 1 and 2
SHUTTER
FLASH
TRIPOD MOUNT

Debug Headers: Cut away the shorted trace and mount header for power debugging

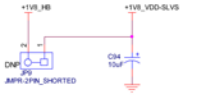
Power

VDD 1.8V SUPPLY

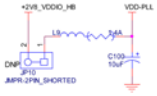


VDD-PHY 1.8V SUPPLY

VDD-SLVS 1.8V SUPPLY

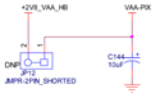


VDD-PLL 2.8V SUPPLY



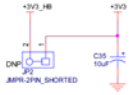
VAA 2.8V SUPPLY

VAA-PIX 2.8V SUPPLY

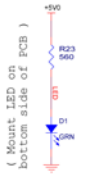


PERIPHERAL 5V SUPPLY

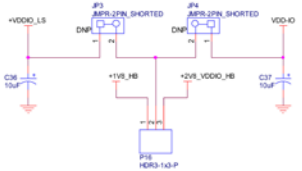
PERIPHERAL 3.3V SUPPLY



5V LED

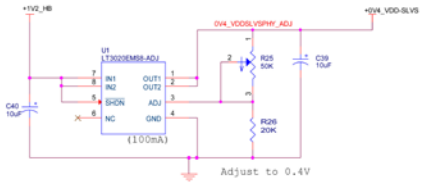


VDDIO & VDDIO_LS 1.8V/2.8V SUPPLY



P16 Default Setting: 1-2 Short (1V8 operation)

VDD_SLVS 0.4V SUPPLY



P18 Default Setting: 1-2 Short (SLVS mode)

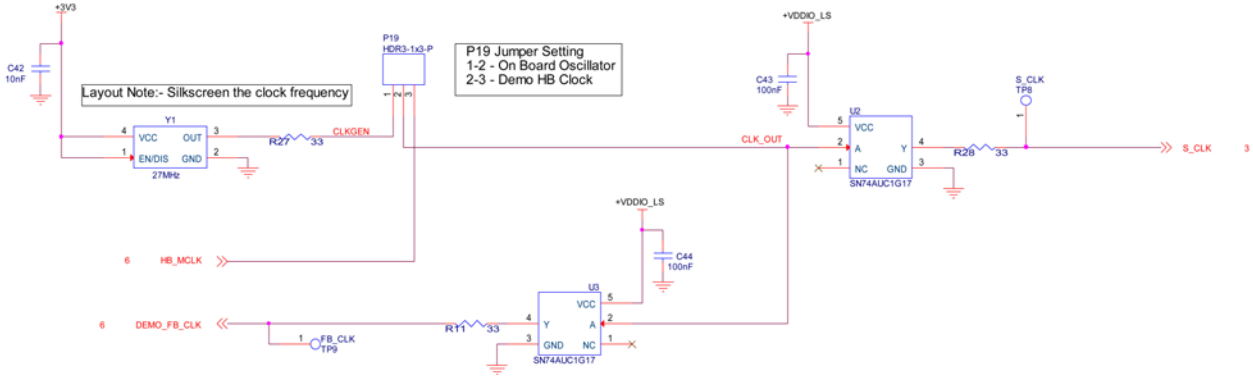
Fiducials

Ground Testpoints

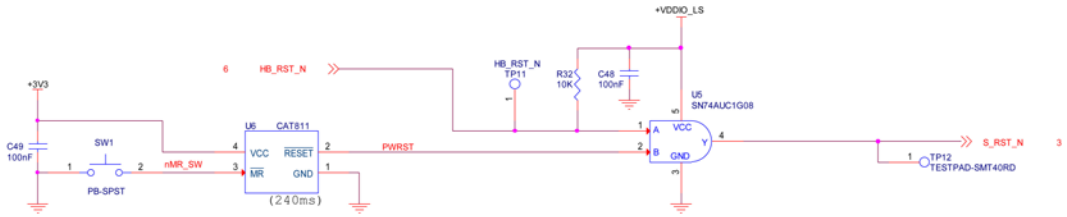
Mounting Holes

Clock and Reset

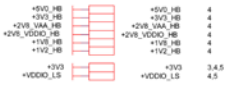
CLOCK CIRCUIT



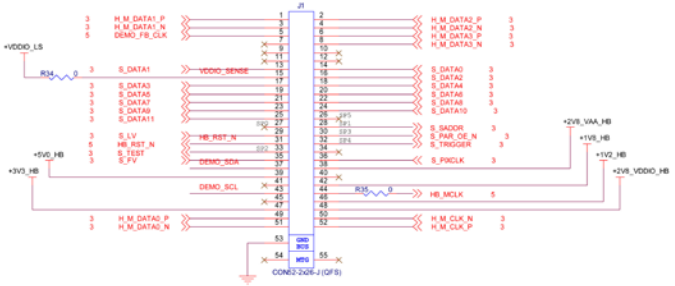
RESET CIRCUIT

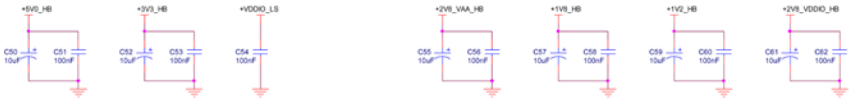


External Interface

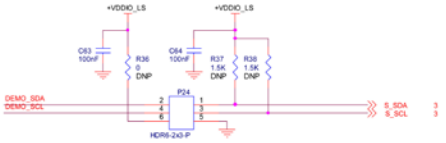


DEMO3 BASEBOARD I/F

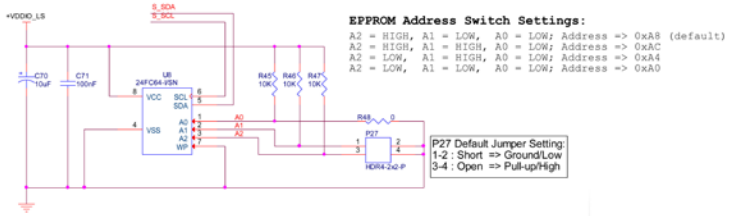




I2C DEBUG



LENS CORRECTION EEPROM



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