# **Darlington Complementary Silicon Power Transistors**

This series of plastic, medium-power silicon NPN and PNP Darlington transistors are designed for general purpose and low speed switching applications.

#### **Features**

- High DC Current Gain  $h_{FE} = 2500$  (typ) @  $I_C = 5.0$  Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:

V<sub>CEO(sus)</sub> = 80 Vdc (min) – BDW46 100 Vdc (min) – BDW42/BDW47

• Low Collector Emitter Saturation Voltage

 $V_{CE(sat)} = 2.0 \text{ Vdc (max)} @ I_C = 5.0 \text{ Adc}$ 3.0 Vdc (max) @  $I_C = 10.0 \text{ Adc}$ 

- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220 Compact Package
- These Devices are Pb-Free and are RoHS Compliant\*

#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BDW46 BDW42, BDW47	V <sub>CEO</sub>	80 100	Vdc
Collector-Base Voltage BDW46 BDW42, BDW47	V <sub>CB</sub>	80 100	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current	Ic	15	Adc
Base Current	I <sub>B</sub>	0.5	Adc
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	85 0.68	W W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL CHARACTERISTICS

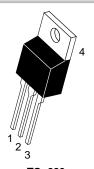
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.47	°C/W



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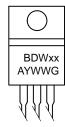
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# 15 AMP DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 80–100 VOLT, 85 WATT



TO-220 CASE 221A STYLE 1

## **MARKING DIAGRAM**



BDWxx = Device Code

x = 42, 46, or 47

A = Assembly Location

Y = Year WW = Work Week

= Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping
BDW42G	TO-220 (Pb-Free)	50 Units/Rail
BDW46G	TO-220 (Pb-Free)	50 Units/Rail
BDW47G	TO-220 (Pb-Free)	50 Units/Rail

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS			•		
Collector Emitter Sustaining Voltage (Note 1) $(I_C = 30 \text{ mAdc}, I_B = 0)$	BDW46 BDW42/BDW47	V <sub>CEO(sus)</sub>	80 100	_ _	Vdc
Collector Cutoff Current ( $V_{CE} = 40 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 50 \text{ Vdc}, I_B = 0$ )	BDW46 BDW42/BDW47	I <sub>CEO</sub>	- -	2.0 2.0	mAdc
Collector Cutoff Current $(V_{CB} = 80 \text{ Vdc}, I_E = 0)$ $(V_{CB} = 100 \text{ Vdc}, I_E = 0)$	BDW46 BDW42/BDW47	I <sub>CBO</sub>	- -	1.0 1.0	mAdc
Emitter Cutoff Current $(V_{BE} = 5.0 \text{ Vdc}, I_C = 0)$		I <sub>EBO</sub>	-	2.0	mAdc
ON CHARACTERISTICS (Note 1)					
DC Current Gain ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 4.0 \text{ Vdc}$ ) ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 4.0 \text{ Vdc}$ )		h <sub>FE</sub>	1000 250	_ _	
Collector–Emitter Saturation Voltage ( $I_C = 5.0$ Adc, $I_B = 10$ mAdc) ( $I_C = 10$ Adc, $I_B = 50$ mAdc)		V <sub>CE(sat)</sub>	- -	2.0 3.0	Vdc
Base–Emitter On Voltage (I <sub>C</sub> = 10 Adc, V <sub>CE</sub> = 4.0 Vdc)		V <sub>BE(on)</sub>	-	3.0	Vdc
SECOND BREAKDOWN (Note 2)			•	•	•
Second Breakdown Collector Current with Base Forward Biased BDW42	V <sub>CE</sub> = 28.4 Vdc	I <sub>S/b</sub>	3.0	_	Adc
BDW46/BDW47	$V_{CE} = 40 \text{ Vdc}$ $V_{CE} = 40 \text{ Vdc}$ $V_{CE} = 22.5 \text{ Vdc}$ $V_{CE} = 36 \text{ Vdc}$		1.2 3.8 1.2	- - -	
DYNAMIC CHARACTERISTICS					
Magnitude of common emitter small signal short circuit curre ( $I_C = 3.0 \text{ Adc}$ , $V_{CE} = 3.0 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	ent transfer ratio	f <sub>T</sub>	4.0	_	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 0.1 MHz)	BDW42 BDW46/BDW47	C <sub>ob</sub>	- -	200 300	pF
Small–Signal Current Gain ( $I_C = 3.0$ Adc, $V_{CE} = 3.0$ Vdc, $f = 1.0$ kHz)		h <sub>fe</sub>	300	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%.

<sup>2.</sup> Pulse Test non repetitive: Pulse Width = 250 ms.

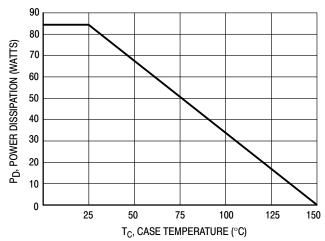


Figure 1. Power Temperature Derating Curve

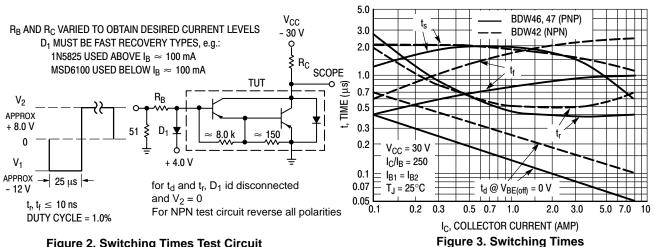


Figure 2. Switching Times Test Circuit

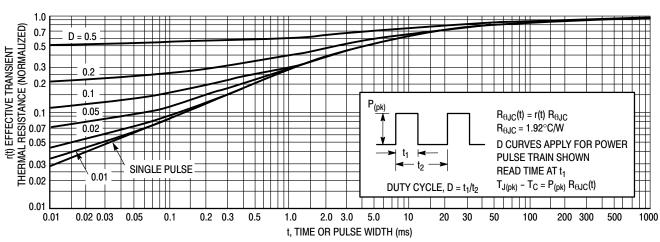
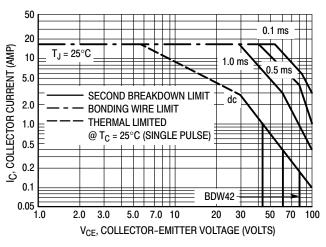


Figure 4. Thermal Response

#### **ACTIVE-REGION SAFE OPERATING AREA**



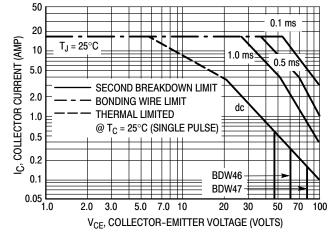


Figure 5. BDW42

Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 and 6 is based on  $T_{J(pk)} = 200$ °C;  $T_C$  is variable depending on conditions.

Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^{\circ} \text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. \*Linear extrapolation

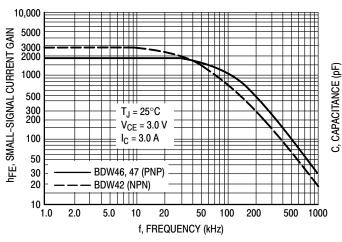


Figure 7. Small-Signal Current Gain

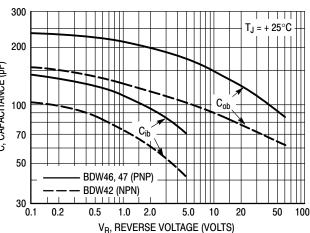


Figure 8. Capacitance

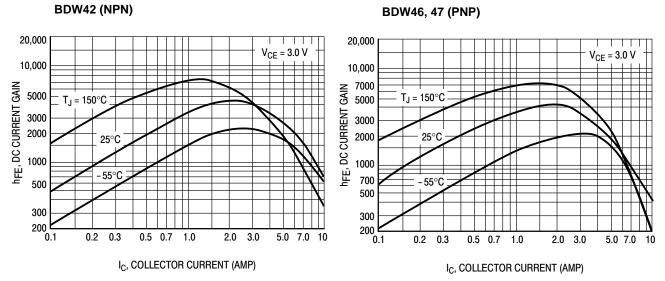


Figure 9. DC Current Gain

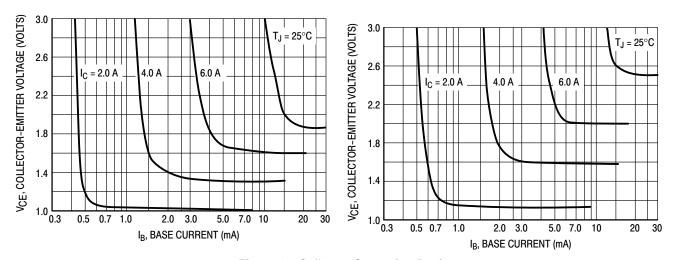


Figure 10. Collector Saturation Region

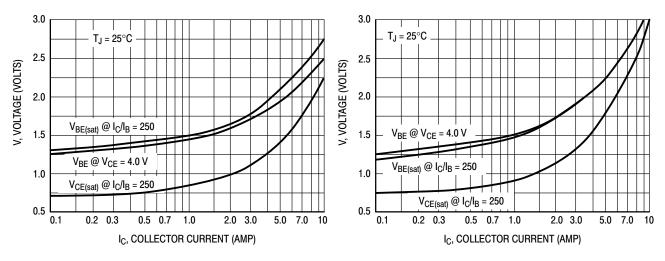


Figure 11. "On" Voltages

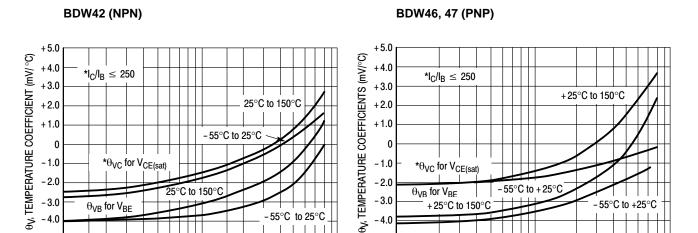


Figure 12. Temperature Coefficients

0.1

0.2

5.0

I<sub>C</sub>, COLLECTOR CURRENT (AMP)

10

2.0 3.0

5.0 7.0

-5.0

0.1

0.2 0.3

0.7

I<sub>C</sub>, COLLECTOR CURRENT (AMP)

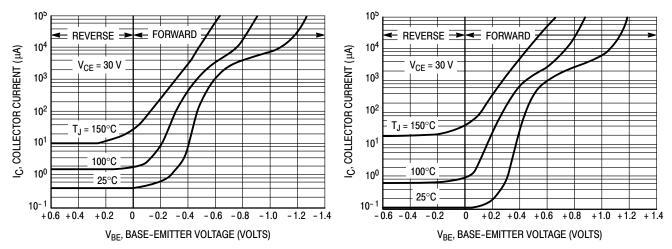


Figure 13. Collector Cut-Off Region

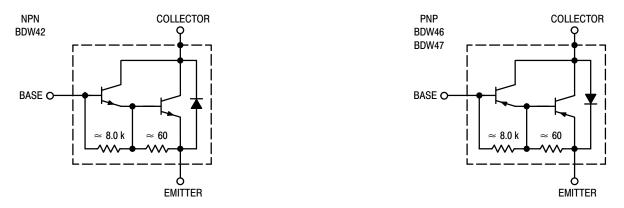
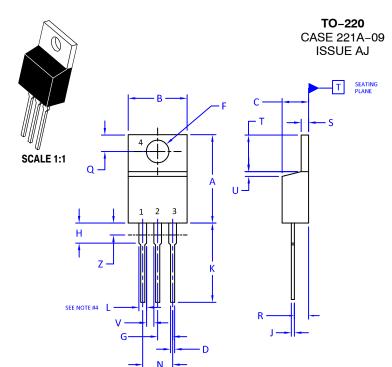


Figure 14. Darlington Schematic

# MECHANICAL CASE OUTLINE



DATE 05 NOV 2019

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: INCHES
- 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

#### 4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
Α	0.570	0.620	14.48	15.75
В	0.380	0.415	9.66	10.53
С	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
Н	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
К	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045		1.15	
Z		0.080		2.04

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	BASE	PIN 1.	BASE	PIN 1.	CATHODE	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	EMITTER	2.	ANODE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	COLLECTOR	3.	GATE	3.	GATE
4.	COLLECTOR	4.	EMITTER	4.	ANODE	4.	MAIN TERMINAL 2
STYLE 5:		STYLE 6:		STYLE 7:		STYLE 8:	
PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	CATHODE
2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE
3.	SOURCE	3.	ANODE	3.	CATHODE	3.	EXTERNAL TRIP/DELAY
4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE
STYLE 9:		STYLE 10:		STYLE 11	:	STYLE 12	:
PIN 1.	GATE	PIN 1.	GATE	PIN 1.	DRAIN	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	SOURCE	2.	SOURCE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	DRAIN	3.	GATE	3.	GATE
4.	COLLECTOR	4.	SOURCE	4.	SOURCE	4.	NOT CONNECTED

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