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## BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)

## Plastic Medium-Power Complementary Silicon Transistors

These devices are designed for general-purpose amplifier and low-speed switching applications.

## Features

- High DC Current Gain -

$$
\mathrm{h}_{\mathrm{FE}}=2500(\mathrm{Typ}) @ \mathrm{I}_{\mathrm{C}}=4.0 \mathrm{Adc}
$$

- Collector Emitter Sustaining Voltage - @ 100 mAdc

$$
\begin{aligned}
\mathrm{V}_{\mathrm{CEO}(\mathrm{sus})} & =80 \mathrm{Vdc}(\mathrm{Min})-\mathrm{BDX53B}, 54 \mathrm{~B} \\
& =100 \mathrm{Vdc}(\mathrm{Min})-\mathrm{BDX53C}, 54 \mathrm{C}
\end{aligned}
$$

- Low Collector-Emitter Saturation Voltage -

$$
\begin{aligned}
\mathrm{V}_{\mathrm{CE}(\mathrm{sat})} & =2.0 \mathrm{Vdc}(\operatorname{Max}) @ \mathrm{I}_{\mathrm{C}}=3.0 \mathrm{Adc} \\
& =4.0 \mathrm{Vdc}(\operatorname{Max}) @ \mathrm{I}_{\mathrm{C}}=5.0 \mathrm{Adc}
\end{aligned}
$$

- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- These Devices are $\mathrm{Pb}-$ Free and are RoHS Compliant*


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
| :---: | :---: | :---: | :---: |
| Collector-Emitter Voltage BDX53B, BDX54B BDX53C, BDX54C | $\mathrm{V}_{\text {CEO }}$ | $\begin{gathered} 80 \\ 100 \end{gathered}$ | Vdc |
| Collector-Base Voltage <br> BDX53B, BDX54B <br> BDX53C, BDX54C | $\mathrm{V}_{C B}$ | $\begin{gathered} 80 \\ 100 \end{gathered}$ | Vdc |
| Emitter-Base Voltage | $\mathrm{V}_{\mathrm{EB}}$ | 5.0 | Vdc |
| Collector Current- Continuous  <br>  - Peak | $I_{C}$ | $\begin{aligned} & 8.0 \\ & 12 \end{aligned}$ | Adc |
| Base Current | $\mathrm{I}_{\mathrm{B}}$ | 0.2 | Adc |
| Total Device Dissipation @ $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ Derate above $25^{\circ} \mathrm{C}$ | $\mathrm{P}_{\mathrm{D}}$ | $\begin{gathered} \hline 65 \\ 0.48 \end{gathered}$ | $\begin{gathered} \mathrm{W} \\ \mathrm{~W} /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Operating and Storage Junction Temperature Range | $\mathrm{T}_{\mathrm{J}}, \mathrm{T}_{\text {stg }}$ | -65 to +150 | ${ }^{\circ} \mathrm{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
| :--- | :---: | :---: | :---: |
| Thermal Resistance, Junction-to-Ambient | $\mathrm{R}_{\text {өJA }}$ | 70 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Thermal Resistance, Junction-to-Case | $\mathrm{R}_{\text {өJC }}$ | 1.92 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

*For additional information on our $\mathrm{Pb}-$ Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
80-100 VOLTS, 65 WATTS


TO-220
CASE 221A
STYLE 1

## MARKING DIAGRAM

 \& PIN ASSIGNMENT

| BDX5xy $=$ | Device Code |
| :--- | :--- |
|  | $x=3$ or 4 |$\quad$| $y=B$ or C |
| :--- |
|  |
|  |
| $=$ | | Assembly Location |
| :--- |
| Y $=$ |

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

## BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)



Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS ( $\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ unless otherwise noted)

| Characteristic |  | Symbol | Min | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OFF CHARACTERISTICS |  |  |  |  |  |
| $\begin{aligned} & \text { Collector-Emitter Sustaining Voltage (Note 1) } \\ & \quad\left(\mathrm{I}_{\mathrm{C}}=100 \mathrm{mAdc}, \mathrm{I}_{\mathrm{B}}=0\right) \end{aligned}$ | BDX53B, BDX54B <br> BDX53C, BDX54C | $\mathrm{V}_{\text {CEO(sus) }}$ | $\begin{gathered} 80 \\ 100 \end{gathered}$ | - | Vdc |
| Collector Cutoff Current $\begin{aligned} & \left(\mathrm{V}_{\mathrm{CE}}=40 \mathrm{Vdc}, \mathrm{I}_{\mathrm{B}}=0\right) \\ & \left(\mathrm{V}_{\mathrm{CE}}=50 \mathrm{Vdc}, \mathrm{I}_{\mathrm{B}}=0\right) \end{aligned}$ | BDX53B, BDX54B BDX53C, BDX54C | $I_{\text {cee }}$ | - | $\begin{aligned} & 0.5 \\ & 0.5 \end{aligned}$ | mAdc |
| Collector Cutoff Current $\begin{aligned} & \left(\mathrm{V}_{\mathrm{CB}}=80 \mathrm{Vdc}, \mathrm{I}_{\mathrm{E}}=0\right) \\ & \left(\mathrm{V}_{\mathrm{CB}}=100 \mathrm{Vdc}, \mathrm{I}_{\mathrm{E}}=0\right) \end{aligned}$ | $\begin{aligned} & \text { BDX53B, BDX54B } \\ & \text { BDX53C, BDX54C } \end{aligned}$ | $\mathrm{I}_{\text {cbo }}$ | - | $\begin{aligned} & 0.2 \\ & 0.2 \end{aligned}$ | mAdc |

ON CHARACTERISTICS (Note 1)

| DC Current Gain <br> $\left(I_{C}=3.0\right.$ Adc, $\left.V_{C E}=3.0 ~ V d c\right)$ | $\mathrm{h}_{\mathrm{FE}}$ | 750 | - | - |
| :--- | :---: | :---: | :---: | :---: |
| Collector-Emitter Saturation Voltage <br> $\left(\mathrm{I}_{\mathrm{C}}=3.0\right.$ Adc, $\left.\mathrm{I}_{\mathrm{B}}=12 \mathrm{mAdc}\right)$ | $\mathrm{V}_{\mathrm{CE} \text { (sat) }}$ | - | 2.0 | Vdc |
| Base-Emitter Saturation Voltage <br> $\left(\mathrm{I}_{\mathrm{C}}=3.0\right.$ Adc, $\left.\mathrm{I}_{\mathrm{C}}=12 \mathrm{~mA}\right)$ | $\mathrm{V}_{\mathrm{BE} \text { (sat) }}$ | - | 2.5 | Vdc |

DYNAMIC CHARACTERISTICS

| Small-Signal Current Gain $\left(\mathrm{I}_{\mathrm{C}}=3.0 \mathrm{Adc}, \mathrm{V}_{\mathrm{CE}}=4.0 \mathrm{Vdc}, \mathrm{f}=1.0 \mathrm{MHz}\right.$ ) |  | $\mathrm{hfe}_{\text {fe }}$ | 4.0 | - | - |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Output Capacitance $\left(\mathrm{V}_{\mathrm{CB}}=10 \mathrm{Vdc}, \mathrm{I}_{\mathrm{E}}=0, f=0.1 \mathrm{MHz}\right)$ | $\begin{aligned} & \text { BDX53B, 53C } \\ & \text { BDX54B, } 54 \mathrm{C} \end{aligned}$ | $\mathrm{C}_{\text {ob }}$ | - | $\begin{aligned} & 300 \\ & 200 \end{aligned}$ | pF |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width $\leq 300 \mu \mathrm{~s}$, Duty Cycle $\leq 2 \%$.

## BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)



Figure 2. Switching Time Test Circuit


Figure 3. Switching Times


Figure 4. Thermal Response


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_{C}-V_{C E}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $\mathrm{T}_{\mathrm{J}(\mathrm{pk})}=150^{\circ} \mathrm{C}$; $\mathrm{T}_{\mathrm{C}}$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to $10 \%$ provided $\mathrm{T}_{\mathrm{J}(\mathrm{pk})}<150^{\circ} \mathrm{C} . \mathrm{T}_{\mathrm{J}(\mathrm{pk})}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

## BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)



Figure 6. Small-Signal Current Gain

## NPN

BDX53B, 53C



Figure 7. Capacitance

PNP
BDX54B, 54C


Figure 8. DC Current Gain


Figure 9. Collector Saturation Region

## BDX53B, BDX53C (NPN), BDX54B, BDX54C (PNP)




Figure 10. "On" Voltages


Figure 11. Temperature Coefficients


Figure 12. Collector Cut-Off Region


Figure 13. Darlington Schematic

ORDERING INFORMATION

| Device | Package | Shipping $^{\dagger}$ |
| :--- | :---: | :---: |
| BDX53BG | TO-220 <br> (Pb-Free) | 50 Units / Rail |
| BDX53CG | TO-220 <br> (Pb-Free) | 50 Units / Rail |
| BDX54BG | TO-220 <br> (Pb-Free) | 50 Units / Rail |
| BDX54CG | TO-220 <br> (Pb-Free) | 50 Units / Rail |

$\dagger$ For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.


DATE 05 NOV 2019
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE $=1.35 \mathrm{MM}$

| DIM | INCHES |  | MILLIMETERS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | MIN. | MAX. | MIN. | MAX. |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.415 | 9.66 | 10.53 |
| C | 0.160 | 0.190 | 4.07 | 4.83 |
| D | 0.025 | 0.038 | 0.64 | 0.96 |
| F | 0.142 | 0.161 | 3.60 | 4.09 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.161 | 2.80 | 4.10 |
| J | 0.014 | 0.024 | 0.36 | 0.61 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.41 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | ---- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |


| STYLE 1: |  |
| ---: | :--- |
| PIN 1. | BASE |
| 2. | COLLECTOR |
| 3. | EMITTER |
| 4. | COLLECTOR |
|  |  |
| STYLE 5: |  |
| PIN 1. | GATE |
| 2. | DRAIN |
| 3. | SOURCE |
| 4. | DRAIN |
| STYLE 9: |  |
| PIN 1. | GATE |
| 2. | COLLECTOR |
| 3. | EMITTER |
| 4. | COLLECTOR |


| STYLE 2: |  |
| ---: | :--- |
| PIN 1. | BASE |
| 2. | EMITTER |
| 3. | COLLECTOR |
| 4. | EMITTER |
|  |  |
| STYLE 6: |  |
| PIN 1. | ANODE |
| 2. | CATHODE |
| 3. | ANODE |
| 4. | CATHODE |
| STYLE 10: |  |
| PIN 1. | GATE |
| 2. | SOURCE |
| 3. | DRAIN |
| 4. | SOURCE |


| STYLE 3: |  | STYLE 4: |  |
| ---: | :--- | ---: | :--- |
| PIN 1. | CATHODE | PIN 1. | MAIN TERMINAL 1 |
| 2. | ANODE | 2. | MAIN TERMINAL 2 |
| 3. | GATE | 3. | GATE |
| 4. | ANODE | 4. | MAIN TERMINAL 2 |
|  |  |  |  |
| STYLE 7: |  | STYLE 8: |  |
| PIN 1. | CATHODE | PIN 1. | CATHODE |
| 2. | ANODE | 2. | ANODE |
| 3. | CATHODE | 3. | EXTERNAL TRIP/DELAY |
| 4. | ANODE | 4. | ANODE |
|  |  |  |  |
| STYLE 11: | STYLE 12. |  |  |
| PIN 1. | DRAIN | PIN 1. MAIN TERMINAL 1 |  |
| 2. SOURCE | 2. MAIN TERMINAL 2 |  |  |
| 3. | GATE | 3. | GATE |
| 4. | SOURCE | 4. NOT CONNECTED |  |


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Scale 1:1

TO-220-3LD
CASE 340AT
ISSUE A

SUPPLIER "A" PACKAGE SHAPE

DATE 03 OCT 2017

NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:

SINGLE GAUGE $=0.51-0.61$
DUAL GAUGE $=1.10-1.45$
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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