# CAT24C32

# EEPROM Serial 32-Kb I²C

### Description

The CAT24C32 is a EEPROM Serial 32−Kb I²C devices, internally organized as 4096 words of 8 bits each.

It features a 32−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

External address pins make it possible to address up to eight CAT24C32 devices on the same bus.

### Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 32−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- PDIP, SOIC, TSSOP, UDFN, US 8−lead, WLCSP 4−ball and 5−ball Packages
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

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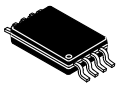
**SOIC−8**
**W SUFFIX**
**CASE 751BD**

**UDFN8**
**HU4 SUFFIX**
**CASE 517AZ**

**SOIC−8 WIDE**
**X SUFFIX**
**CASE 751BE**

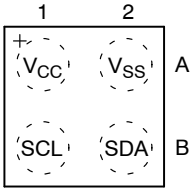


**TSSOP−8**
**Y SUFFIX**
**CASE 948AL**

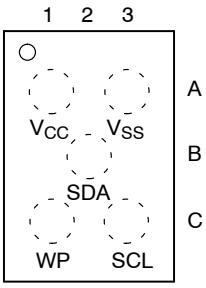
**WLCSP5**
**C5A SUFFIX**
**CASE 567JQ**

**WLCSP4**
**C4C SUFFIX**
**CASE 567JY**

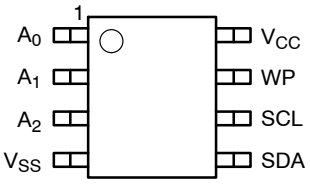
**PIN CONFIGURATIONS** (Top Views)




WLCSP4 (C4C)




WLCSP5 (C5A)




PDIP (L), SOIC (W), TSSOP (Y),
US (US), UDFN (HU4)

For the location of Pin 1, please consult the corresponding package drawing.

* In Development; please contact factory for availability

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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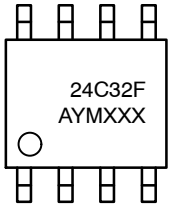
## DEVICE MARKINGS

(SOIC−8)




24C32F = Specific Device Code
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

(WLCSP−5)


2 = Specific Device Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)

(TSSOP−8)


C32F = Specific Device Code
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

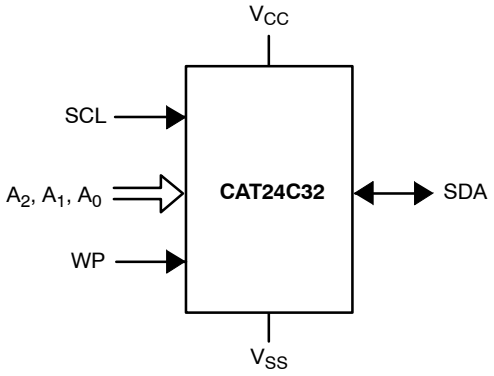
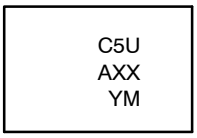



**Figure 1. Functional Symbol**

(WLCSP−4)


B = Specific Device Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)

(UDFN−8)




C5U = Specific Device Code
A = Assembly Location
XX = Last Two Digits of Assembly Lot Number
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)

## PIN FUNCTION

| Pin Name | Function |
|---|---|
| A0, A1, A2 | Device Address |
| SDA | Serial Data |
| SCL | Serial Clock |
| WP | Write Protect |
| $V_{CC}$ | Power Supply |
| $V_{SS}$ | Ground |

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameters | Ratings | Units |
|---|---|---|
| Storage Temperature | −65 to +150 | °C |
| Voltage on any Pin with Respect to Ground (Note 1) | −0.5 to +6.5 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than $V_{CC}$ + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than $V_{CC}$ + 1.5 V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

| Symbol | Parameter | Min | Units |
|---|---|---|---|
| $N_{END}$ (Note 3) | Endurance | 1,000,000 | Program/Erase Cycles |
| $T_{DR}$ | Data Retention | 100 | Years |

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, $V_{CC}$ = 5 V, 25°C.

**Table 3. D.C. OPERATING CHARACTERISTICS**

($V_{CC}$ = 1.8 V to 5.5 V, $T_A$ = −40°C to +125°C and $V_{CC}$ = 1.7 V to 5.5 V, $T_A$ = −40°C to +85°C, unless otherwise specified.)

| Symbol | Parameter | Test Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CCR}$ | Read Current | Read, $f_{SCL}$ = 400 kHz | | | 1 | mA |
| $I_{CCW}$ | Write Current | Write, $f_{SCL}$ = 400 kHz | | | 2 | mA |
| $I_{SB}$ | Standby Current | All I/O Pins at GND or $V_{CC}$ | $T_A$ = −40°C to +85°C<br>$V_{CC} \le 3.3$ V | | 1 | μA |
| | | | $T_A$ = −40°C to +85°C<br>$V_{CC}$ > 3.3 V | | 3 | |
| | | | $T_A$ = −40°C to +125°C | | 5 | |
| $I_L$ | I/O Pin Leakage | Pin at GND or $V_{CC}$ | | | 2 | μA |
| $V_{IL}$ | Input Low Voltage | | | −0.5 | $V_{CC}$ x 0.3 | V |
| $V_{IH}$ | Input High Voltage | SCL, SDA Inputs | | $V_{CC}$ x 0.7 | 6.5 | V |
| | | WP, A0, A1, A2 Inputs | | $V_{CC}$ x 0.7 | $V_{CC}$ + 0.5 | |
| $V_{OL1}$ | Output Low Voltage | $V_{CC} \ge 2.5$ V, $I_{OL}$ = 3.0 mA | | | 0.4 | V |
| $V_{OL2}$ | Output Low Voltage | $V_{CC}$ < 2.5 V, $I_{OL}$ = 1.0 mA | | | 0.2 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 4. PIN IMPEDANCE CHARACTERISTICS**

($V_{CC}$ = 1.8 V to 5.5 V, $T_A$ = −40°C to +125°C and $V_{CC}$ = 1.7 V to 5.5 V, $T_A$ = −40°C to +85°C, unless otherwise specified.)

| Symbol | Parameter | Conditions | Max | Units |
|---|---|---|---|---|
| $C_{IN}$ (Note 4) | SDA I/O Pin Capacitance | $V_{IN}$ = 0 V, $T_A$ = 25°C, f = 1.0 MHz | 8 | pF |
| $C_{IN}$ (Note 4) | Input Capacitance (other pins) | $V_{IN}$ = 0 V, $T_A$ = 25°C, f = 1.0 MHz | 6 | pF |
| $I_{WP}$ (Note 5) | WP Input Current | $V_{IN} < V_{IH}$, $V_{CC}$ = 5.5 V | 130 | μA |
| | | $V_{IN} < V_{IH}$, $V_{CC}$ = 3.3 V | 120 | |
| | | $V_{IN} < V_{IH}$, $V_{CC}$ = 1.7 V | 80 | |
| | | $V_{IN} > V_{IH}$ | 2 | |
| $I_A$ (Note 5) | Address Input Current (A0, A1, A2) Product Rev F | $V_{IN} < V_{IH}$, $V_{CC}$ = 5.5 V | 50 | μA |
| | | $V_{IN} < V_{IH}$, $V_{CC}$ = 3.3 V | 35 | |
| | | $V_{IN} < V_{IH}$, $V_{CC}$ = 1.7 V | 25 | |
| | | $V_{IN} > V_{IH}$ | 2 | |

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x $V_{CC}$), the strong pull−down reverts to a weak current source.

**Table 5. A.C. CHARACTERISTICS**
($V_{CC}$ = 1.8 V to 5.5 V, $T_A$ = −40°C to +125°C and $V_{CC}$ = 1.7 V to 5.5 V, $T_A$ = −40°C to +85°C.) (Note 6)

| Symbol | Parameter | Standard $V_{CC}$ = 1.7 V – 5.5 V | | Fast $V_{CC}$ = 1.7 V – 5.5 V | | Fast–Plus (Note 9) $V_{CC}$ = 2.5 V – 5.5 V $T_A$ = –40°C to +85°C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $F_{SCL}$ | Clock Frequency | | 100 | | 400 | | 1,000 | kHz |
| $t_{HD:STA}$ | START Condition Hold Time | 4 | | 0.6 | | 0.25 | | μs |
| $t_{LOW}$ | Low Period of SCL Clock | 4.7 | | 1.3 | | 0.45 | | μs |
| $t_{HIGH}$ | High Period of SCL Clock | 4 | | 0.6 | | 0.40 | | μs |
| $t_{SU:STA}$ | START Condition Setup Time | 4.7 | | 0.6 | | 0.25 | | μs |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | 0 | | 0 | | μs |
| $t_{SU:DAT}$ | Data In Setup Time | 250 | | 100 | | 50 | | ns |
| $t_R$ (Note 7) | SDA and SCL Rise Time | | 1,000 | | 300 | | 100 | ns |
| $t_F$ (Note 7) | SDA and SCL Fall Time | | 300 | | 300 | | 100 | ns |
| $t_{SU:STO}$ | STOP Condition Setup Time | 4 | | 0.6 | | 0.25 | | μs |
| $t_{BUF}$ | Bus Free Time Between STOP and START | 4.7 | | 1.3 | | 0.5 | | μs |
| $t_{AA}$ | SCL Low to Data Out Valid | | 3.5 | | 0.9 | | 0.40 | μs |
| $t_{DH}$ (Note 7) | Data Out Hold Time | 100 | | 100 | | 50 | | ns |
| $T_i$ (Note 7) | Noise Pulse Filtered at SCL and SDA Inputs | | 100 | | 100 | | 100 | ns |
| $t_{SU:WP}$ | WP Setup Time | 0 | | 0 | | 0 | | μs |
| $t_{HD:WP}$ | WP Hold Time | 2.5 | | 2.5 | | 1 | | μs |
| $t_{WR}$ | Write Cycle Time | | 5 | | 5 | | 5 | ms |
| $t_{PU}$ (Notes 7, 8) | Power−up to Ready Mode | | 1 | | 1 | | 1 | ms |

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. $t_{PU}$ is the delay between the time $V_{CC}$ is stable and the device is ready to accept commands.
9. Fast−Plus (1 MHz) speed class available for product revision “F”. The die revision “F” is identified by letter “F” or a dedicated marking code on top of the package.

**Table 6. A.C. TEST CONDITIONS**

| | |
|---|---|
| Input Drive Levels | 0.2 x $V_{CC}$ to 0.8 x $V_{CC}$ |
| Input Rise and Fall Time | ≤ 50 ns |
| Input Reference Levels | 0.3 x $V_{CC}$, 0.7 x $V_{CC}$ |
| Output Reference Level | 0.5 x $V_{CC}$ |
| Output Test Load | Current Source $I_{OL}$ = 3 mA ($V_{CC}$ ≥ 2.5 V); $I_{OL}$ = 1 mA ($V_{CC}$ < 2.5 V); $C_L$ = 100 pF |

### Power−On Reset (POR)

Each CAT24C32 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after $V_{CC}$ exceeds the POR trigger level and will power down into Reset mode when $V_{CC}$ drops below the POR trigger level. This bi−directional POR behavior protects the device against ‘brown−out’ failure following a temporary loss of power.

### Pin Description

**SCL:** The Serial Clock input pin accepts the clock signal generated by the Master.

**SDA:** The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

**$A_0$, $A_1$ and $A_2$:** The Address inputs set the device address that must be matched by the corresponding Slave address bits. The Address inputs are hard−wired HIGH or LOW allowing for up to eight devices to be used (cascaded) on the same bus. When left floating, these pins are pulled LOW internally. The Address inputs are not available for use with WLCSP 4−ball and 5−ball.

**WP:** When pulled HIGH, the Write Protect input pin inhibits all write operations. When left floating, this pin is pulled LOW internally. The WP input is not available for the WLCSP 4−ball, therefore all write operations are allowed for the device in this package.

### Functional Description

The CAT24C32 supports the Inter−Integrated Circuit ($I^2C$) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic, and Slave devices which execute requests. The CAT24C32 operates as a Slave device. Both Master and Slave can transmit or receive, but only the Master can assign those roles.

### $I^2C$ Bus Protocol

The 2−wire $I^2C$ bus consists of two lines, SCL and SDA, connected to the $V_{CC}$ supply via pull−up resistors. The Master provides the clock to the SCL line, and either the Master or the Slaves drive the SDA line. A ‘0’ is transmitted by pulling a line LOW and a ‘1’ by letting it stay HIGH. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

### START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 2). The START consists of a HIGH to LOW SDA transition, while SCL is HIGH. Absent the START, a Slave will not respond to the Master. The STOP completes all commands, and consists of a LOW to HIGH SDA transition, while SCL is HIGH.

### Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8−bit Slave address. For the CAT24C32, the first four bits of the Slave address are set to 1010 (Ah); the next three bits, $A_2$, $A_1$ and $A_0$, must match the logic state of the similarly named input pins. The devices in WLCSP (C5A and C4C) respond only to the Slave Address with $A_2$ $A_1$ $A_0$ = 0 0 0. The R/W bit tells the Slave whether the Master intends to read (1) or write (0) data (Figure 3).

### Acknowledge

During the 9$^{th}$ clock cycle following every byte sent to the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 4). Bus timing is illustrated in Figure 5.

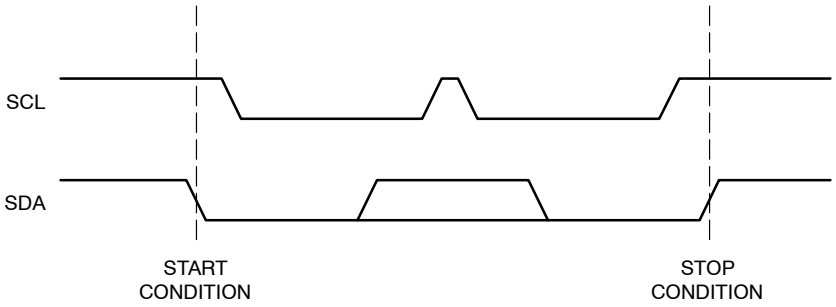
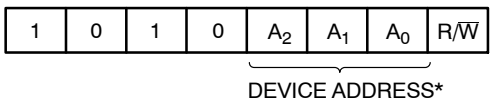



**Figure 2. Start/Stop Timing**




* The devices in WLCSP 4−ball and 5−ball respond only to Slave Address byte with $A_2$ $A_1$ $A_0$ = 0 0 0

**Figure 3. Slave Address Bits**

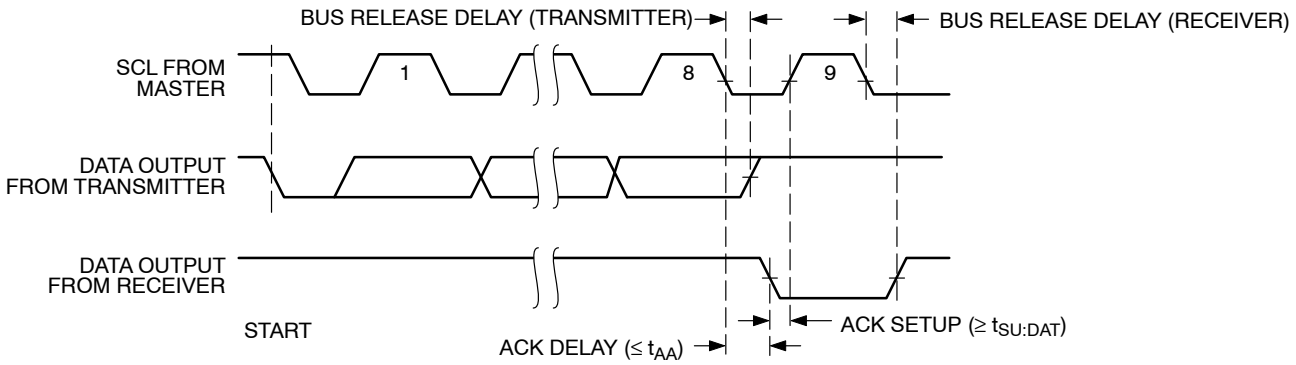



**Figure 4. Acknowledge Timing**

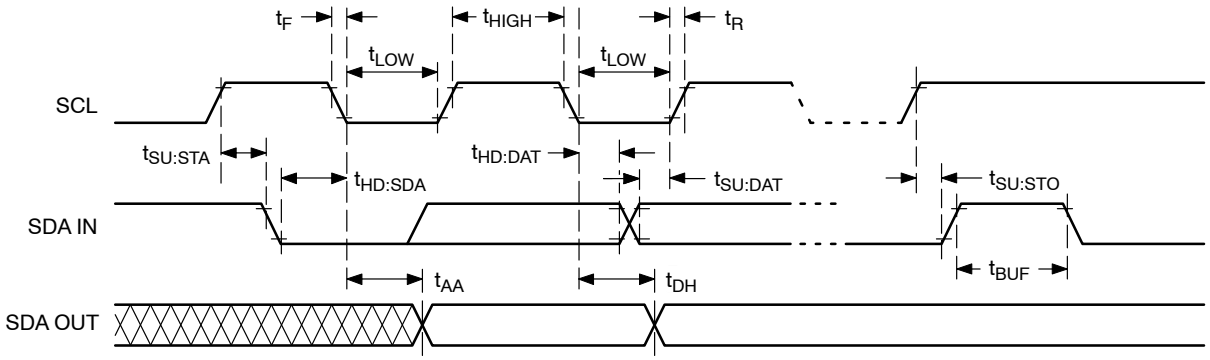



**Figure 5. Bus Timing**

## WRITE OPERATIONS

### Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0'. The Master then sends two address bytes and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 6). The STOP starts the internal Write cycle, and while this operation is in progress ($t_{WR}$), the SDA output is tri−stated and the Slave does not acknowledge the Master (Figure 7).

### Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 8). Up to 32 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle ($t_{WR}$).

### Acknowledge Polling

As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow−up with a new Read or Write request, rather than wait for the maximum specified Write time ($t_{WR}$) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

### Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the Write operation. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the 1$^{st}$ data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the Slave will not acknowledge the data byte and the Write request will be rejected.

### Delivery State

The CAT24C32 is shipped erased, i.e., all bytes are FFh.

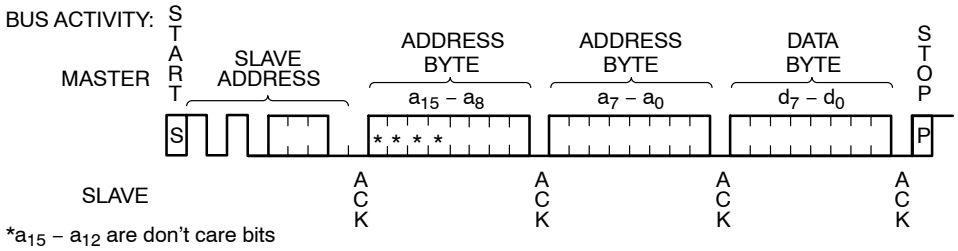



**Figure 6. Byte Write Sequence**

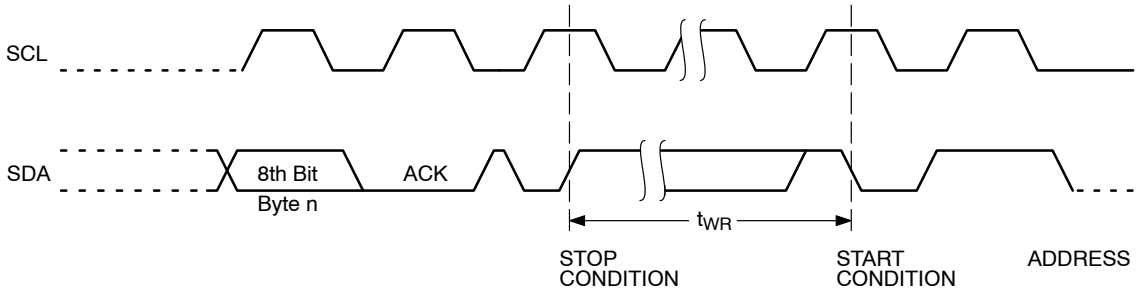



**Figure 7. Write Cycle Timing**

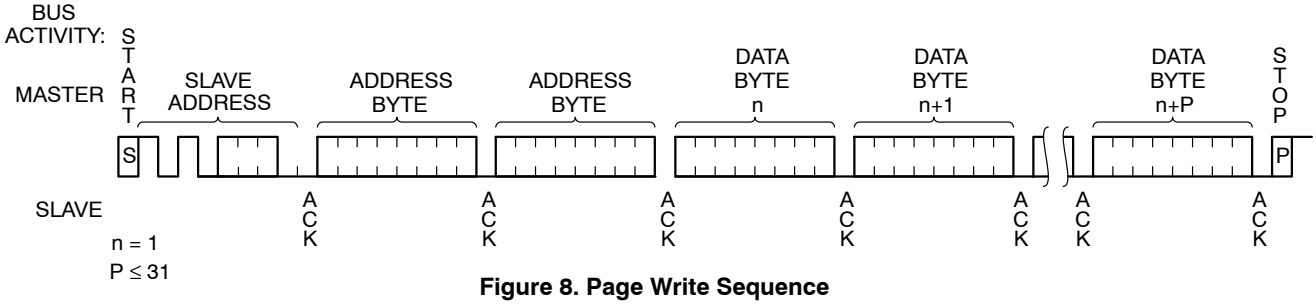



**Figure 8. Page Write Sequence**

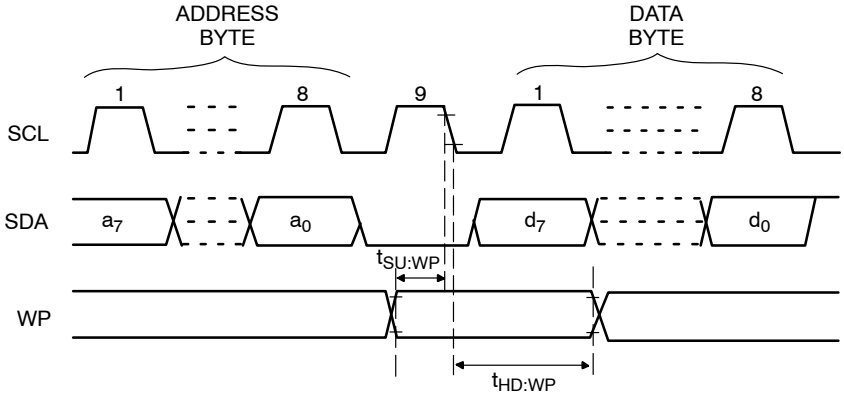



**Figure 9. WP Timing**

## READ OPERATIONS

### Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 10). The Slave then returns to Standby mode.

### Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0' and then sends two address bytes to the Slave. Rather than completing the Byte Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 11).

### Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 12). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory.

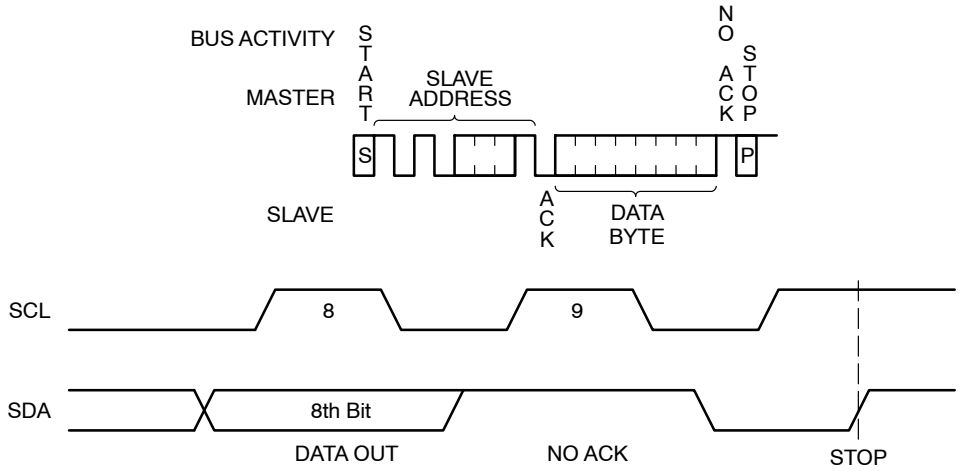



**Figure 10. Immediate Read Sequence and Timing**

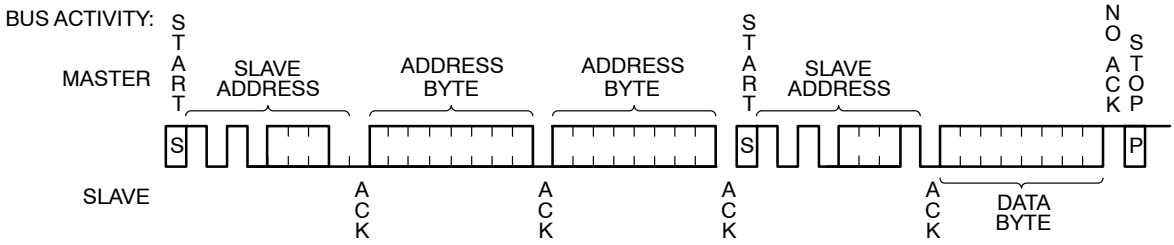



**Figure 11. Selective Read Sequence**

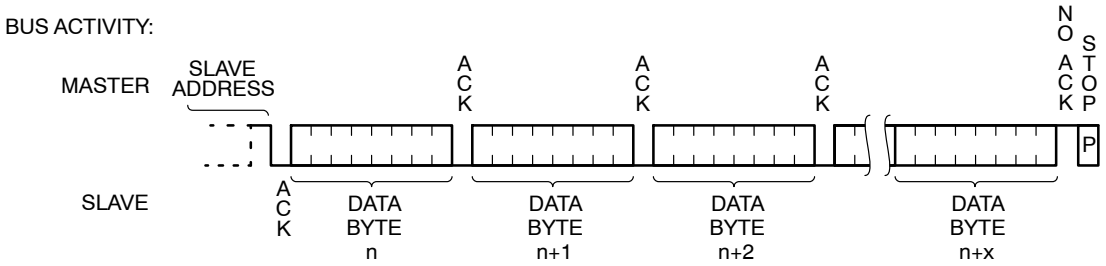



**Figure 12. Sequential Read Sequence**

## ORDERING INFORMATION

| Device Order Number | Specific Device Marking | Package Type | Temperature Range | Lead Finish | Shipping† |
|---|---|---|---|---|---|
| CAT24C32HU4I−GT3 | C5U | UDFN8 | I = Industrial (−40°C to +85°C) | NiPdAu | Tape & Reel, 3,000 Units / Reel |
| CAT24C32C5ATR | 2 | WLCSP5 | I = Industrial (−40°C to +85°C) | SnAgCu | Tape & Reel, 5,000 Units / Reel |
| CAT24C32C5CTR | P | WLCSP5 with Die Coat | I = Industrial (−40°C to +85°C) | SnAgCu | Tape & Reel, 5,000 Units / Reel |
| CAT24C32C4CTR | B | WLCSP4 with Die Coat | I = Industrial (−40°C to +85°C) | SnAg | Tape & Reel, 5,000 Units / Reel |
| CAT24C32XI−T2 (Note 14) | TBD | SOIC−8 | I = Industrial (−40°C to +85°C) | Matte−Tin | Tape & Reel, 2,000 Units / Reel |
| CAT24C32WI−GT3 | 24C32F | SOIC−8, JEDEC | I = Industrial (−40°C to +85°C) | NiPdAu | Tape & Reel, 3,000 Units / Reel |
| CAT24C32YI−GT3 | C32F | TSSOP−8 | I = Industrial (−40°C to +85°C) | NiPdAu | Tape & Reel, 3,000 Units / Reel |
| CAT24C32USI−T3 (In Development) | TBD | US8 | I = Industrial (−40°C to +85°C) | Matte−Tin | Tape & Reel, 3,000 Units / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. All packages are RoHS−compliant (Lead−free, Halogen−free).
11. The standard lead finish is NiPdAu.
12. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
13. **Caution: The EEPROM devices delivered in WLCSP must never be exposed to ultraviolet light. When exposed to ultraviolet light the EEPROM cells lose their stored data.**
14. In development.

ON Semiconductor is licensed by the Philips Corporation to carry the $I^2C$ bus protocol.

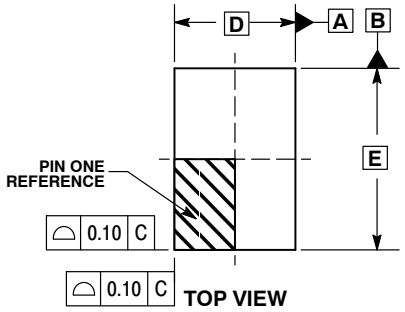
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

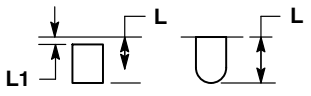
ON Semiconductor®

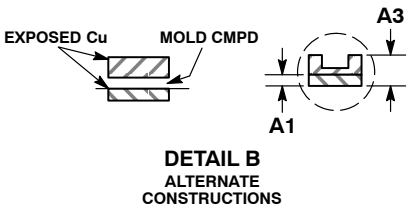
**SCALE 2:1**

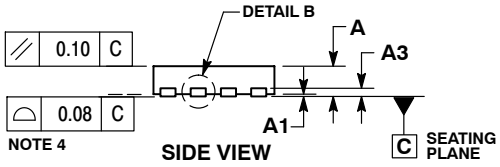
**UDFN8, 2x3 EXTENDED PAD**
CASE 517AZ
ISSUE A

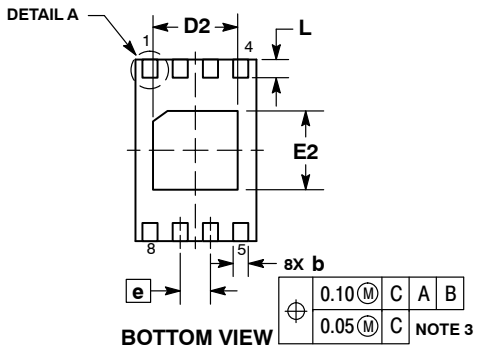
DATE 23 MAR 2015



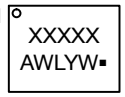




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.35 | 1.45 |
| E | 3.00 BSC | |
| E2 | 1.25 | 1.35 |
| e | 0.50 BSC | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.15 |

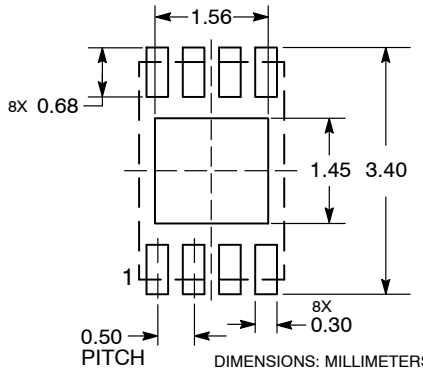
### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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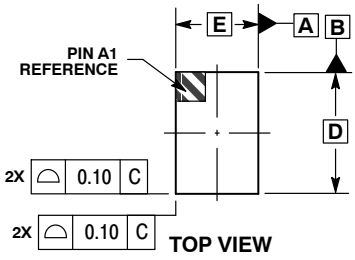
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

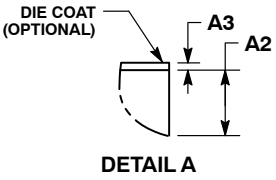
ON Semiconductor®

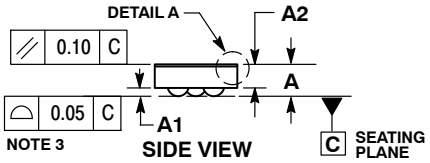
**WLCSP5, 1.34x0.91**
CASE 567JQ
ISSUE A

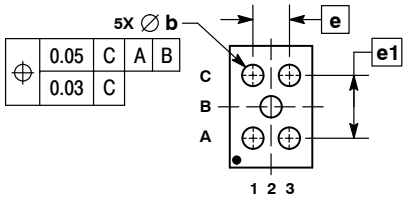
DATE 09 JUN 2015

**SCALE 4:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.

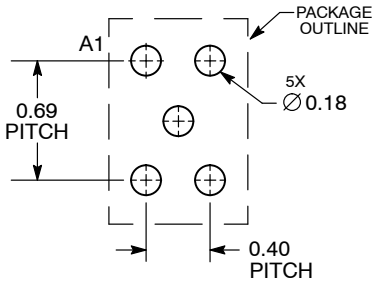
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | --- | 0.35 |
| A1 | 0.08 | 0.12 |
| A2 | 0.23 REF | |
| A3 | 0.025 REF | |
| b | 0.16 | 0.20 |
| D | 1.34 BSC | |
| E | 0.91 BSC | |
| e | 0.40 BSC | |
| e1 | 0.693 BSC | |

### GENERIC MARKING DIAGRAM*


X = Specific Device Code
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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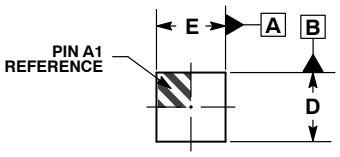
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

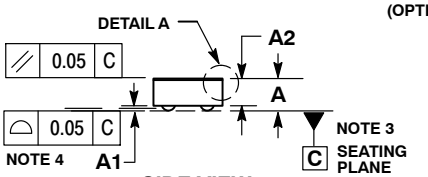
**WLCSP4, 0.77x0.77**
CASE 567JY
ISSUE C

**SCALE 4:1**

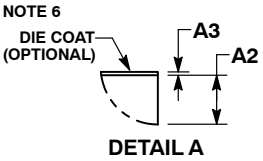
DATE 07 MAR 2017



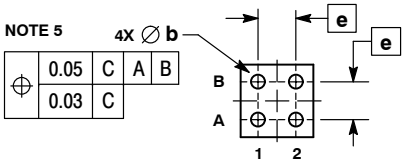

**TOP VIEW**




**SIDE VIEW**




**DETAIL A**




**BOTTOM VIEW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.
6. BACKSIDE COATING IS OPTIONAL.

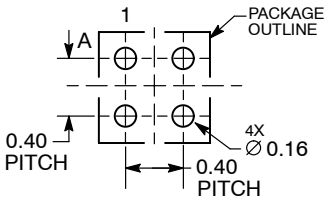
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | --- | --- | 0.35 |
| A1 | 0.04 | 0.06 | 0.08 |
| A2 | | 0.23 REF | |
| A3 | | 0.025 REF | |
| b | 0.15 | 0.155 | 0.16 |
| D | 0.75 | 0.77 | 0.79 |
| E | 0.75 | 0.77 | 0.79 |
| e | | 0.40 BSC | |

### GENERIC MARKING DIAGRAM*


X = Specific Device Code
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| **DESCRIPTION:** | **WLCSP4, 0.77X0.77** | **PAGE 1 OF 1** |

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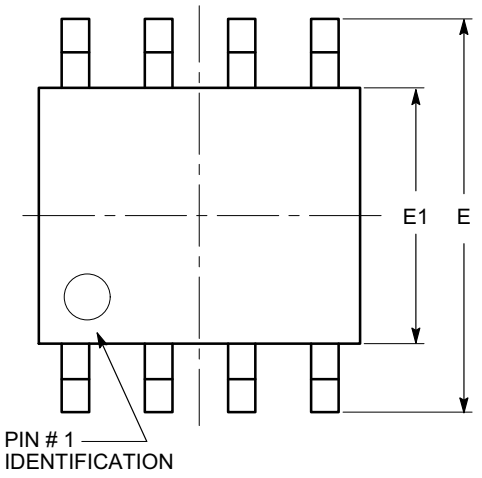
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

ON Semiconductor®

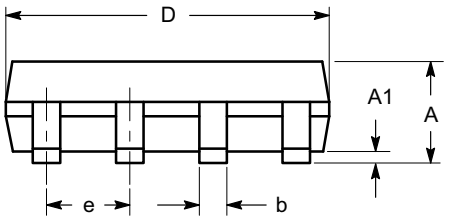
**SOIC 8, 150 mils**
CASE 751BD–01
ISSUE O

DATE 19 DEC 2008

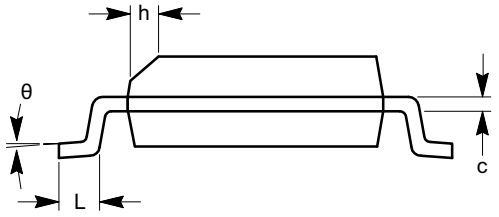



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |




**SIDE VIEW**




**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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| DESCRIPTION: | SOIC 8, 150 MILS | PAGE 1 OF 1 |

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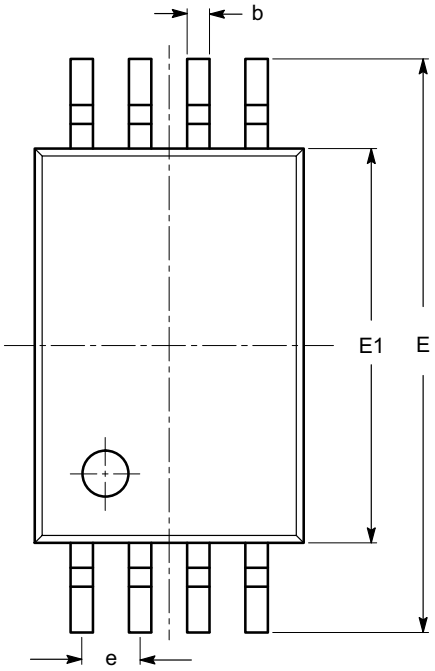
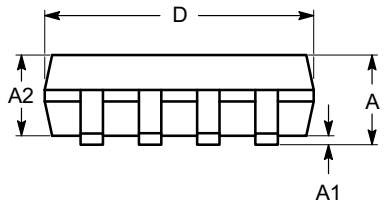
**TSSOP8, 4.4x3**
CASE 948AL−01
ISSUE O

DATE 19 DEC 2008

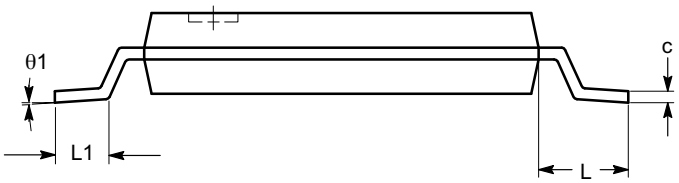



**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 0.90 | 1.05 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| D | 2.90 | 3.00 | 3.10 |
| E | 6.30 | 6.40 | 6.50 |
| E1 | 4.30 | 4.40 | 4.50 |
| e | 0.65 BSC | | |
| L | 1.00 REF | | |
| L1 | 0.50 | 0.60 | 0.75 |
| θ | 0º | | 8º |




**SIDE VIEW**




**END VIEW**

**Notes:**
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| **DESCRIPTION:** | **TSSOP8, 4.4X3** | **PAGE 1 OF 1** |

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