ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and onsemi and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

CAT93C76B

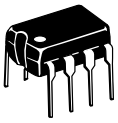
EEPROM Serial 8-Kb Microwire

ON Semiconductor®

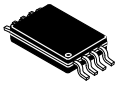
www.onsemi.com

SOIC−8
V SUFFIX
CASE 751BD

UDFN−8
HU4 SUFFIX
CASE 517AZ



PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8
Y SUFFIX
CASE 948AL

MSOP−8
Z SUFFIX
CASE 846AD

Description

The CAT93C76B is an 8−Kb Microwire Serial EEPROM memory device which is configured as either registers of 16 bits (ORG pin at V_{CC} or Not Connected) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C76B is manufactured using ON Semiconductor's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8−pin PDIP, SOIC, TSSOP, MSOP and 8−pad UDFN packages.

Features

- High Speed Operation: 4 MHz (5 V), 2 MHz (1.8 V)
- 1.8 V (1.65 V*) to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self−timed Write Cycle with Auto−clear
- Software Write Protection
- Power−up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Ranges
- Sequential Read
- 8−pin PDIP, SOIC, TSSOP, MSOP and 8−Pad UDFN Packages
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant†

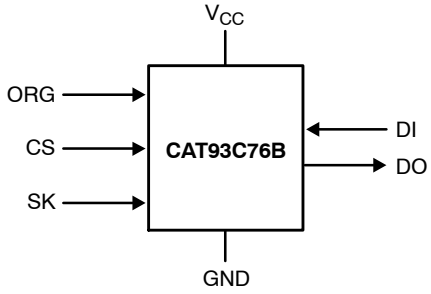


Figure 1. Functional Symbol

***CAT93C76Bxx−xxL (T_A = −20°C to +85°C)**

†For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN CONFIGURATION

PDIP (L), SOIC (V),
TSSOP (Y), UDFN (HU4), MSOP (Z)
(Top View)

PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

NOTE: When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pull−up device will select the x16 organization.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

© Semiconductor Components Industries, LLC, 2013

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−2.0 to +V_{CC} +2.0	V
V_{CC} with Respect to Ground	−2.0 to +7.0	V
Lead Soldering Temperature (10 seconds)	300	°C
Output Short Circuit Current (Note 2)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Reference Test Method	Min	Units
N_{END} (Note 3)	Endurance	MIL−STD−883, Test Method 1033	1,000,000	Cycles / Byte
T_{DR} (Note 3)	Data Retention	MIL−STD−883, Test Method 1008	100	Years
V_{ZAP} (Note 3)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2,000	V
I_{LTH} (Notes 3, 4)	Latch−Up	JEDEC Standard 17	100	mA

3. These parameters are tested initially and after a design or process change that affects the parameter.
4. Latch−up protection is provided for stresses up to 100 mA on I/O pins from −1 V to V_{CC} + 1 V.

Table 3. D.C. OPERATING CHARACTERISTICS

(V_{CC} = +1.8 V to +5.5 V, T_A = −40°C to +125°C, V_{CC} = +1.65 V to +5.5 V, T_A = −20°C to +85°C unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CC1}	Supply Current (Write)	Write, V_{CC} = 5.0 V			2	mA
I_{CC2}	Supply Current (Read)	Read, DO open, f_{SK} = 2 MHz, V_{CC} = 5.0 V			500	μA
I_{SB1}	Standby Current (x8 Mode)	V_{IN} = GND or V_{CC} CS = GND, ORG = GND	T_A = −40°C to +85°C		2	μA
			T_A = −40°C to +125°C		5	
I_{SB2}	Standby Current (x16 Mode)	V_{IN} = GND or V_{CC} CS = GND, ORG = Float or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		3	
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC} CS = GND	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} < 5.5 V		−0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V ≤ V_{CC} < 5.5 V		2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.65 V ≤ V_{CC} < 4.5 V		0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.65 V ≤ V_{CC} < 4.5 V		V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OL} = 3 mA			0.4	V
V_{OH1}	Output High Voltage	4.5 V ≤ V_{CC} < 5.5 V, I_{OH} = −400 μA		2.4		V
V_{OL2}	Output Low Voltage	1.65 V ≤ V_{CC} < 4.5 V, I_{OL} = 1 mA			0.2	V
V_{OH2}	Output High Voltage	1.65 V ≤ V_{CC} < 4.5 V, I_{OH} = −100 μA		V_{CC} − 0.2		V

Table 4. PIN CAPACITANCE (Note 3)

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT}	Output Capacitance (DO)	V_{OUT} = 0 V			5	pF
C_{IN}	Input Capacitance (CS, SK, DI, ORG)	V_{IN} = 0 V			5	pF

Table 5. INSTRUCTION SET (Note 5)

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10–A0	A9–A0			Read Address AN– A0
ERASE	1	11	A10–A0	A9–A0			Clear Address AN– A0
WRITE	1	01	A10–A0	A9–A0	D7–D0	D15–D0	Write Address AN– A0
EWEN	1	00	11XXXXXXXXX	11XXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXX	00XXXXXXXX			Write Disable
ERAL*	1	00	10XXXXXXXXX	10XXXXXXXX			Clear All Addresses
WRAL*	1	00	01XXXXXXXXX	01XXXXXXXX	D7–D0	D15–D0	Write All Addresses

* Not available at V_{CC} < 1.8 V

5. Address bit A10 for the 1,024x8 org. and A9 for the 512x16 org. are “don’t care” bits, but must be kept at either a “1” or “0” for READ, WRITE and ERASE commands.

Table 6. A.C. CHARACTERISTICS

(V_{CC} = +1.8 V to +5.5 V, T_A = −40°C to +125°C, V_{CC} = +1.65 V to +5.5 V, T_A = −20°C to +85°C unless otherwise specified.)

Symbol	Parameter	V_{CC} < 4.5 V		V_{CC} > 4.5 V		Units
		Min	Max	Min	Max	
t_{CSS}	CS Setup Time	50		50		ns
t_{CSH}	CS Hold Time	0		0		ns
t_{DIS}	DI Setup Time	100		50		ns
t_{DIH}	DI Hold Time	100		50		ns
t_{PD1}	Output Delay to 1		0.25		0.1	μs
t_{PD0}	Output Delay to 0		0.25		0.1	μs
t_{HZ} (Note 6)	Output Delay to High−Z		100		100	ns
t_{EW}	Program/Erase Pulse Width		5		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		0.1		μs
t_{SKHI}	Minimum SK High Time	0.25		0.1		μs
t_{SKLOW}	Minimum SK Low Time	0.25		0.1		μs
t_{SV}	Output Delay to Status Valid		0.25		0.1	μs
SK_{MAX}	Maximum Clock Frequency	DC	2000	DC	4000	kHz

6. This parameter is tested initially and after a design or process change that affects the parameter.

Table 7. POWER−UP TIMING (Notes 6, 7)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 8. A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Voltages	0.2 V_{CC} to 0.7 V_{CC}	1.65 V ≤ V_{CC} ≤ 4.5 V
Timing Reference Voltages	0.5 V_{CC}	1.65 V ≤ V_{CC} ≤ 4.5 V
Output Load	Current Source I_{OLmax}/I_{OHmax}; CL = 100 pF	

Device Operation

The CAT93C76B is a 8192−bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C76B can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 13−bit instructions control the read, write and erase operations of the device. When organized as X8, seven 14−bit instructions control the read, write and erase operations of the device. The CAT93C76B operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical “1” start bit, a 2−bit (or 4−bit) opcode, 10−bit address (an additional bit when organized X8) and for write operations a 16−bit data field (8−bit for X8 organizations). The most significant bit of the address is “don’t care” but it must be present.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C76B will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

For the CAT93C76B, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. Since this device features Auto−Clear before write, it is NOT necessary to erase a memory location before it is written into.

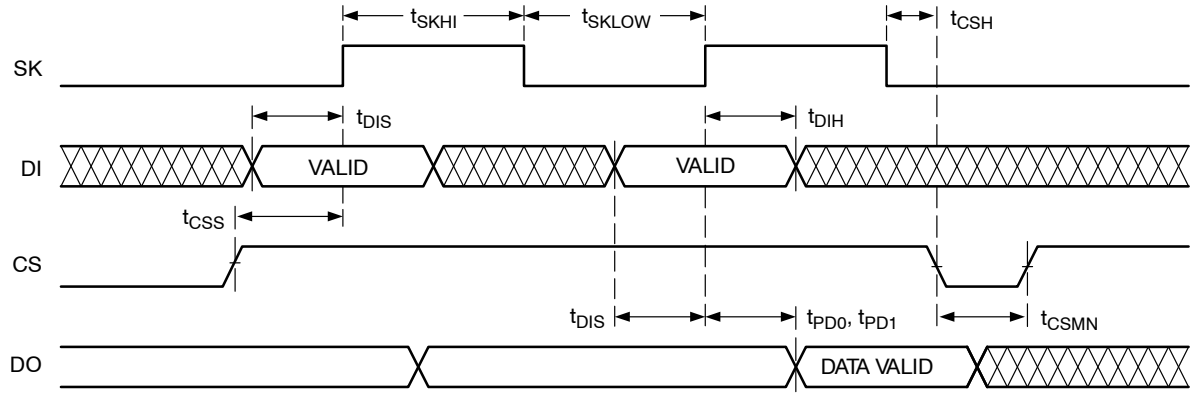


Figure 2. Synchronous Data Timing

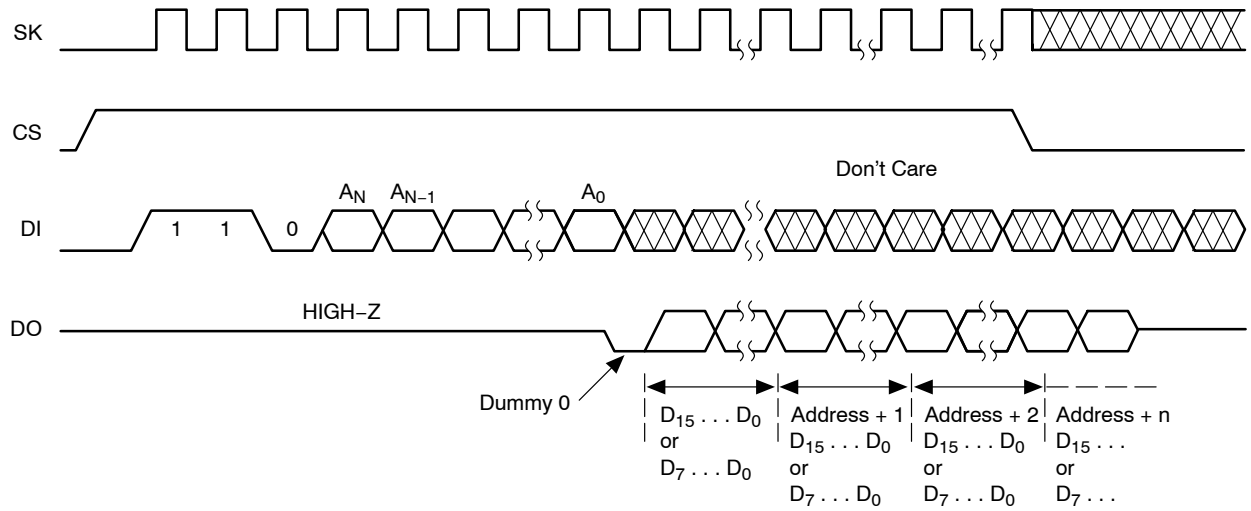


Figure 3. READ Instruction Timing

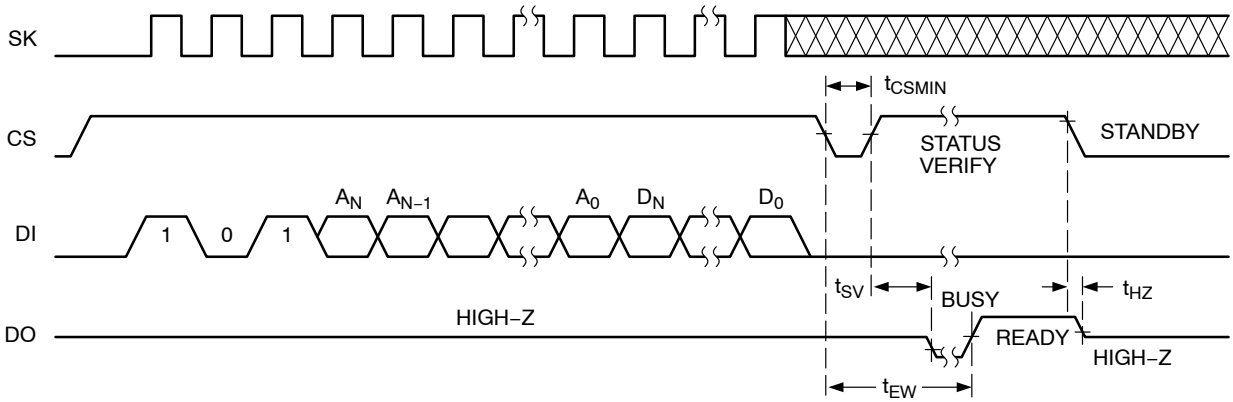


Figure 4. WRITE Instruction Timing

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The CAT93C76B powers up in the write disable state. Any writing after power−up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C76B write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Note 1: *After the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock (SK) in order to start the self−timed high voltage cycle. This is important because if CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.*

Power−On Reset (POR)

The CAT93C76B incorporates Power−On Reset (POR) circuitry which protects the device against malfunctioning while V_{CC} is lower than the recommended operating voltage.

The device will power up into a read−only state and will power−down into a reset state when V_{CC} crosses the POR level of ~1.3 V.

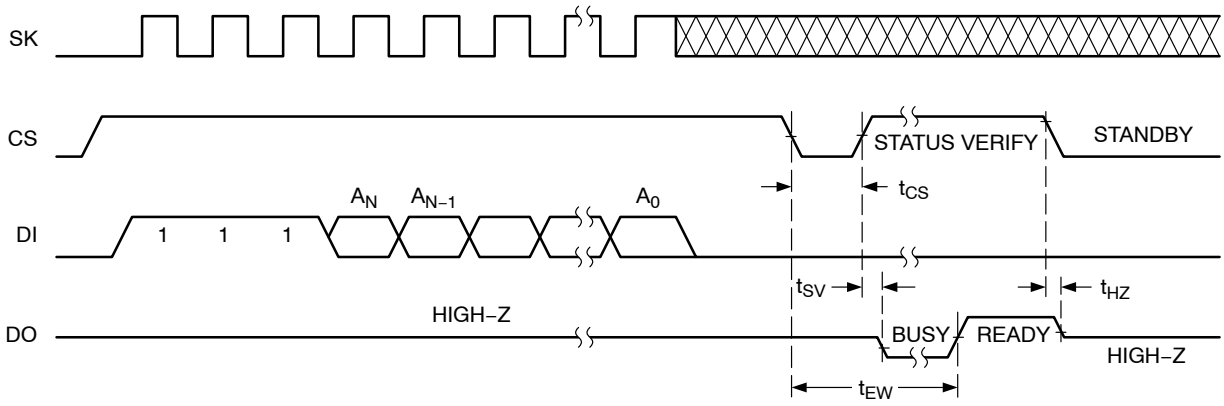


Figure 5. ERASE Instruction Timing

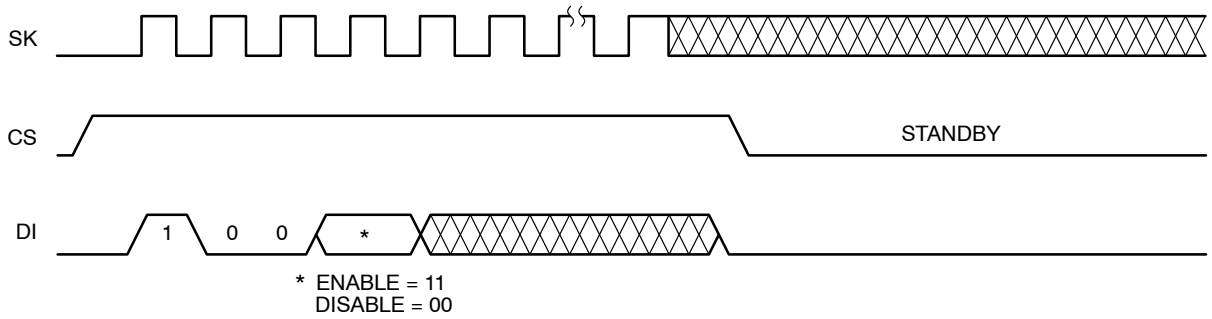


Figure 6. EWEN/EWDS Instruction Timing

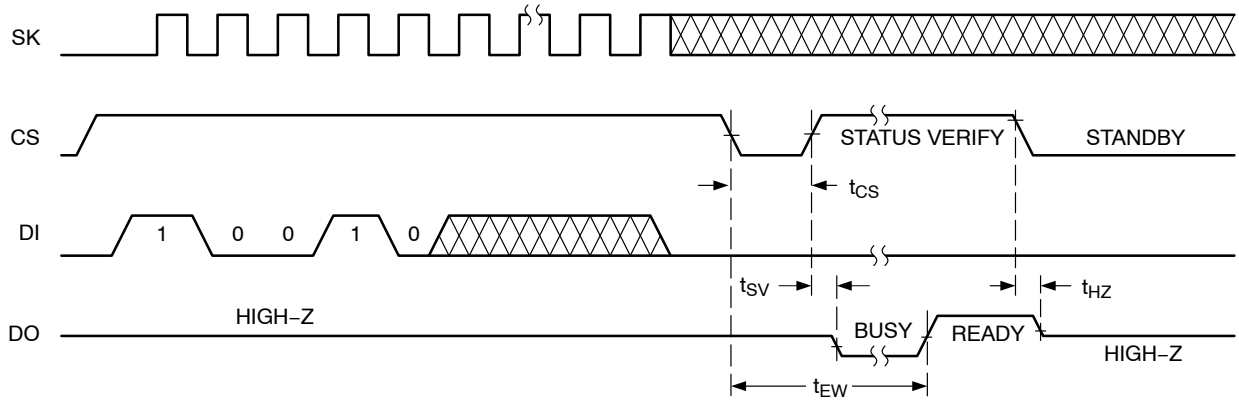


Figure 7. ERAL Instruction Timing

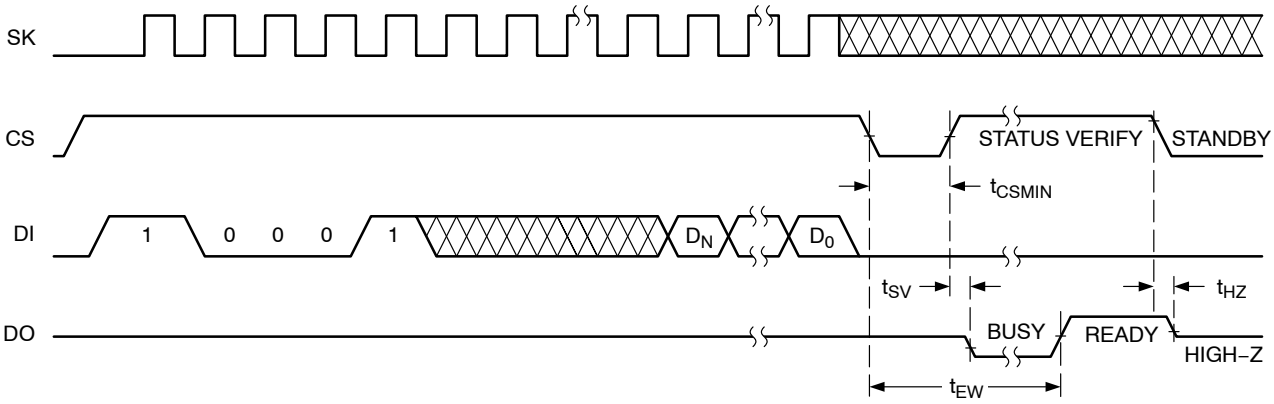


Figure 8. WRAL Instruction Timing

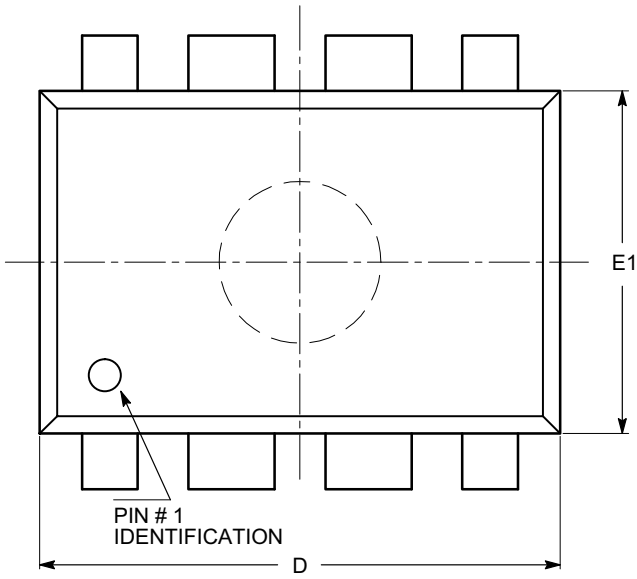
ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping
CAT93C76BLI−G	93C76D	PDIP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tube, 50 Units / Tube
CAT93C76BVI−GT3	93C76D	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BVI−G	93C76D	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tube, 100 Units / Tube
CAT93C76BVI−GT3L	93C76D	SOIC−8, JEDEC	I = Industrial (−20°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BVE−GT3	93C76D	SOIC−8, JEDEC	E = Extended (−40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BYI−GT3	M76D	TSSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BYI−G	M76D	TSSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tube, 100 Units / Tube
CAT93C76BYI−GT3L	M76D	TSSOP−8	I = Industrial (−20°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BYE−GT3	M76D	TSSOP−8	E = Extended (−40°C to +125°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BHU4I−GT3	M3U	UDFN−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT93C76BZI−GT3	M3YM	MSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

8. All packages are RoHS−compliant (Lead−free, Halogen−free).
9. The standard lead finish is NiPdAu.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
11. For additional package and temperature options, please contact your nearest ON Semiconductor sales office.
12. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

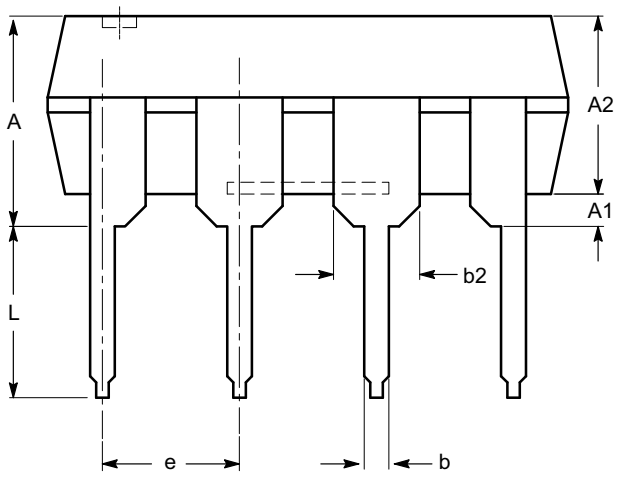
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

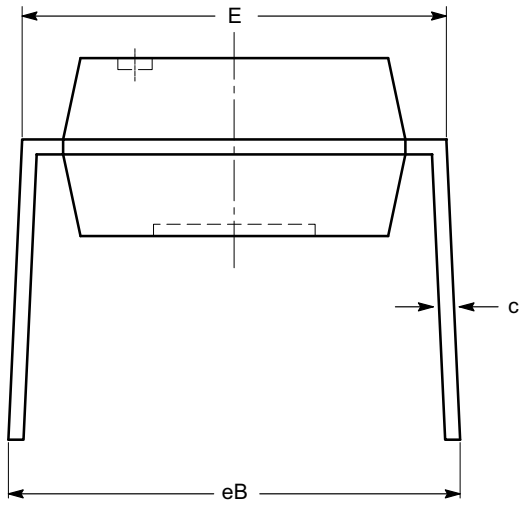


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

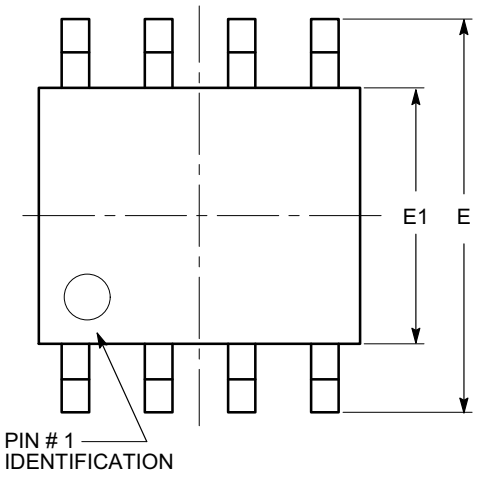


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

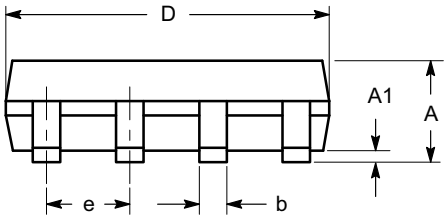
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

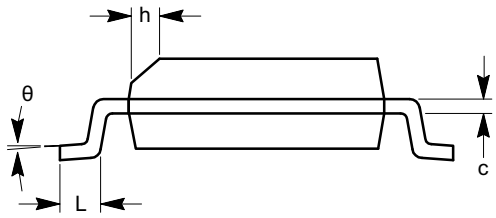


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

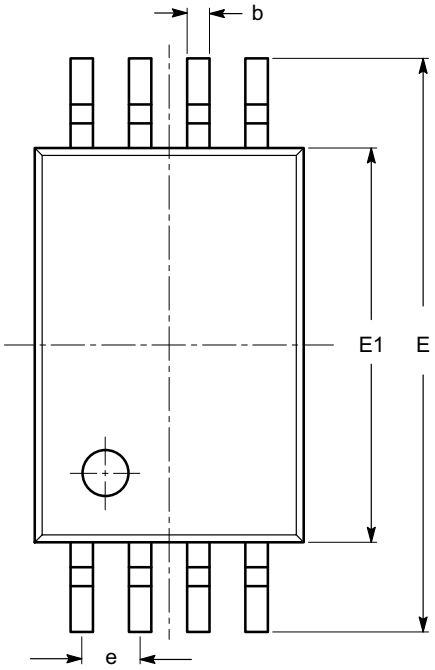


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

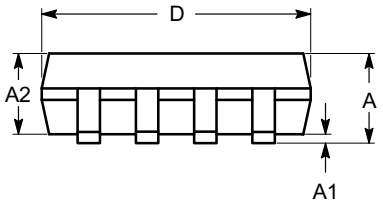
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

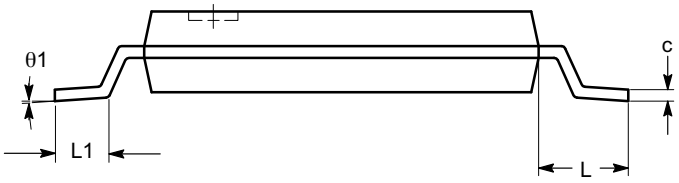


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

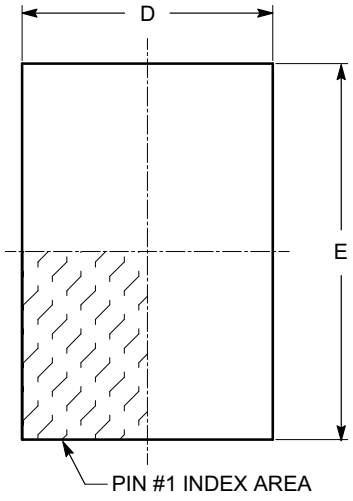


END VIEW

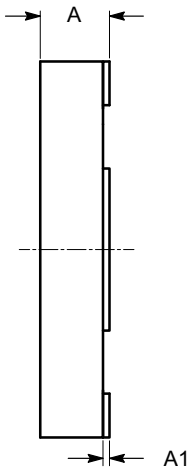
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PACKAGE DIMENSIONS

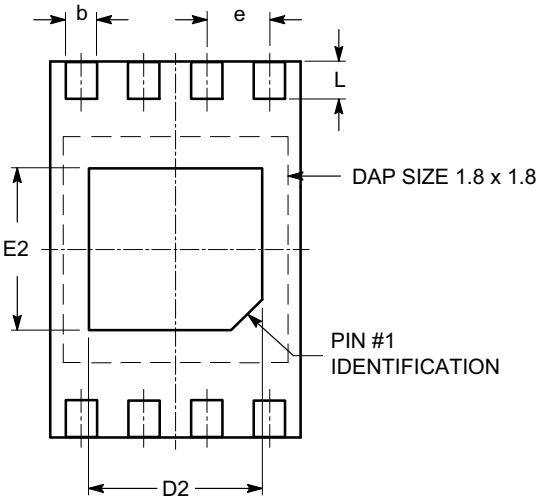
UDFN8, 2x3 EXTENDED PAD
CASE 517AZ−01
ISSUE O



TOP VIEW



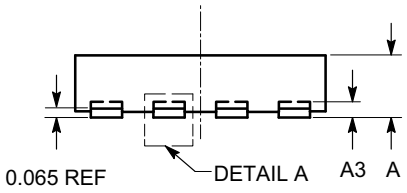
SIDE VIEW



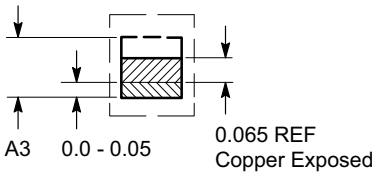
BOTTOM VIEW

SYMBOL	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
A3		0.127 REF	
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D2	1.35	1.40	1.45
E	2.95	3.00	3.05
E2	1.25	1.30	1.35
e		0.50 REF	
L	0.25	0.30	0.35

Notes:
(1) All dimensions are in millimeters.
(2) Refer JEDEC MO-236/MO-252.



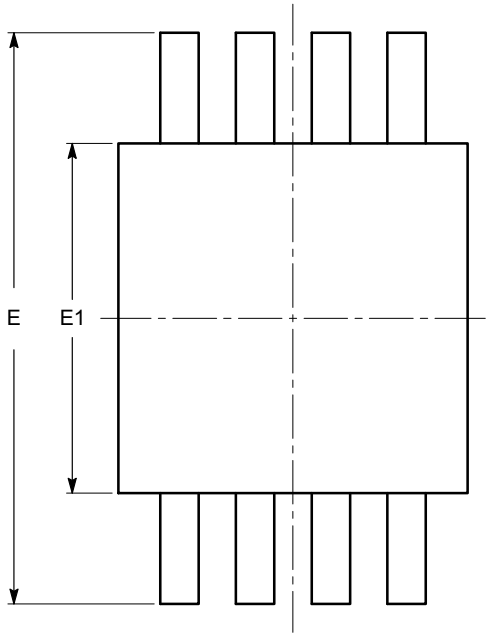
FRONT VIEW



DETAIL A

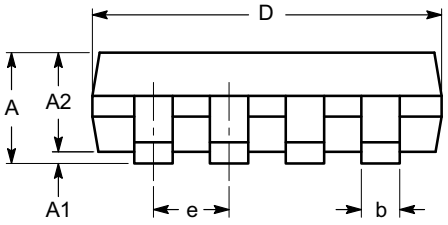
PACKAGE DIMENSIONS

MSOP 8, 3x3
CASE 846AD−01
ISSUE O

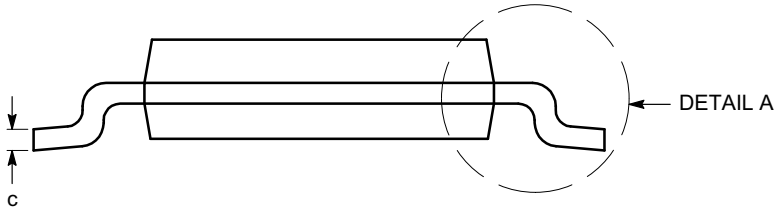


TOP VIEW

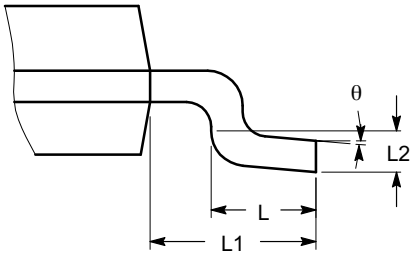
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e		0.65 BSC	
L	0.40	0.60	0.80
L1		0.95 REF	
L2		0.25 BSC	
θ	0°		6°



SIDE VIEW



END VIEW



DETAIL A

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for EEPROM ***category:***

Click to view products by ON Semiconductor ***manufacturer:***

Other Similar products are found below :

M29F040-70K6 718278CB 718620G 444358RB 444362FB BR93C46-WMN7TP EEROMH CAT25320YIGT-KK LE24C162-R-E 5962-8751409YA BR9016AF-WE2 LE2464DXATBG CAS93C66VP2I-GT3 W60002FT20T CAT24S128C4UTR ZD24C64B-SSGMA0 BL24C04F-RRRC S-25C040A0I-I8T1U AT24C256BY7-YH-T M24C64-DFCT6TPK BR24C21FJ-E2 BR24G02FVJ-3GTE2 BR24L16FJ-WE2 BR24L16FVJ-WE2 BR24S16FJ-WE2 BR24S256F-WE2 BR93L56RFV-WE2 BR93L66F-WE2 BR93L76RFV-WE2 CAT24C64C4CTR CHL24C32WEGT3 AT28HC256E-12SU-T AT93C46DY6-YH-T BR24T02FVT-WSGE2 M35B32-WMN6TP M24C64-FMC6TG M24C08-WDW6TP CAT25080VP2IGTQH CAT25020ZIGT-QP CAT24C01VP2I-GT3 CAT93C76BZI-GT3 CAT64LC40WI-T3 CAT25256HU4E-GT3 CAT25128VP2I-GT3 CAT25040VP2I-GT3 CAT25020VP2I-GT3 CAT24C16ZI-G CAT24C05LI-G CAT24C01ZI-G CAT24C05WI-G