AX-SFEU, AX-SFEU-API

Ultra-Low Power, AT Command / API Controlled, Sigfox® Compliant Transceiver IC for Up-Link and Down-Link

ON Semiconductor®

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OVERVIEW

Circuit Description

AX−SFEU and AX−SFEU−API are ultra−low power single chip solutions for a node on the Sigfox network with both up− and down−link functionality. The AX−SFEU chip is delivered fully ready for operation and contains all the necessary firmware to transmit and receive data from the Sigfox network in Europe. It connects to the customer product using a logic level RS232 UART. AT commands are used to send frames and configure radio parameters.

The AX−SFEU−API variant is intended for customers wishing to write their own application software based on the AX−SF−LIB−1−GEVK library.

Features

Functionality and Ecosystem

- Sigfox up−link and down−link functionality controlled by AT commands or API
- The AX−SFEU and AX−SF−API ICs are part of a whole development and product ecosystem available from ON Semiconductor for any Sigfox requirement. Other parts of the ecosystem include
  - Ready to go development kit DVK−SFEU−[API]−1−GEVK including a 2 year Sigfox subscription
  - Sigfox Ready® certified reference design for the AX−SFEU and AX−SFEU−API ICs
  - AX−SF10−MINI21−868−B1 and AX−SF10−ANT21−868−B1, Sigfox compliant SMT modules based on AX−SFEU with 50 Ω pads or chip antenna. Not available for AX−SFEU−API

General Features

- QFN40 5 mm x 7 mm package
- Supply range 1.8 V* − 3.6 V
- −40°C to 85°C
- Temperature sensor
- Supply voltage measurements

*The device is operational from 1.8 V to 3.6 V. However, a supply voltage below 2.0 V is considered an extreme condition. Details see Table 4.

- 10 GPIO pins
  - 4 GPIO pins with selectable voltage measure functionality, differential (1 V or 10 V range) or single ended (1 V range) with 10 bit resolution
  - 2 GPIO pins with selectable sigma delta DAC output functionality
  - 2 GPIO pins with selectable output clock
  - 3 GPIO pins selectable as SPI master interface
  - Integrated RX/TX switching with differential antenna pins

Power Consumption

- Ultra−low Power Consumption:
  - Charge required to send a Sigfox OOB packet at 14 dBm output power: 0.28 C
  - Deepsleep mode current: 100 nA
  - Sleep mode current: 1.3 μA
  - Standby mode current: 0.5 mA
  - Continuous radio RX−mode at 869.525 MHz : 10 mA
  - Continuous radio TX−mode at 868.130 MHz
    19 mA @ 0 dBm
    49 mA @ 14 dBm

High Performance Narrow−band Sigfox RF Transceiver

- Receiver
  - Carrier frequency 869.525 MHz
  - Data−rate 600 bps FSK
  - Sensitivity
    −126 dBm @ 600 bps, 869.525 MHz, GFSK
  - 0 dBm maximum input power
- Transmitter
  - Carrier frequency 868.13 MHz
  - Data−rate 100 bps PSK
  - High efficiency, high linearity integrated power amplifier
  - Maximum output power 14 dBm
  - Power level programmable in 1 dBm steps

Applications

Sigfox networks up−link and down−link.

BLOCK DIAGRAM

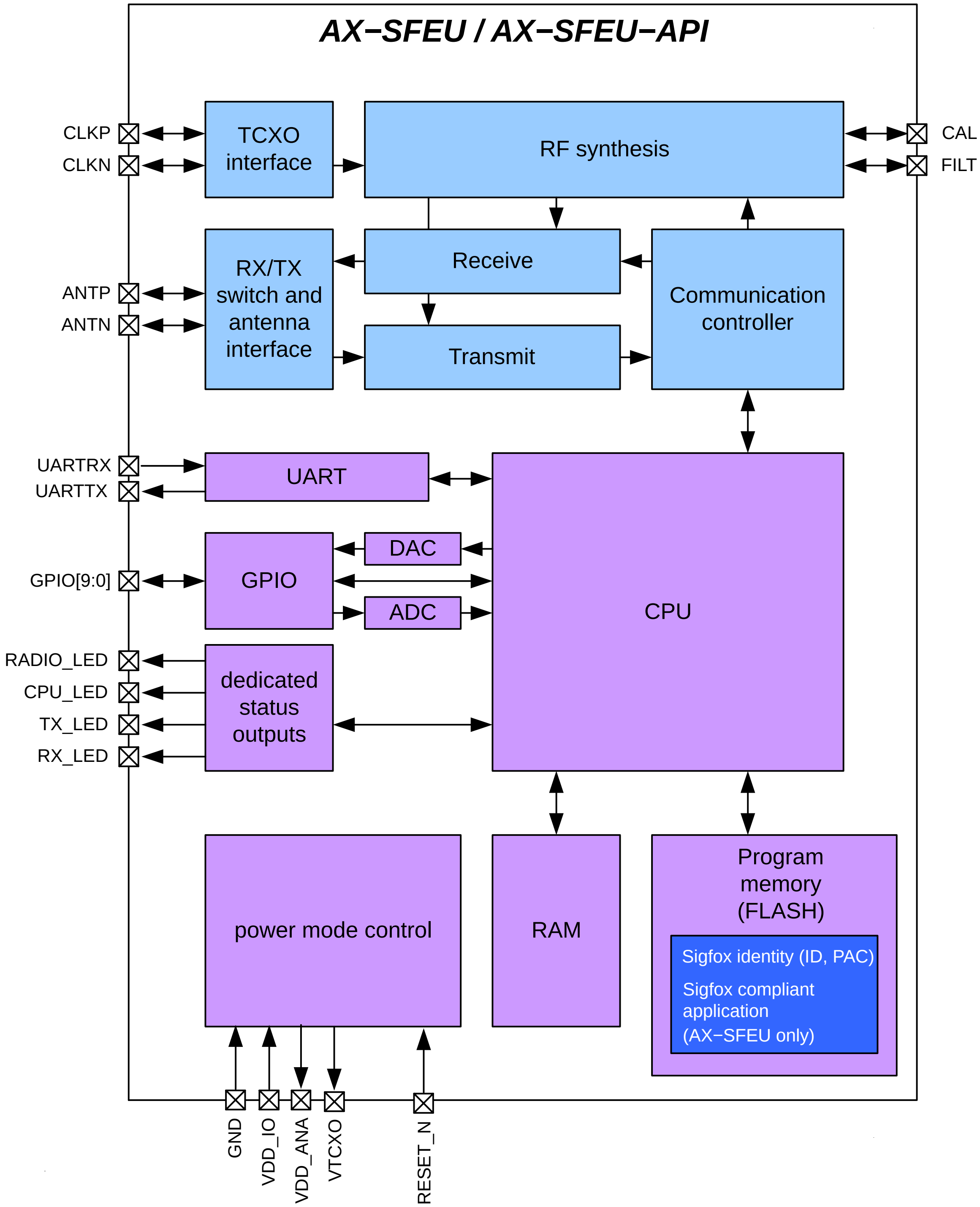


Figure 1. Functional Block Diagram of the AX−SFEU / AX−SFEU−API

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
VDD_ANA	1	P	Analog power output, decouple to neighboring GND
GND	2	P	Ground, decouple to neighboring VDD_ANA
ANTP	3	A	Differential antenna input/output
ANTN	4	A	Differential antenna input/output
NC	5	N	Do not connect
GND	6	P	Ground, decouple to neighboring VDD_ANA
VDD_ANA	7	P	Analog power output, decouple to neighboring GND
GND	8	P	Ground
FILT	9	A	Synthesizer filter
L2	10	A	Must be connected to pin L1
L1	11	A	Must be connected to pin L2
NC	12	N	Do not connect
GPIO8	13	I/O/PU	General purpose IO
GPIO7	14	I/O/PU	General purpose IO, selectable SPI functionality (MISO)
GPIO6	15	I/O/PU	General purpose IO, selectable SPI functionality (MOSI)
GPIO5	16	I/O/PU	General purpose IO, selectable SPI functionality (SCK)
GPIO4	17	I/O/PU	General purpose IO, selectable ΣΔ DAC functionality, selectable dock functionality
CPU_LED	18	O	CPU activity indicator
RADIO_LED	19	O	Radio activity indicator
VTCXO	20	O	TCXO power
GPIO9	21	I/O/PU	General purpose IO, wakeup from deep sleep
UARTTX	22	O	UART transmit
UARTRX	23	I/PU	UART receive
RX_LED	24	O	Receive activity indicator
TX_LED	25	O	Transmit activity indicator
NC	26	PD	Do not connect
RESET_N	27	I/PU	Optional reset pin. Internal pull−up resistor is permanently enabled, nevertheless it is recommended to connect this pin to VDD_IO if it is not used.
GND	28	P	Ground
VDD_IO	29	P	Unregulated power supply
GPIO0	30	I/O/A/PU	General purpose IO, selectable ADC functionality, selectable ΣΔ DAC functionality, selectable clock functionality
GPIO1	31	I/O/A/PU	General purpose IO, selectable ADC functionality
GPIO2	32	I/O/A/PU	General purpose IO, selectable ADC functionality
NC	33	N	Do not connect
NC	34	N	Do not connect
GPIO3	35	I/O/A/PU	General purpose IO, selectable ADC functionality
VDD_IO	36	P	Unregulated power supply
CAL	37	A	Connect to FILT as shown in the application diagram
NC	38	N	Connect to Ground
CLKN	39	A	TCXO interface

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
CLKP	40	A	TCXO interface
GND	Center pad	P	Ground on center pad of QFN, must be connected

A = analog input
I = digital input signal
O = digital output signal
PU = pull−up
I/O = digital input/output signal
N = not to be connected
P = power or ground
PD = pull−down

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible. Pins GPIO[3:0] must not be driven above VDD_IO, all other digital inputs are 5 V tolerant. All GPIO pins and UARTRX start up as input with pull−up. For explanations on how to use the GPIO pins, see chapter “AT Commands”.

Table 2.

Pin	Possible GPIO Modes
GPIO0	0, 1, Z, U, A, T
GPIO1	0, 1, Z, U, A
GPIO2	0, 1, Z, U, A
GPIO3	0, 1, Z, U, A
GPIO4	0, 1, Z, U, T
GPIO5	0, 1, Z, U
GPIO6	0, 1, Z, U
GPIO7	0, 1, Z, U
GPIO8	0, 1, Z, U
GPIO9	0, 1, Z, U

0 = pin drives
1 = not to be connected
Z = pin is high impedance input
U = pin is input with pull−up
A = pin is analog input
T = pin is driven by clock or DAC

Pinout Drawing

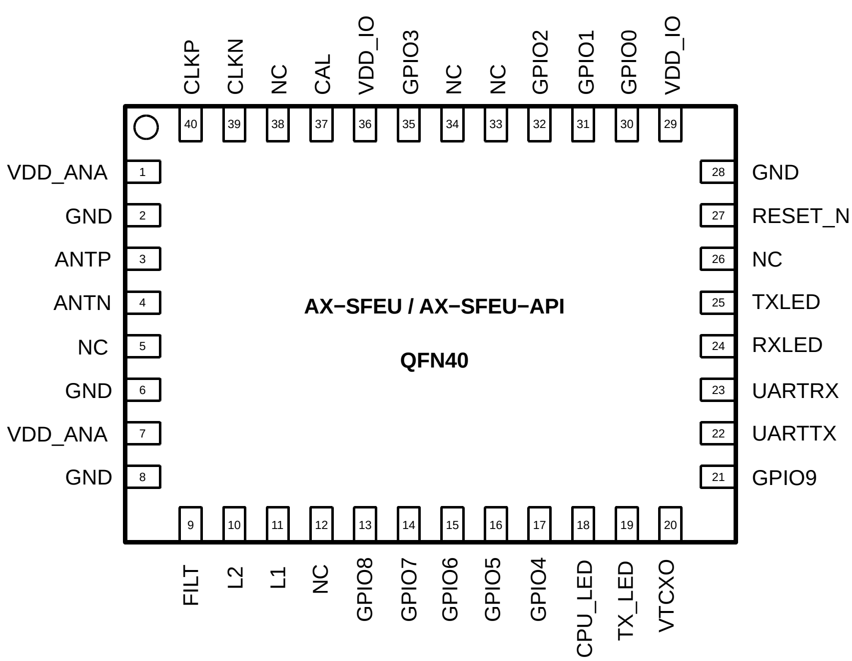


Figure 2. Pinout Drawing (Top View)

SPECIFICATIONS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Units
VDD_IO	Supply voltage		−0.5	5.5	V
IDD	Supply current			200	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input	ANTP and ANTN pins in RX mode		10	dBm
I_{I1}	DC current into any pin except ANTP, ANTN		−10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		−100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		−0.5	5.5	V
	Input voltage digital pins		−0.5	5.5	V
V_{es}	Electrostatic handling	HBM	−2000	2000	V
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−65	150	°C
T_j	Junction Temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 4. SUPPLIES

Conditions for all current and charge values unless otherwise specified are for the hardware configuration described in the AX−SFEU Application Note: Sigfox Compliant Reference Design.

Symbol	Description	Condition	Min	Typ	Max	Units
T_{AMB}	Operational ambient temperature		−40	27	85	°C
VDD_{IO}	I/O and voltage regulator supply voltage		1.8*	3.0	3.6	V
VDD_{IO_R1}	I/O voltage ramp for reset activation; Note 1	Ramp starts at VDD_IO ≤ 0.1 V	0.1			V/ms
VDD_{IO_R2}	I/O voltage ramp for reset activation; Note 1	Ramp starts at 0.1 V < VDD_IO < 0.7 V	3.3			V/ms
I_{DS}	Deep sleep mode current	AT$P=2		100		nA
I_{SLP}	Sleep mode current	AT$P=1		1.3		μA
I_{STDBY}	Standby mode current Note 3			0.5		mA
I_{RX_CONT}	Current consumption continuous RX	AT$SR=1,1,−1		10		mA
$Q_{SFX\_OOB\_0}$	Charge to send a Sigfox out of band message, 0 dBm	AT$S0		0.12		C
$Q_{SFX\_BIT\_0}$	Charge to send a bit, 0 dBm	AT$SB=0		0.08		C
$Q_{SFX\_BITDL\_0}$	Charge to send a bit with downlink receive, 0 dBm	AT$SB=0,1		0.27		C
$Q_{SFX\_LFR\_0}$	Charge to send the longest possible Sigfox frame (12 byte) , 0dBm	AT$SF=00112233445566778899aabb		0.14		C
$Q_{SFX\_LFRDL\_0}$	Charge to send the longest possible Sigfox frame (12 byte) with downlink receive, 0 dBm	AT$SF=00112233445566778899aabb,1		0.27		C
$Q_{SFX\_OOB\_14}$	Charge to send a Sigfox out of band message, 14 dBm	AT$S0		0.28		C
$Q_{SFX\_BIT\_14}$	Charge to send a bit, 14 dBm	AT$SB=0		0.20		C
$Q_{SFX\_BITDL\_14}$	Charge to send a bit with downlink receive, 14 dBm	AT$SB=0,1		0.35		C
$Q_{SFX\_LFR\_14}$	Charge to send the longest possible Sigfox frame (12 byte) , 14 dBm	AT$SF=00112233445566778899aabb		0.39		C
$Q_{SFX\_LFRDL\_14}$	Charge to send the longest possible Sigfox frame (12 byte) with downlink receive, 14 dBm	AT$SF=00112233445566778899aabb,1		0.46		C
$I_{TXMOD0AVG}$	Modulated Transmitter Current, Note 2	Pout=0 dBm; average		19.0		mA
$I_{TXMOD14AVG}$	Modulated Transmitter Current, Note 2	Pout=14 dBm; average		49.0		mA

*The device is operational from 1.8 V to 3.6 V. However, a supply voltage below 2.0 V is considered an extreme condition and operation can lead to reduced output power and increased spurious emission.

1. If VDD_IO ramps cannot be guaranteed, an external reset circuit is recommended, see the AX8052 Application Note: Power On Reset
2. The output power of the AX−SFEU / AX−SFEU−API can be programmed in 1 dB steps from 0 dBm – 14 dBm. Current consumption values are given for a matching network that is optimized for 14 dBm output. 0 dBm transmission with typically 10 mA can be achieved with other networks that are optimized for 0 dBm operation.
3. Internal 20 MHz iscillator, voltage conditioning and supervisory circuit running.

Typical Current Waveform

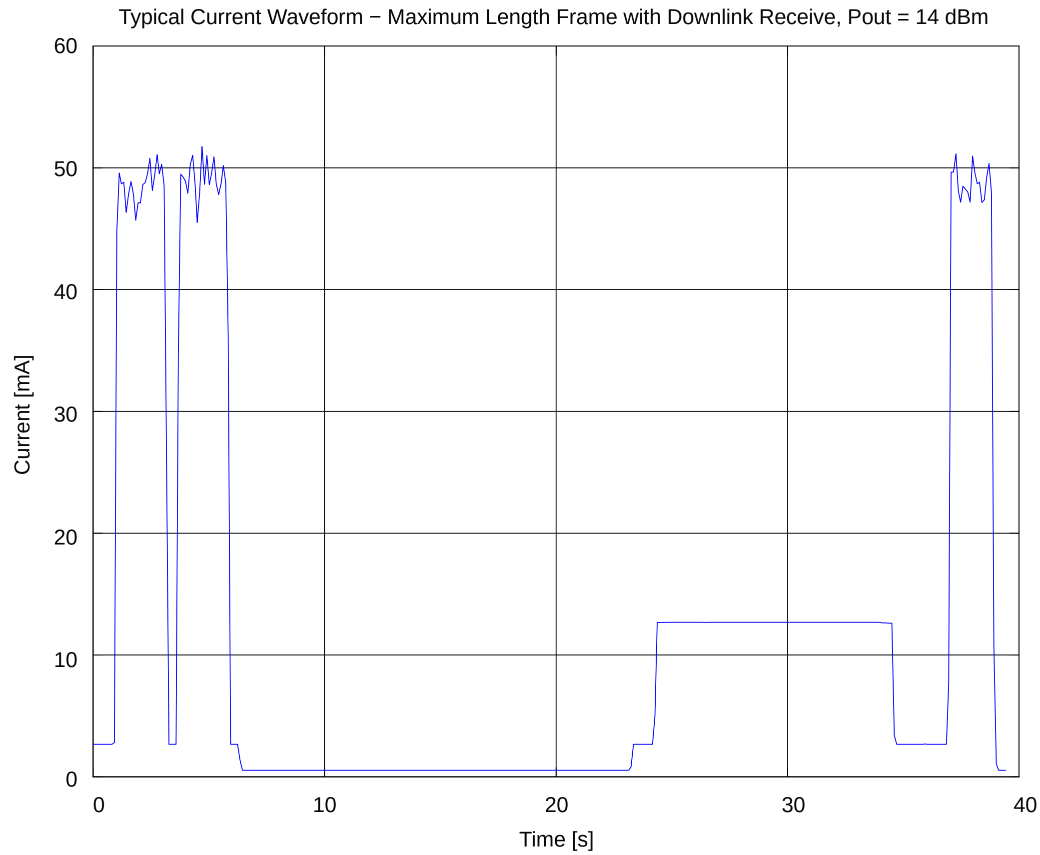


Figure 3. Typical Current Waveform for a Maximum Length Frame with Downlink Receive at 14 dBm Output Power

Battery Life Examples

Scenario 1:

- CR2032 coin cell battery
- One OOB frame transmitter per day at Pout=0 dBm
- Device in Sleep
- Neglecting battery self discharge

CR2032 capacity	225 mAh * 3600 s/h	810 C
Sleep charge per day	1.3 μA * 86400 s	0.11 C/day
OOB frame transmission		0.12 C/day
Total Charge consumption		0.23 C/day
Battery life		9.6 Years

Scenario 2:

- 2 AAA Alkaline batteries in series
- One OOB frame transmitter per day at Pout=14 dBm
- Four maximum length frames with downlink receive per day at Pout=14 dBm
- Device in Sleep
- Neglecting battery self discharge

2 AAA alkaline capacity	1500 mAh * 3600 s/h	5400 C
Sleep charge per day	1.3 μA * 86400 s	0.11 C/day
OOB frame transmission		0.28 C/day
Frame transmission with downlink	4 * 0.46 C/day	1.84 C/day
Total Charge consumption		2.26 C/day
Battery life		6.5 Years

Table 5. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Units
Digital Inputs						
V_{T+}	Schmitt trigger low to high threshold point	VDD_IO = 3.3 V		1.55		V
V_{T-}	Schmitt trigger high to low threshold point			1.25		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
V_{IPA}	Input voltage range, GPIO[3:0]		−0.5		VDD_IO	V
V_{IPBC}	Input voltage range, GPIO[9:4], UARTRX		−0.5		5.5	V
I_L	Input leakage current		−10		10	μA
R_{PU}	Programmable Pull−Up Resistance			65		kΩ
Digital Outputs						
I_{OH}	Output Current, high Ports GPIO[9:0], UARTTX, TXLED, RXLED, TXLED, CPULED	V_{OH} = 2.4 V	8			mA
I_{OL}	Output Current, low GPIO[9:0], UARTTX, TXLED, RXLED, TXLED, CPULED	V_{OL} = 0.4 V	8			mA
I_{OZ}	Tri−state output leakage current		−10		10	μA

AC Characteristics

Table 6. TCXO REFERENCE INPUT

Symbol	Description	Condition	Min	Typ	Max	Units
f_{TCXO}	TCXO frequency	A passive network between the TCXO output and the pins CLKP and CLKN is required. For detailed TCXO network recommendations depending on the TCXO output swing refer to the AX5043 Application Note: Use with a TCXO Reference Clock. For TCXO recommendations see the Ax−SFEU Application Note: Sigfox Compliant Reference Design		48		MHz

Table 7. TRANSMITTER

Conditions for transmitter specifications unless otherwise specified with the antenna network from AX−SFEU Application Note: Sigfox Compliant Reference Design and at 868.130 MHz.

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate			100		bps
PTX_{min}	Lowest Transmitter output power	AT$CW=868130000,1,0		0		dBm
PTX_{max}	Highest Transmitter output power	AT$CW=868130000,1,14		14		dBm
PTX_{step}	Programming step size output power			1		dB
dTX_{temp}	Transmitter power variation vs. temperature	−40°C to +85°C		±0.5		dB
dTX_{Vdd}	Transmitter power variation vs. VDD_IO	1.8 to 3.6 V		±0.5		dB
PTX_{harm2}	Emission @ 2nd harmonic			−51		dBc
PTX_{harm3}	Emission @ 3rd harmonic			−63		
PTX_{harm4}	Emission @ 4th harmonic			−84		

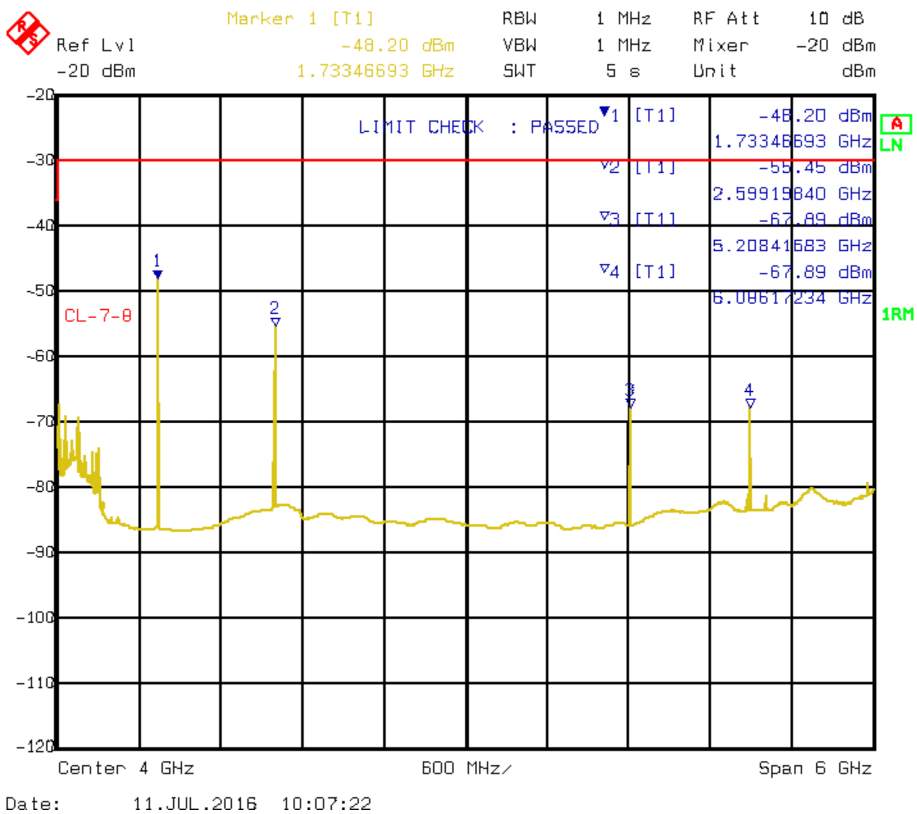


Figure 4. Typical Spectrum with Harmonics at 14 dBm Output Power

Table 8. RECEIVER

Conditions for transmitter specifications unless otherwise specified with the antenna network from AX−SFEU Application Note: Sigfox Compliant Reference Design and at 869.525 MHz.

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate			600		bps
IS_{BER868}		AT$SB=x,1, AT$SF=x,1, AT$SR PER < 0.1		−126		dBm
BLK_{2M_868}	Blocking at ±2 MHz offset	Channel/Blocker @ PER = 0.1, wanted signal level is +3 dB above the typical sensitivity, the blocker signal is CW		68		dB
BLK_{10M_868}	Blocking at ±10 MHz offset	Channel/Blocker @ PER = 0.1, wanted signal level is +3 dB above the typical sensitivity, the blocker signal is CW		78		dB

Table 9. ADC / TEMPERATURE SENSOR

Symbol	Description	Condition	Min	Typ	Max	Units
ADCRES	ADC resolution			10		Bits
V_{ADCREF}	ADC reference voltage		0.95	1	1.05	V
Z_{ADC00}	Input capacitance				2.5	pF
DNL	Differential nonlinearity			± 1		LSB
INL	Integral nonlinearity			± 1		LSB
OFF	Offset			3		LSB
GAIN_ERR	Gain error			0.8		%
ADC in Differential Mode						
V_{ABS_DIFF}	Absolute voltages & common mode voltage in differential mode at each input		0		VDD_IO	V
V_{FS_DIFF01}	Full swing input for differential signals	Gain x1	−500		500	mV
V_{FS_DIFF10}		Gain x10	−50		50	mV
ADC in Single Ended Mode						
V_{MID_SE}	Mid code input voltage in single ended mode			0.5		V
V_{IN_SE00}	Input voltage in single ended mode		0		VDD_IO	V
V_{FS_SE01}	Full swing input for single ended signals	Gain x1	0		1	V
Temperature Sensor						
T_{RNG}	Temperature range	AT$T?	−40		85	°C
T_{ERR_CAL}	Temperature error	AT$T?	−2		2	°C

COMMAND INTERFACE

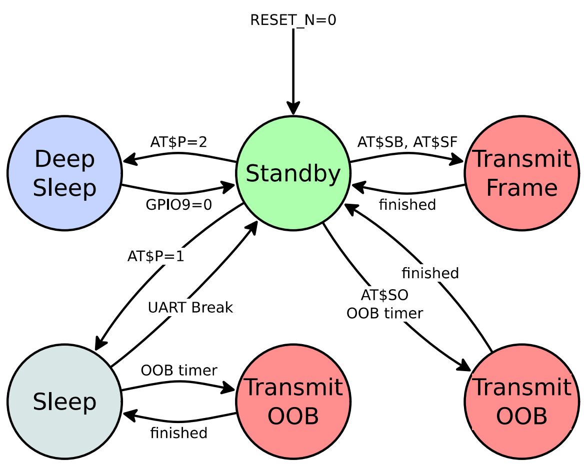
General Information

The chapter “Command Interface” is a documentation of the AT−Command set for devices which do not have an API−interface. To see whether the device is capable of receiving AT−Commands, please refer to chapter “Part Numbers”. If the device has been shipped with the API−Interface, please refer to the SW manual and ”apiexample” code delivered with AX−SF−LIB−1−GEVK for an introduction on how to setup a project and how to use the API−Interface.

Serial Parameters: 9600, 8, N, 1

The AX−SFEU uses the UART (pins UARTTX, UARTRX) to communicate with a host and uses a bitrate of **9600 baud**, no parity, 8 data bits and one stop bit.

Power Modes



Standby

After Power−Up and after finishing a SIGFOX transmission, AX−SFEU enters Standby mode. In Standby mode, AX−SFEU listens on the UART for commands from the host. Also, OOB frames are transmitted whenever the OOB timer fires. To conserve power, the AX−SFEU can be put into Sleep or turned off (Deep Sleep) completely.

Sleep

The command **AT$P=1** is used to put the AX−SFEU into Sleep mode. In this mode, only the wakeup timer for out−of−band messages is still running. To wake the AX−SFEU up from Sleep mode toggle the serial UARTRX pin, e.g. by sending a break (break is an RS232 framing violation, i.e. at least 10 bit durations low). When an Out of Band (OOB) message is due, AX−SFEU automatically wakes up to transmit the message, and then returns to Sleep mode.

Deep Sleep

In Deep Sleep mode, the AX−Sigfox is completely turned off and only draws negligible leakage current. Deep Sleep mode can be activated with **AT$P=2**. To wake−up from Deep Sleep mode, GPIO9 is pulled to GND.

When using Deep Sleep mode, keep two things in mind: Everything is turned off, timers are not running at all and all settings will be lost (use **AT$WR** to save settings to flash before entering Deep Sleep mode). Out−of−band messages will therefore not be sent. The pins states are frozen in Deep Sleep mode. The user must ensure that this will not result in condition which would draw a lot of current.

AT Commands

Numerical Syntax

hexdigit	::= [0−9A−Fa−f]
hexnum	::= “0x” hexdigit+
decnum	::= “0” | [1−9] [0−9]*
octnum	::= “0” [0−7]+
binnum	::= “0b” [01]+
bit	::= [01]
optnum	::= “−1”
frame	::= (hexdigit hexdigit)+
uint	::= hexnum | decnum | octnum | binnum
uint_opt	::= uint | optnum

Command Syntax

A command starts with ‘AT’ (everything is case sensitive!), continues with the actual command followed by parameters (if any) and ends with any kind of whitespace (space, tab, newline etc.)

If incorrect syntax is detected (“parsing error”) all input is ignored up until the next whitespace character.

Also note that any number can be entered in any format (Hexadecimal, Decimal, Octal and binary) by adding the corresponding prefix (‘0x’, ‘0’, ‘0b’). The only exception is the ‘Send Frame’ command (`AT$SF`) which expects a list of hexadecimal digits without any prefix.

Return Codes

A successful command execution is indicated by sending ‘OK’. If a command returns a value (e.g. by querying a register) only the value is returned.

Examples

Bold text is sent to AX−SFEU.

AT$I=0
AXSEM AT Command Interface

Here, we execute command ‘I’ to query some general information.

AT$SF=aabb1234
OK

This sends a Sigfox frame containing { 0x00 : 0x11 : 0x22 : 0x33 : 0x44 }, then waits for a downlink response telegram, which in this example contains { 0xAA : 0xBB : 0xCC : 0xDD }.

AT$CB=0011223344,1
OK
RX=AA BB CC DD

This sends a Sigfox frame containing { 0xAA : 0xBB : 0x12 : 0x34 } without waiting for a response telegram.

AT$CB=0xAA,1
OK

The ‘CB’ command sends out a continuous pattern of bits, in this case 0xAA = 0b10101010.

AT$P=1
OK

This transitions the device into sleep mode. Out−of−band transmissions will still be triggered. The UART is powered down. The device can be woken up by a low level on the UART signal, i.e. by sending break.

Table 10. COMMANDS

Command	Name	Description
AT	Dummy Command	Just returns ‘OK’ and does nothing else. Can be used to check communication.
AT$SB=bit[,bit]	Send Bit	Send a bit status (0 or 1). Optional bit flag indicates if AX−SFEU should receive a downlink frame.
AT$SF=frame[,bit]	Send Frame	Send payload data, 1 to 12 bytes. Optional bit flag indicates if AX−SFEU should receive a downlink frame.
AT$SO	Manually send out of band message	Send the out−of−band message.
AT$TR?	Get the transmit repeat	Returns the number of transmit repeats. Default: 2
AT$TR=?	Get transmit range	Returns the allowed range of transmit repeats.
AT$TR=uint	Get transmit repeat	Sets the transmit repeat.
ATSuint?	Get Register	Query a specific configuration register’s value. See chapter “Registers” for a list of registers.
ATSuint=uint	Set Register	Change a configuration register.
ATSuint=?	Get Register Range	Returns the allowed range of transmit repeats.
AT$IF=uint	Set TX Frequency	Set the output carrier macro channel for Sigfox frames.
AT$IF?	Get TX Frequency	Get the currently chosen TX frequency.
AT$DR=uint	Set RX Frequency	Set the reception carrier macro channel for Sigfox frames.
AT$DR?	Get RX Frequency	Get the currently chosen RX frequency.
AT$CW=uint,bit[,uint_opt]	Continuous Wave	To run emission tests for Sigfox certification it is necessary to send a continuous wave, i.e. just the base frequency without any modulation. Parameters: **Name** / **Range** / **Description** Frequency / 800000000−999999999, 0 / Continuous wave frequency in Hz. Use 868130000 for Sigfox or 0 to keep previous frequency. Mode / 0, 1 / Enable or disable carrier wave. Power / 0−14 / dBm of signal | Default: 14
AT$CB=uint_opt,bit	Test Mode: TX constant byte	For emission testing it is useful to send a specific bit pattern. The first parameter specifies the byte to send. Use ‘−1’ for a (pseudo−)random pattern. Parameters: **Name** / **Range** / **Decsription** Pattern / 0−255, −1 / Byte to send. Use ‘−1’ for a (pseudo−)random pattern. Mode / 0, 1 / Enable or disable pattern test mode.
AT$T?	Get Temperature	Measure internal temperature and return it in 1/10th of a degree Celsius.
AT$V?	Get Voltages	Return current voltage and voltage measured during the last transmission in mV.

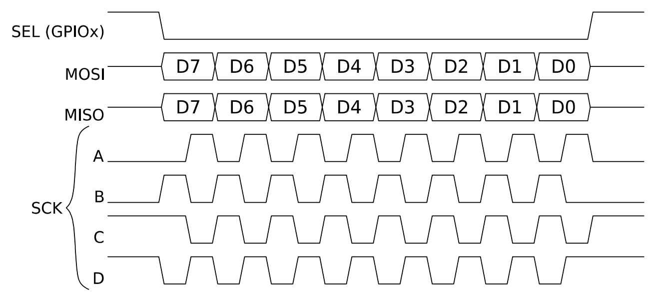
Table 10. COMMANDS

Command	Name	Description
AT$I=uint	Information	Display various product information: 0: Software Name & Version Example Response: AX−SFEU 1.0.6−ETSI 1: Contact Details Example Response: support@axsem.com 2: Silicon revision lower byte Example Response: 8F 3: Silicon revision upper byte Example Response: 00 4: Major Firmware Version Example Response: 1 5: Minor Firmware Version Example Response: 0 7: Firmware Variant (Frequency Band etc. (EU/US)) Example Response: ETSI 8: Firmware VCS Version Example Response: v1.0.2−36 9: SIGFOX Library Version Example Response: DL0−1.4 10: Device ID Example Response: 00012345 11: PAC Example Response: 0123456789ABCDEF
AT$P=uint	Set Power Mode	To conserve power, the AX−SFEU can be put to sleep manually. Depending on power mode, you will be responsible for waking up the AX−SFEU again! 0: software reset (settings will be reset to values in flash) 1: sleep (send a break to wake up) 2: deep sleep (toggle GPIO9 or RESET_N pin to wake up; the AX−SFEU is not running and all settings will be reset!)
AT$WR	Save Config	Write all settings to flash (RX/TX frequencies, registers) so they survive reset/deep sleep or loss of power. Use AT$P=0 to reset the AX−SFEU and load settings from flash.
AT:Pn?	Get GPIO Pin	Return the setting of the GPIO Pin *n*; *n* can range from 0 to 9. A character string is returned describing the mode of the pin, followed by the actual value. If the pin is configured as analog pin, then the voltage (range 0…1 V) is returned. The mode characters have the following meaning: **Mode** **Description** 0 Pin drives low 1 Pin drives high Z Pin is high impedance input U Pin is input with pull−up A Pin is analog input (GPIO pin 0…3 only) T Pin is driven by clock or DAC (GPIO pin 0 and 4 only) The default mode after exiting reset is U on all GPIO pins.
AT:Pn=?	Get GPIO Pin Range	Print a list of possible modes for a pin. The table below lists the response. **Pin** **Modes** P0 0, 1, Z, U, A, T P1 0, 1, Z, U, A P2 0, 1, Z, U, A P3 0, 1, Z, U, A P4 0, 1, Z, U, T P5 0, 1, Z, U P6 0, 1, Z, U P7 0, 1, Z, U P8 0, 1, Z, U P9 0, 1, Z, U
AT:Pn=mode	Set GPIO Pin	Set the GPIO pin mode. For a list of the modes see the command AT:Pn?

Table 10. COMMANDS

<table>
<tr><th>Command</th><th>Name</th><th>Description</th></tr>
<tr><td>AT:ADC Pn[−Pn [(1V|10V)]]?</td><td>Get GPIO Pin Analog Voltage</td><td>Measure the voltage applied to a GPIO pin. The command also allows measurement of the voltage difference across two GPIO pins. In differential mode, the full scale range may also be specified as 1 V or 10 V. Note however that the pin input voltages must not exceed the range 0..VDD_IO. The command returns the result as fraction of the full scale range (1 V if none is specified). The GPIO pins referenced should be initialized to analog mode before issuing this command.</td></tr>
<tr><td>AT:SPI[(A|B|C|D)]=bytes</td><td>SPI Transaction</td><td>This command clocks out bytes on the SPI port. The clock frequency is 312.5 kHz. The command returns the bytes read on MISO during output. Optionally the clocking mode may be specified (default is A):

Mode | Clock Inversion | Clock Phase
A | normal | normal
B | normal | alternate
C | inverted | normal
D | inverted | alternate



Note that SEL, if needed, is not generated by this command, and must instead be driven using standard GPIO commands (AT:Pn=0|1).</td></tr>
<tr><td>AT:CLK=freq,reffreq</td><td>Set Clock Generator</td><td>Output a square wave on the pin(s) set to T mode. The frequency of the square wave is (freq / 2^{16}) × reffreq. Possible values for reffreq are 20000000, 10000000, 5000000, 2500000, 1250000, 625000, 312500, 156250. Possible values if freq are 0…65535.</td></tr>
<tr><td>AT:CLK=OFF</td><td>Turn off Clock Generator</td><td>Switch off the clock generator</td></tr>
<tr><td>AT:CLK?</td><td>Get Clock Generator</td><td>Return the settings of the clock generator. Two numbers are returned, freq and reffreq.</td></tr>
<tr><td>AT:DAC=value</td><td>Set ΣΔ DAC</td><td>Output a ΣΔ DAC value on the pin(s) set to T mode. Parameter value may be in the range −32768…32767. The average output voltage is (1/2 + value / 2^{17}) × VDD.
An external low pass filter is needed to get smooth output voltages. The modulation frequency is 20 MHz. A possible low pass filter choice is a simple RC low pass filter with R = 10 kΩ and C = 1 μF.</td></tr>
<tr><td>AT:DAC=OFF</td><td>Turn off ΣΔ DAC</td><td>Switch off the DAC</td></tr>
<tr><td>AT:DAC?</td><td>Get ΣΔ DAC</td><td>Return the DAC value</td></tr>
</table>

Table 10. COMMANDS

Command	Name	Description
AT$TM=mode,config	Activates the Sigfox Testmode	Available test modes: 0. TX BPSK Send only BPSK with Synchro Bit + Synchro frame + PN sequence: No hopping centered on the TX_frequency. Config bits 0 to 6 define the number of repetitions. Bit 7 of config defines if a delay is applied of not in the loop 1. TX Protocol: Tx mode with full protocol with Sigfox key: Send Sigfox protocol frames with initiate downlink flag = True. Config defines the number of repetitions. 2. RX Protocol: This mode tests the complete downlink protocol in Downlink only. Config defines the number of repetitions. 3. RX GFSK: RX mode with known pattern with SB + SF + Pattern on RX_frequency (internal comparison with received frame ⇔ known pattern = AA AA B2 27 1F 20 41 84 32 68 C5 BA AE 79 E7 F6 DD 9B. Config defines the number of repetitions. Config defines the number of repetitions. 4. RX Sensitivity: Does uplink + downlink frame with Sigfox key and specific timings. This test is specific to SIGFOX’s test equipments & softwares. 5. TX Synthesis: Does one uplink frame on each Sigfox channel to measure frequency synthesis step
AT$SE	Starts AT$TM−3,255 indefinitely	Convenience command for sensitivity tests
AT$SL[=frame]	Send local loop	Sends a local loop frame with optional payload of 1 to 12 bytes. Default payload: 0x84, 0x32, 0x68, 0xC5, 0xBA, 0x53, 0xAE, 0x79, 0xE7, 0xF6, 0xDD, 0x9B.
AT$RL	Receive local loop	Starts listening for a local loop.

Table 11. REGISTERS

Number	Name	Description	Default	Range	Units
300	Out Of Band Period	AX−SFEU sends periodic static messages to indicate that they are alive. Set to 0 to disable.	24	0−24	hours
302	Power Level	The output power of the radio.	14	0−14	dBm

APPLICATION INFORMATION

Typical Application Diagrams

Typical AX−SFEU / AX−SFEU−API Application Diagram

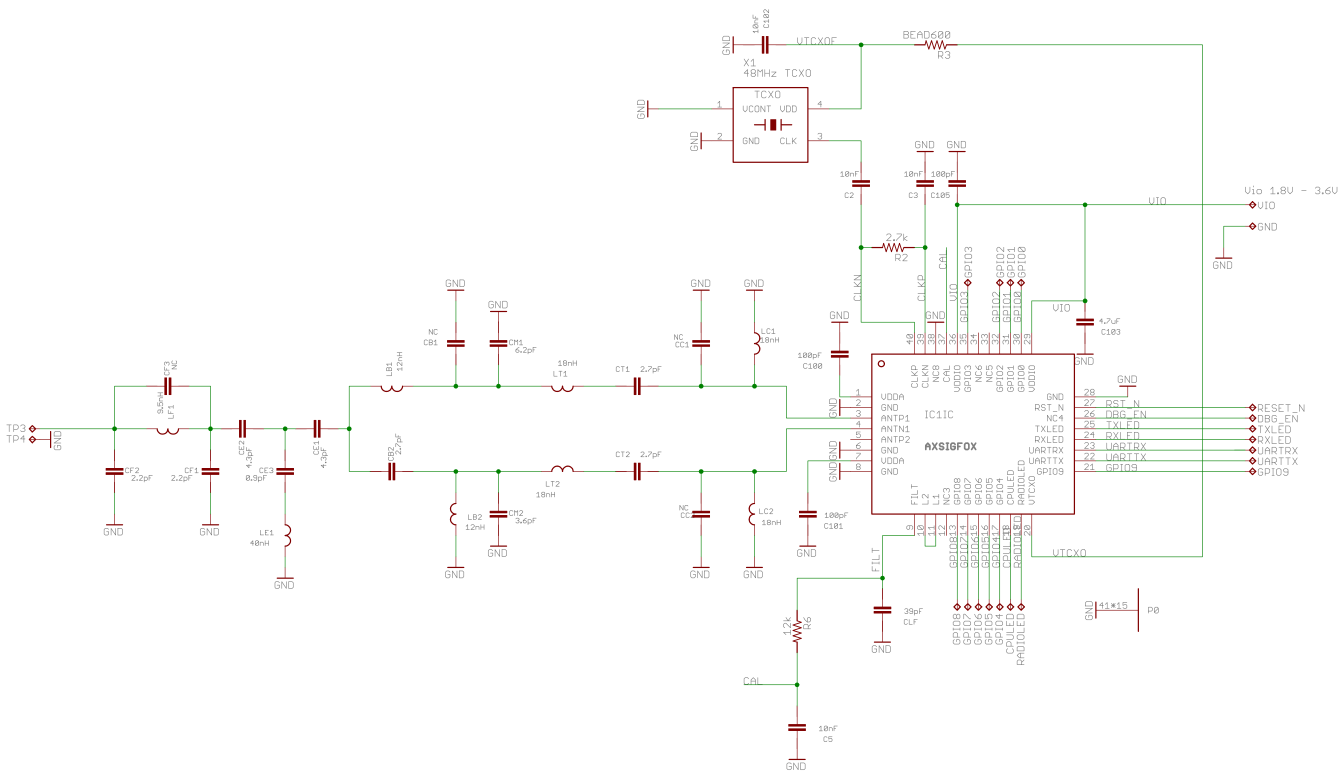
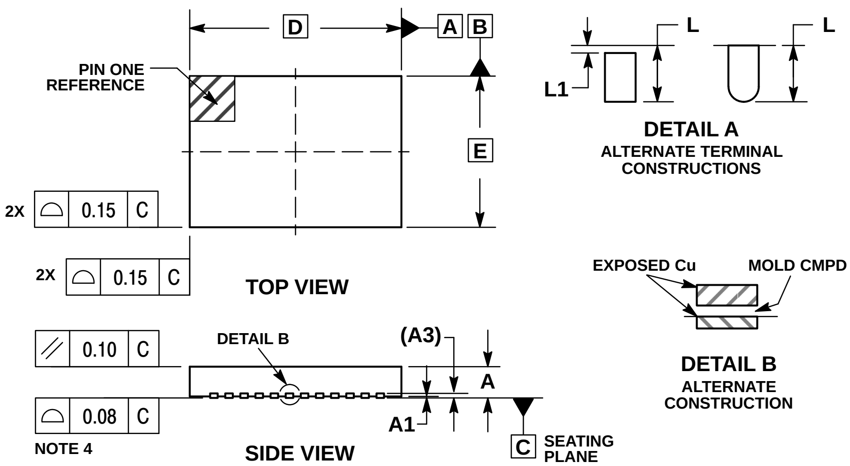


Figure 5. Typical Application Diagram

For detailed application configuration and BOM see the AX−SFEU Application Note: Sigfox Compliant Reference Design.

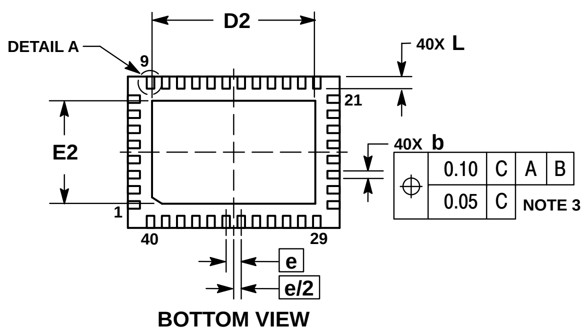
QFN40 PACKAGE INFORMATION

QFN40 7x5, 0.5P
CASE 485EG
ISSUE A

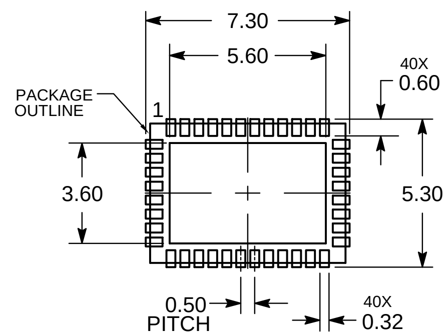


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D2	5.30	5.50
E	5.00 BSC	
E2	3.30	3.50
e	0.50 BSC	
L	0.30	0.50
L1	−−−	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

QFN40 Soldering Profile

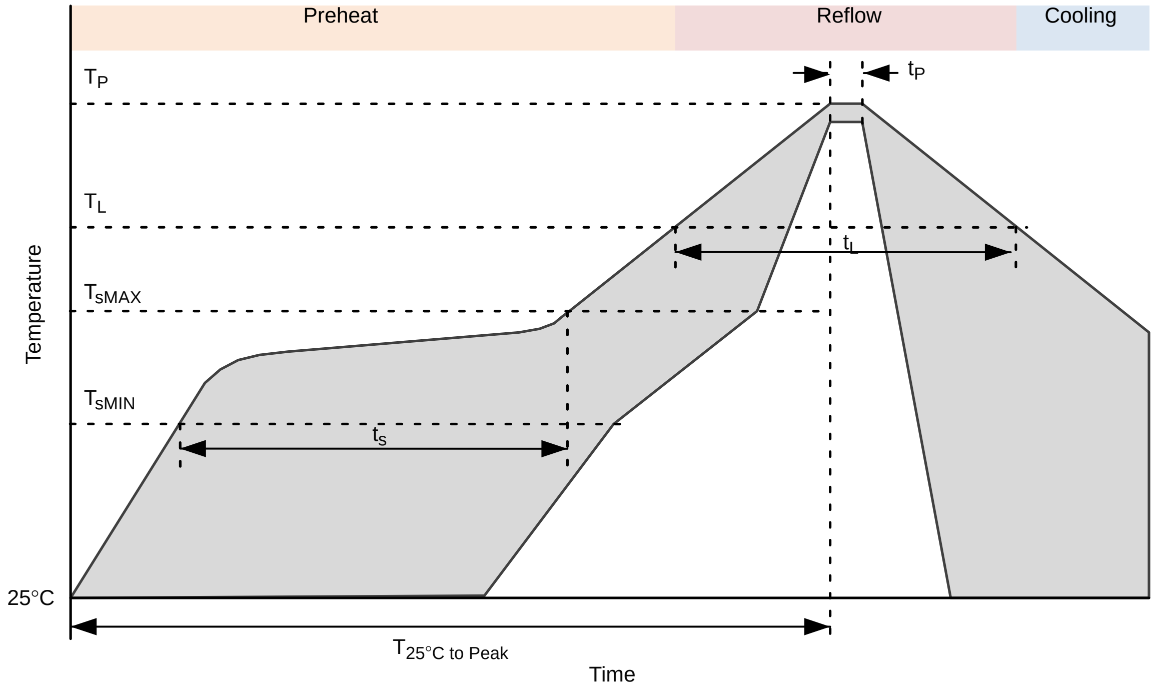


Figure 6. QFN40 Soldering Profile

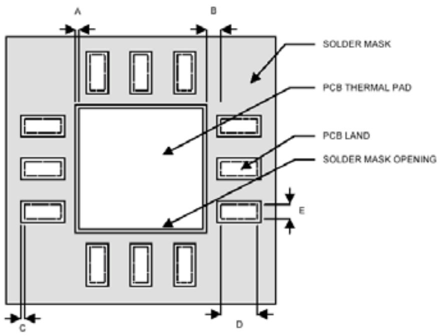
Table 12.

Profile Feature		Pb−Free Process
Average Ramp−Up Rate		3°C/s max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 – 180 sec
Time 25°C to Peak Temperature	$T_{25°C\ to\ Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 – 150 s
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 – 40 s
Cooling Phase		
Ramp−down rate		6°C/s max.

1. All temperatures refer to the top side of the package, measured on the the package body surface.

QFN40 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 7.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
D = PCB land length = QFN solder pad length + 0.1 mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 7. PCB Land and Solder Mask Recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 8.
4. The aperture opening for the signal pads should be between 50−80% of the QFN pad area as shown in Figure 9.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No−clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water−soluble flux is used.

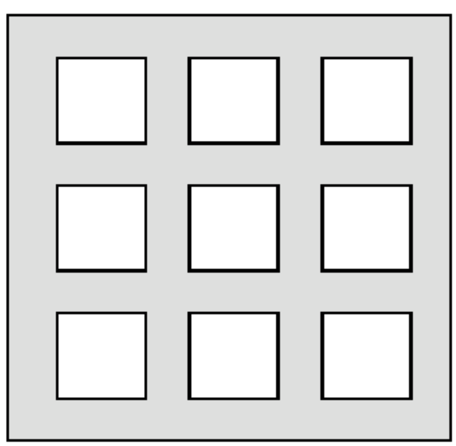


Figure 8. Solder Paste Application on Exposed Pad

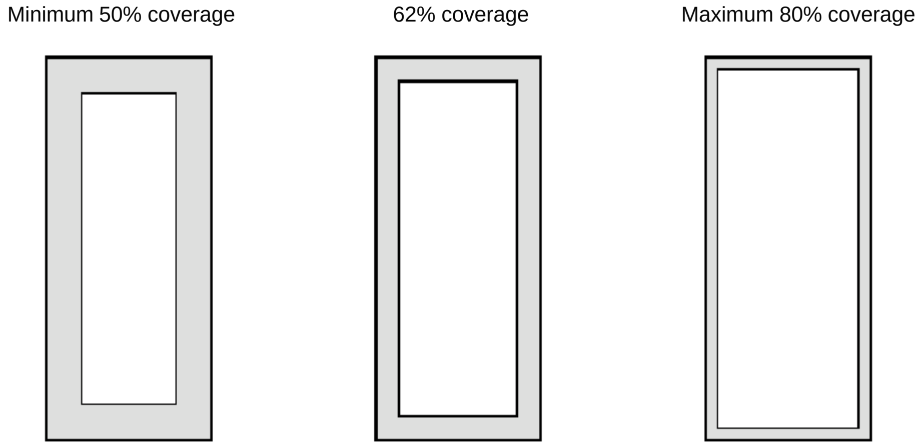


Figure 9. Solder Paste Application on Pins

Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. ON Semiconductor customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify ON Semiconductor for any damages resulting from such improper use or sale.

Device Information

The following device information can be queried using the AT−Commands AT$I=4, AT$I=5 for the APP version and AT$I=2, AT$I=3 for the chip version.

Table 13. DEVICE VERSIONS

Product	Part Number	APP Version		Chip Version	
		[0]	[1]	[0]	[1]
AX−SFEU	AX−SFEU−1−01−XXXX[1]	0x01	0x01	0x8F	0x51
AX−SFEU−API	AX−SFEU−API−1−01−XXXX[1]	0x01	0x01	0x8F	0x51

1. TB05 for Reel 500, TX30 for Reel 3000 reel

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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