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EFC2J004NUZ

Power MOSFET for 1-Cell Lithium-ion Battery Protection 12 V, 7.1 mΩ, 14 A, Dual N-Channel



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This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

Features

- 2.5 V Drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halogen Free and RoHS compliance

Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at $T_a = 25^\circ\text{C}$ (Notes 1, 2)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	± 8	V
Source Current (DC)	I_S	14	A
Source Current (Pulse) $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$	I_{SP}	60	A
Total Dissipation (Note 2)	P_T	1.5	W
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

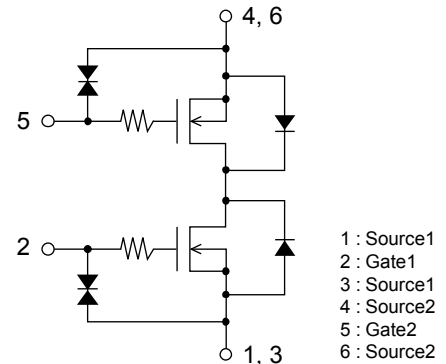
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 2)	$R_{\theta JA}$	83	$^\circ\text{C/W}$

Note 2 : Surface mounted on ceramic substrate ($5000\text{ mm}^2 \times 0.8\text{ mm}$).

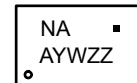
V_{SSS}	$R_{SS(on)}$ Max	I_S Max
12 V	7.1 mΩ @ 4.5 V	14 A
	7.7 mΩ @ 3.8 V	
	9.5 mΩ @ 3.1 V	
	12.4mΩ @ 2.5 V	

ELECTRICAL CONNECTION N-Channel



WLCSP6, 2.11x1.18x0.10

GENERIC MARKING DIAGRAM



NA = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot
▪ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS at Ta = 25°C (Notes 3, 4)

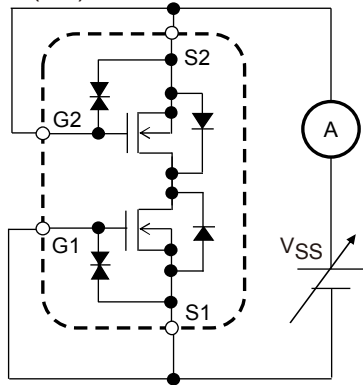
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Source to Source Breakdown Voltage	V(BR)SSS	IS = 1 mA, VGS = 0 V Test Circuit 1	12			V
Zero-Gate Voltage Source Current	ISSS	VSS = 10 V, VGS = 0 V Test Circuit 1			1	μA
Gate to Source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V Test Circuit 2			±1	μA
Gate Threshold Voltage	VGS(th)	VSS = 6 V, IS = 1 mA Test Circuit 3	0.4		1.3	V
Static Source to Source On-State Resistance (Note 4)	RSS(on)	IS = 5 A, VGS = 4.5 V Test Circuit 4	3.7	5.4	7.1	mΩ
		IS = 5 A, VGS = 3.8 V Test Circuit 4	4.1	5.9	7.7	mΩ
		IS = 5 A, VGS = 3.1 V Test Circuit 4	4.6	6.7	9.5	mΩ
		IS = 5 A, VGS = 2.5 V Test Circuit 4	5.8	8.4	12.4	mΩ
Turn-ON Delay Time	td(on)	VSS = 5 V, VGS = 3.8 V, IS = 5 A Rg = 10 kΩ Test Circuit 5		15		μs
Rise Time	tr			35		μs
Turn-OFF Delay Time	td(off)			100		μs
Fall Time	tf			75		μs
Total Gate Charge	Qg		VSS = 6 V, VGS = 4.5 V, IS = 14 A Test Circuit 6		36	
Forward Source to Source Voltage	VF(S-S)	IS = 3 A, VGS = 0 V Test Circuit 7		0.76		V

Note 3 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

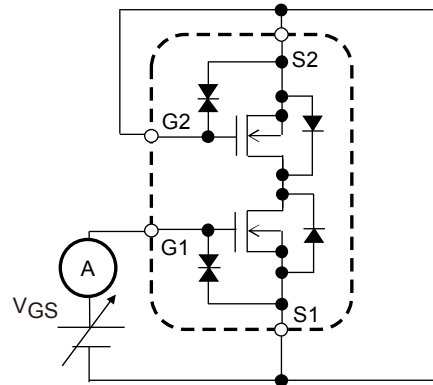
Note 4 : Mounted on ON Semiconductor board.

Test circuits are example of measuring FET1 side

Test Circuit 1
 $V_{(BR)SSS} / I_{SSS}$

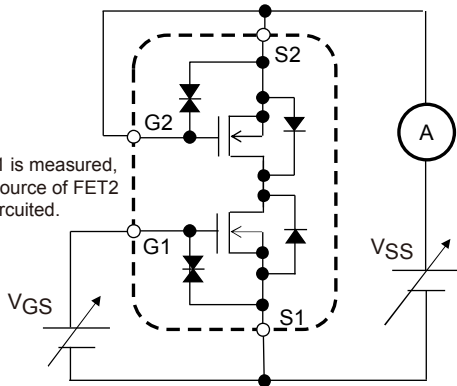


Test Circuit 2
 I_{GSS}



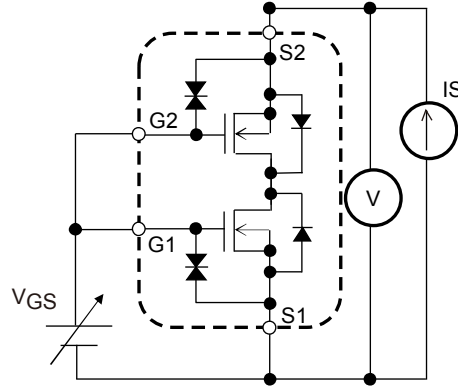
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
 $V_{GS(th)}$

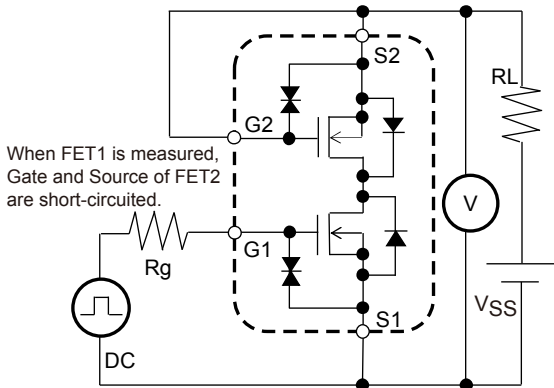


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
 $R_{SS(on)}$

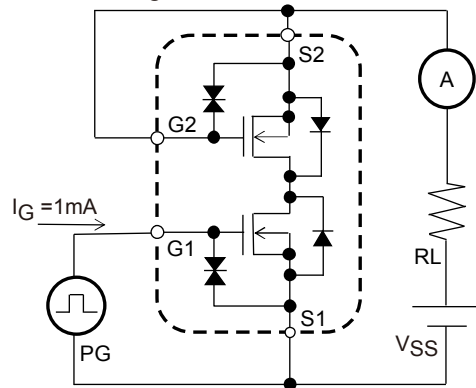


Test Circuit 5
 $t_d(on), t_r, t_d(off), t_f$



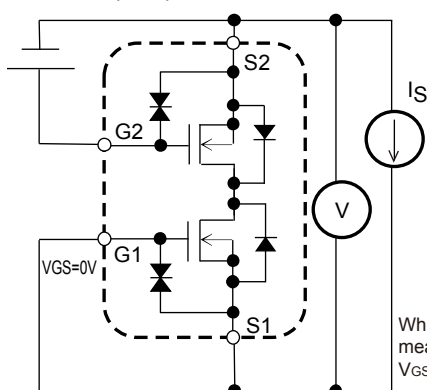
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 6
 Q_g



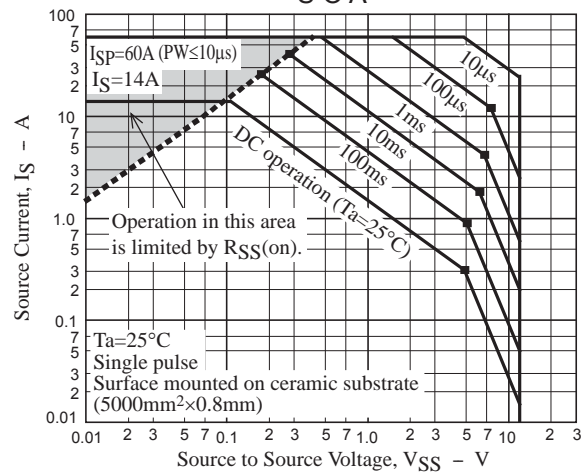
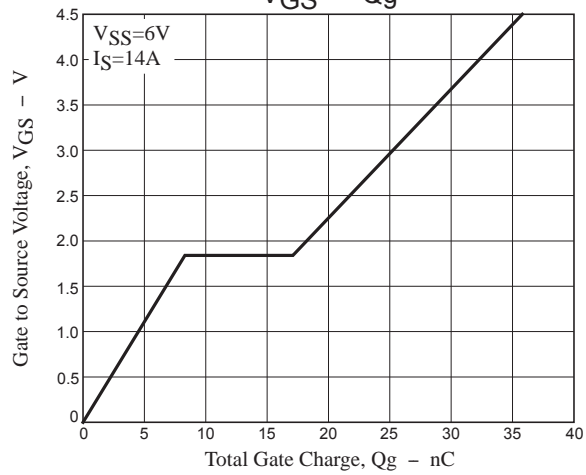
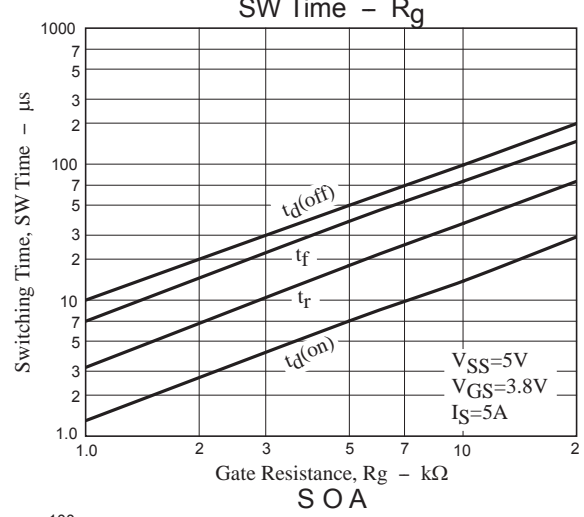
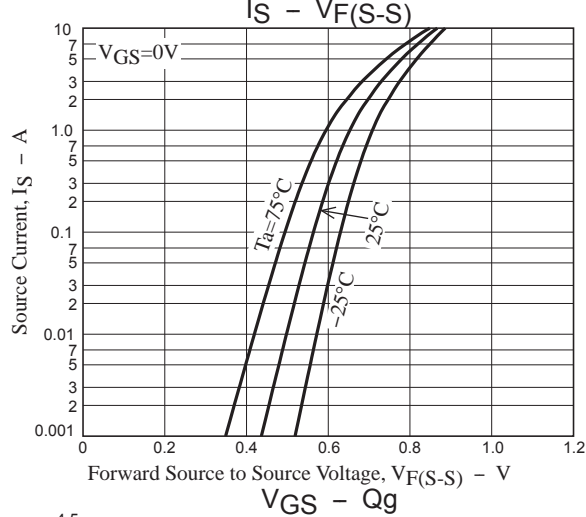
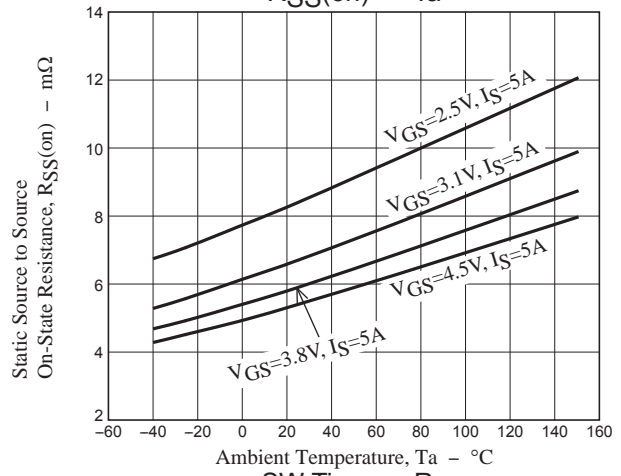
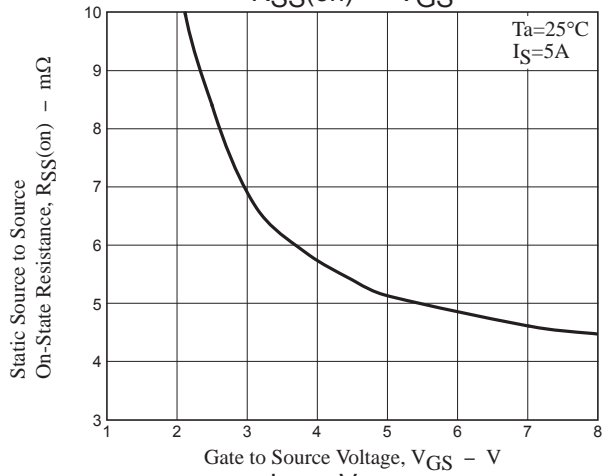
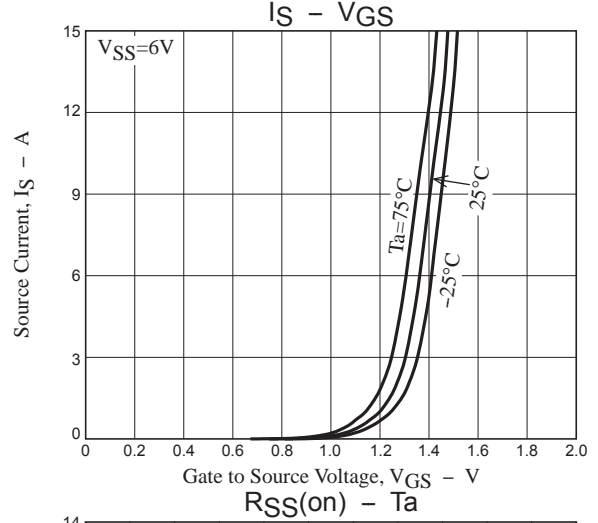
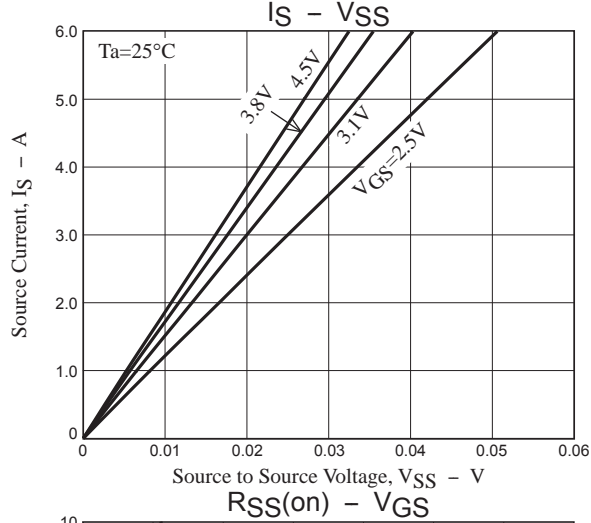
When FET1 is measured, Gate and Source of FET2 are short-circuited.

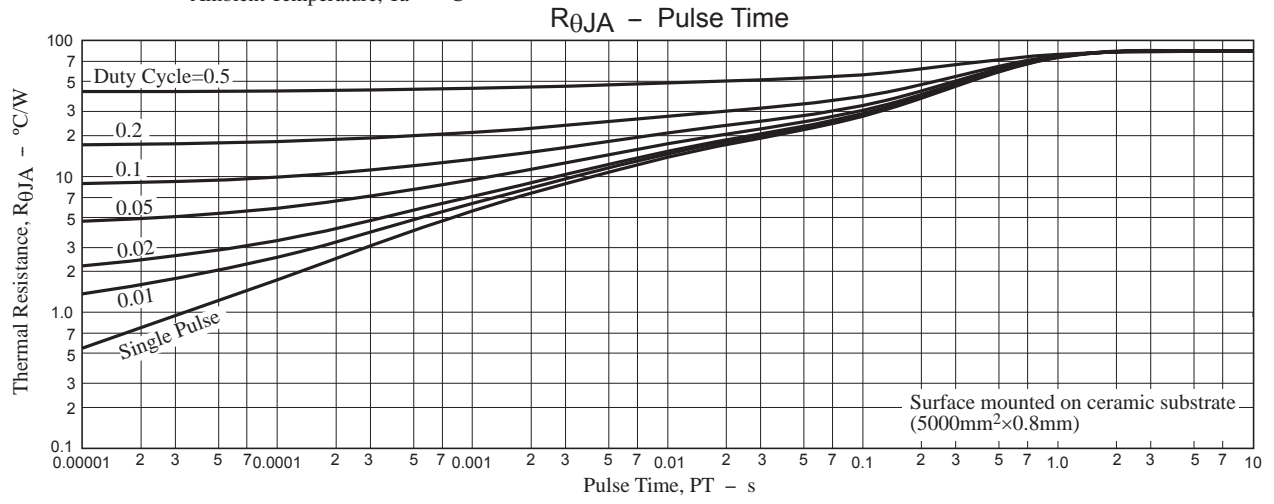
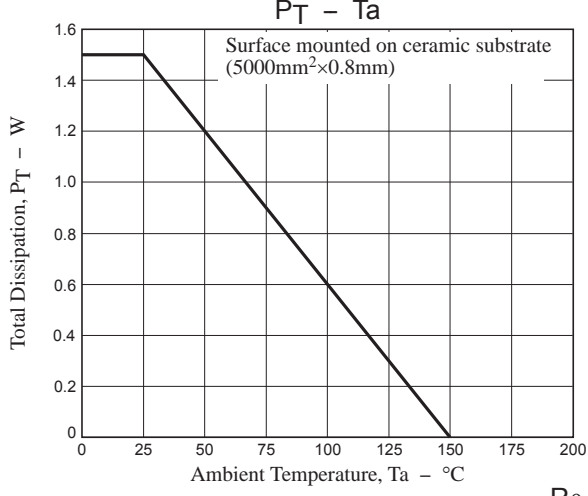
Test Circuit 7
 $V_F(S-S)$



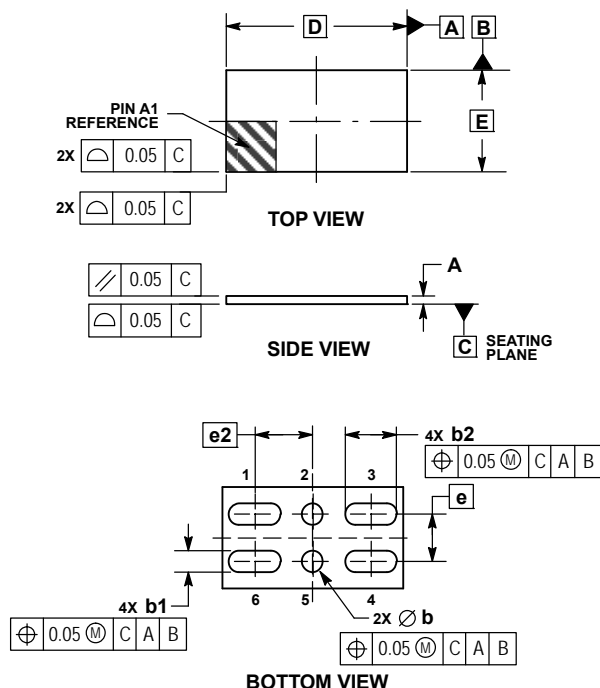
When FET1 is measured, +4.5V is added to V_{GS} of FET2.

When FET2 is measured, the position of FET1 and FET2 is switched.





WLCSP6, 2.11x1.18x0.10
CASE 567NP
ISSUE B

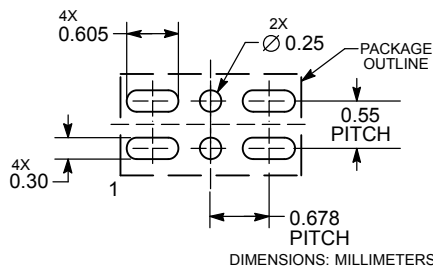


- 1 : Source1
- 2 : Gate1
- 3 : Source1
- 4 : Source2
- 5 : Gate2
- 6 : Source2

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.08	0.10	0.12
b	0.22	0.25	0.28
b1	0.27	0.30	0.33
b2	0.575	0.605	0.635
D	2.11 BSC		
E	1.18 BSC		
e	0.55 BSC		
e2	0.6775 BSC		

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)
EFC2J004NUZTDG	NA	WLCSP6, 2.11x1.18x0.10 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the EFC2J004NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

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[MIC4420CM-TR](#) [VN1206L](#) [SBVS138LT1G](#) [614234A](#) [715780A](#) [NTNS3166NZT5G](#) [SSM6J414TU,LF\(T](#) [751625C](#) [BUK954R8-60E](#)
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