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# EFC3J018NUZ

## Power MOSFET for 1-2 Cells Lithium-ion Battery Protection 20 V, 4.7 mΩ, 23 A, Dual N-Channel



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This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-2 cells lithium-ion battery applications.

### Features

- 2.5 V drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- Pb-Free, Halogen Free and RoHS compliance

### Applications

- 1-2 Cells Lithium-ion Battery Charging and Discharging Switch

### SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS** at Ta = 25°C (Note 1)

| Parameter  | Symbol               | Value       | Unit |
|--|----------------------|-------------|------|
| Source to Source Voltage                               | V <sub>SSS</sub>     | 20          | V    |
| Gate to Source Voltage                                 | V <sub>GSS</sub>     | ±12         | V    |
| Maximum Operating Gate to Source Voltage (Note 2)      | V <sub>GSS(OP)</sub> | ±8          | V    |
| Source Current (DC)                                    | I <sub>S</sub>       | 23          | A    |
| Source Current (Pulse)<br>PW ≤ 100 μs, duty cycle ≤ 1% | I <sub>SP</sub>      | 100         | A    |
| Total Dissipation (Note 3)                             | P <sub>T</sub>       | 2.5         | W    |
| Junction Temperature                                   | T <sub>j</sub>       | 150         | °C   |
| Storage Temperature                                    | T <sub>stg</sub>     | -55 to +150 | °C   |

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note 2 : Functional operation above the stresses listed in the recommended operating ranges is not implied. Extended exposure to stresses beyond the recommended operating ranges limits may affect device reliability

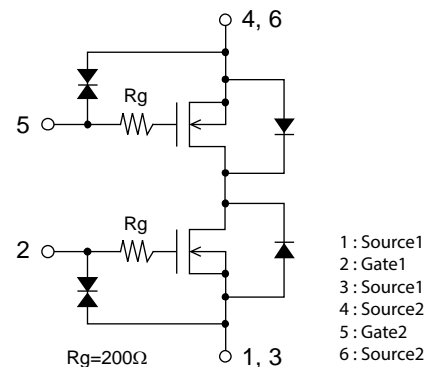
### THERMAL RESISTANCE RATINGS

| Parameter                    | Symbol           | Value | Unit |
|------------------------------|------------------|-------|------|
| Junction to Ambient (Note 3) | R <sub>θJA</sub> | 50    | °C/W |

Note 3 : Surface mounted on ceramic substrate (5000 mm<sup>2</sup> × 0.8 mm).

| V <sub>SSS</sub> | R <sub>SS(on)</sub> Max | I <sub>S</sub> Max |
|------------------|-------------------------|--------------------|
| 20 V             | 4.7 mΩ @ 4.5 V          | 23 A               |
|                  | 4.75 mΩ @ 4.0 V         |                    |
|                  | 4.9 mΩ @ 3.8 V          |                    |
|                  | 5.4 mΩ @ 3.1 V          |                    |
|                  | 9.0 mΩ @ 2.5 V          |                    |

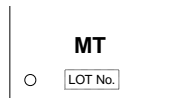
### ELECTRICAL CONNECTION N-Channel



### MARKING



WLCSP6, 1.77x3.05



MT = Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

**ELECTRICAL CHARACTERISTICS at Ta = 25°C (Notes 4, 5)**

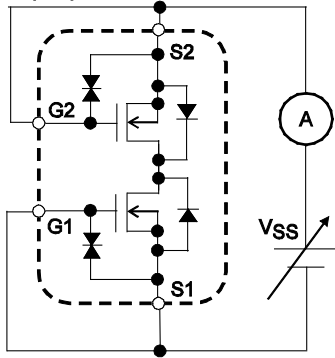
| Parameter                                   | Symbol   | Conditions   | Value |       |      | Unit |
|---|----------|--|-------|-------|------|------|
|   |          |  | min   | typ   | max  |      |
| Source to Source Breakdown Voltage          | V(BR)SSS | IS = 1 mA, VGS = 0 V Test Circuit 1                  | 20    |       |      | V    |
| Zero-Gate Voltage Source Current            | ISSS     | VSS = 20 V, VGS = 0 V Test Circuit 1                 |       |       | 1    | μA   |
| Gate to Source Leakage Current              | IGSS     | VGS = ±8 V, VSS = 0 V Test Circuit 2                 |       |       | ±1   | μA   |
| Gate Threshold Voltage                      | VGS(th)  | VSS = 10 V, IS = 1 mA Test Circuit 3                 | 0.5   |       | 1.3  | V    |
| Static Source to Source On-State Resistance | RSS(on)  | IS = 5 A, VGS = 4.5 V Test Circuit 4                 | 2.5   | 3.6   | 4.7  | mΩ   |
|   |          | IS = 5 A, VGS = 4.0 V Test Circuit 4                 | 2.56  | 3.65  | 4.75 | mΩ   |
|   |          | IS = 5 A, VGS = 3.8 V Test Circuit 4                 | 2.6   | 3.75  | 4.9  | mΩ   |
|   |          | IS = 5 A, VGS = 3.1 V Test Circuit 4                 | 2.9   | 4.15  | 5.4  | mΩ   |
|   |          | IS = 5 A, VGS = 2.5 V Test Circuit 4                 | 3.3   | 4.75  | 9.0  | mΩ   |
| Turn-ON Delay Time                          | td(on)   | VSS = 10 V, VGS = 4.5 V, IS = 3 A<br>Test Circuit 5  |       | 280   |      | ns   |
| Rise Time                                   | tr       |  |       | 890   |      | ns   |
| Turn-OFF Delay Time                         | td(off)  |  |       | 4,100 |      | ns   |
| Fall Time                                   | tf       |  |       | 2,800 |      | ns   |
| Total Gate Charge                           | Qg       | VSS = 10 V, VGS = 4.5 V, IS = 23 A<br>Test Circuit 6 |       | 75    |      | nC   |
| Forward Source to Source Voltage            | VF(S-S)  | IS = 3 A, VGS = 0 V Test Circuit 7                   |       | 0.74  | 1.2  | V    |

Note 4 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted.  
Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

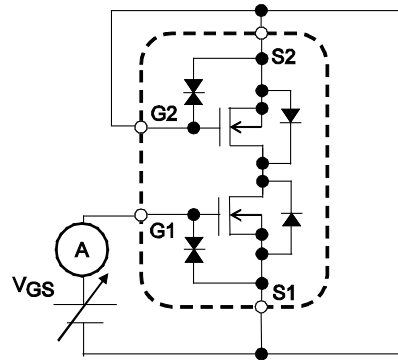
Note 5 : Refer to the JIS 7030 measuring methods for transistors for measuring.

Test circuits are example of measuring FET1 side

**Test Circuit 1**  
 $V_{(BR)SSS} / I_{SSS}$

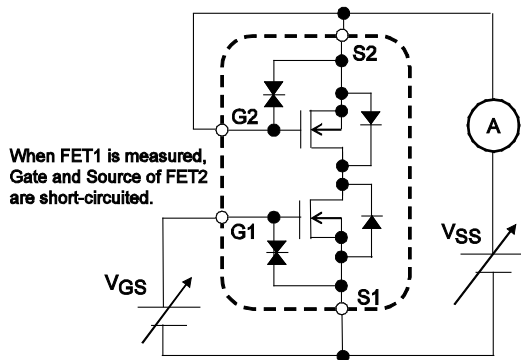


**Test Circuit 2**  
 $I_{GSS}$



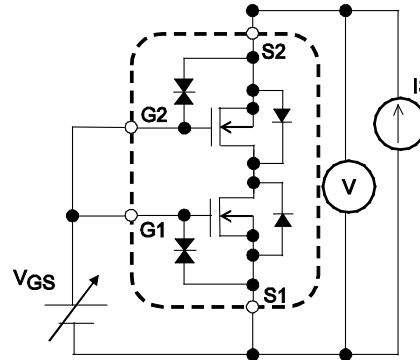
When FET1 is measured, Gate and Source of FET2 are short-circuited.

**Test Circuit 3**  
 $V_{GS(th)}$

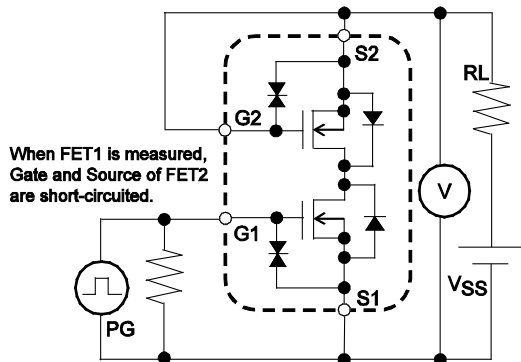


When FET1 is measured, Gate and Source of FET2 are short-circuited.

**Test Circuit 4**  
 $R_{SS(on)}$

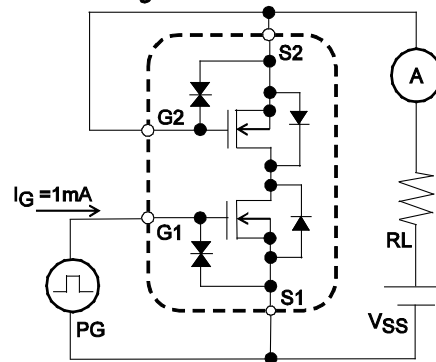


**Test Circuit 5**  
 $t_{d(on)}, t_r, t_{d(off)}, t_f$



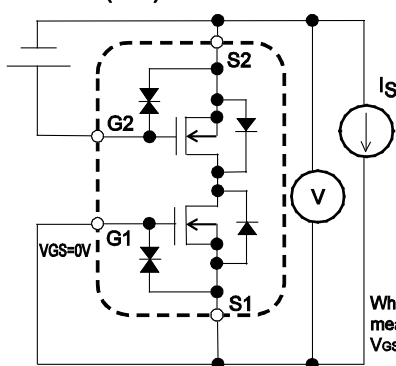
When FET1 is measured, Gate and Source of FET2 are short-circuited.

**Test Circuit 6**  
 $Q_g$



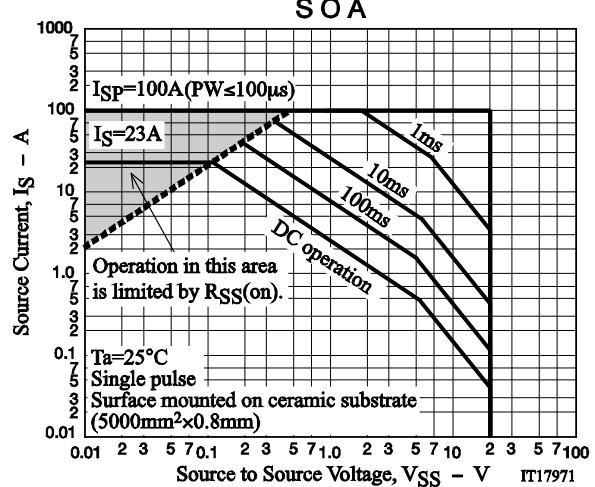
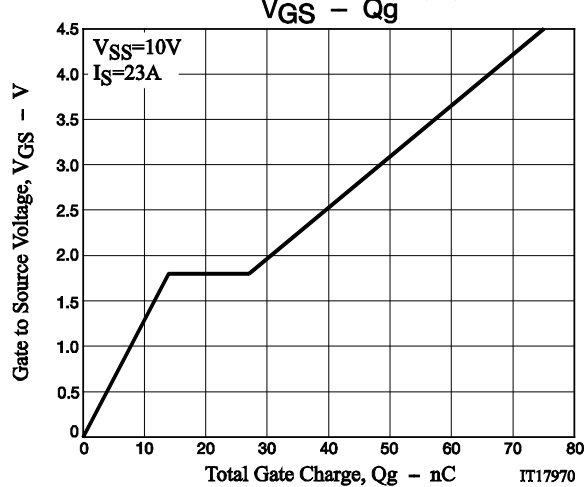
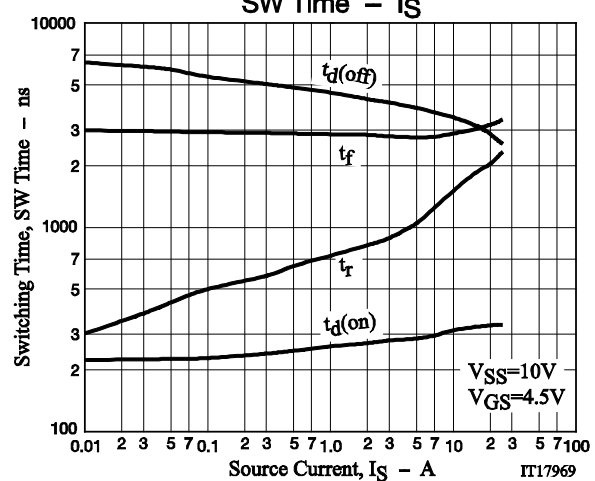
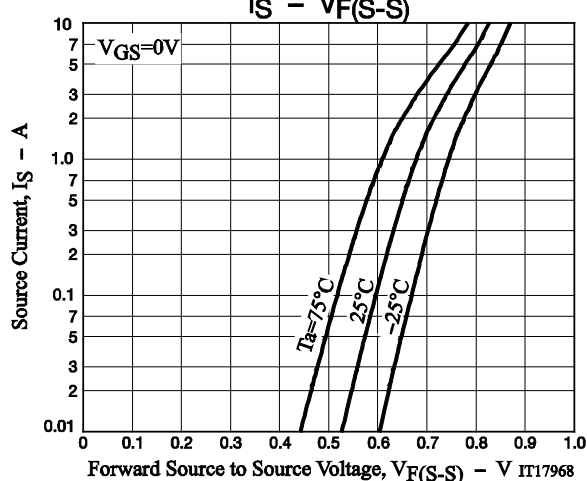
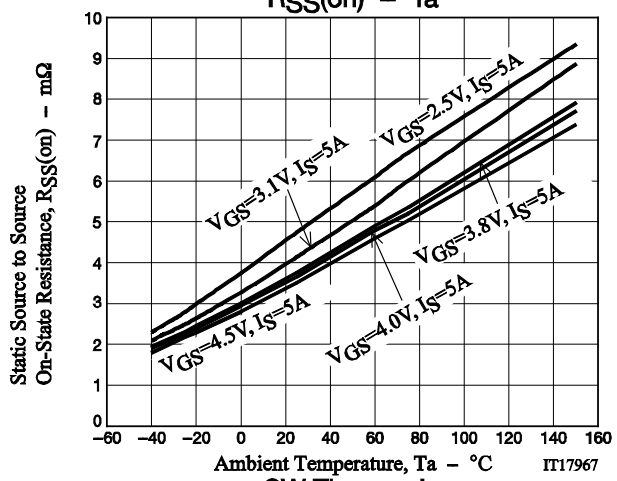
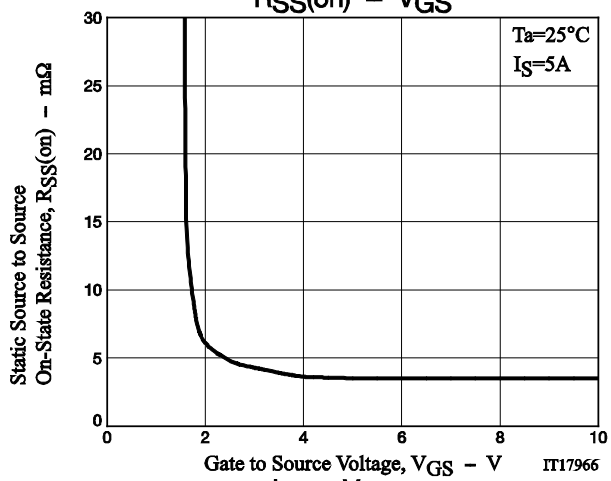
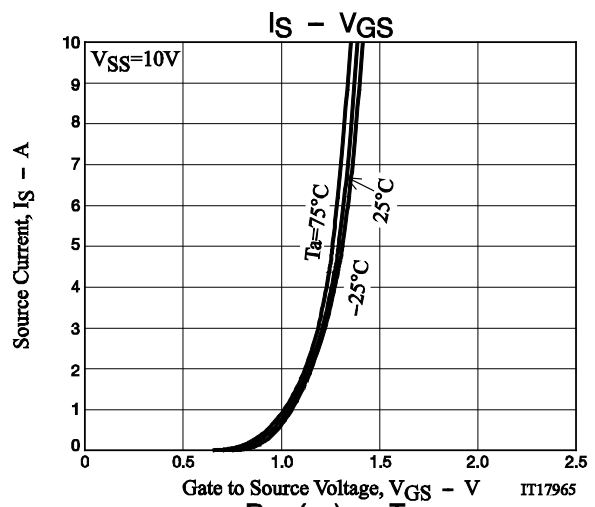
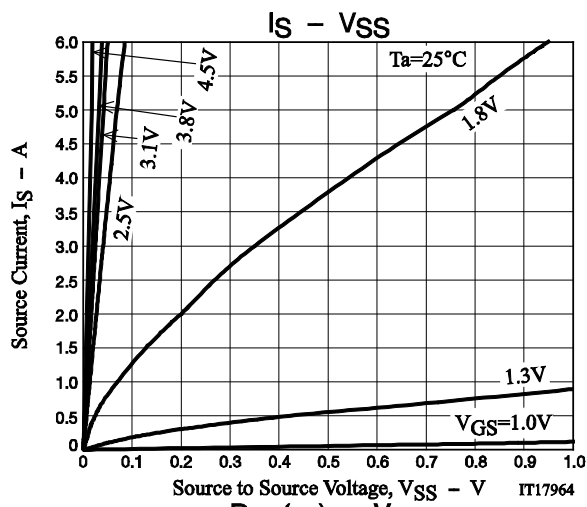
When FET1 is measured, Gate and Source of FET2 are short-circuited.

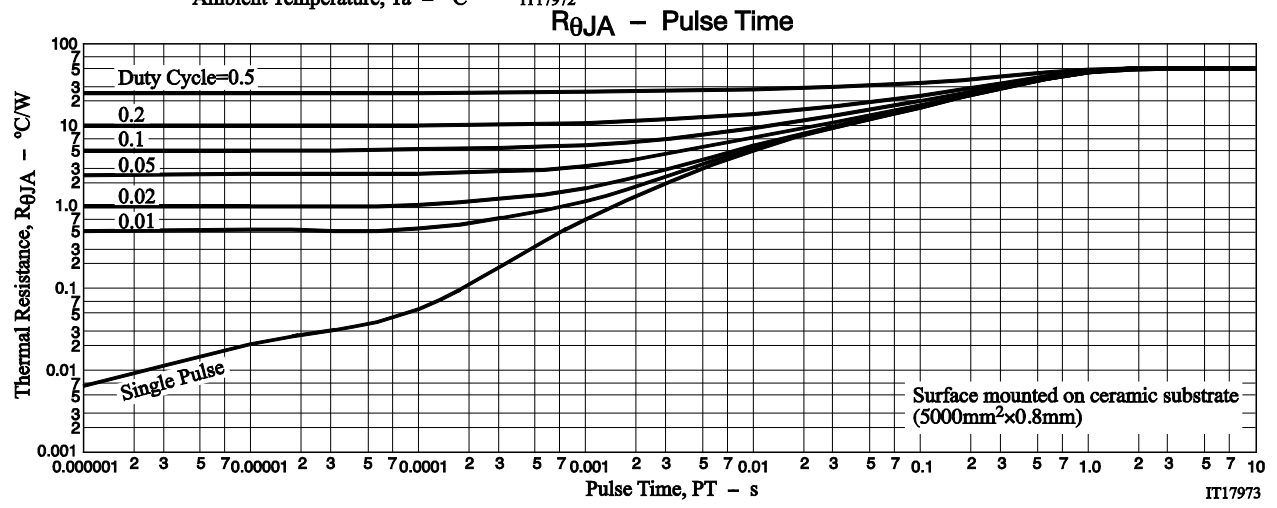
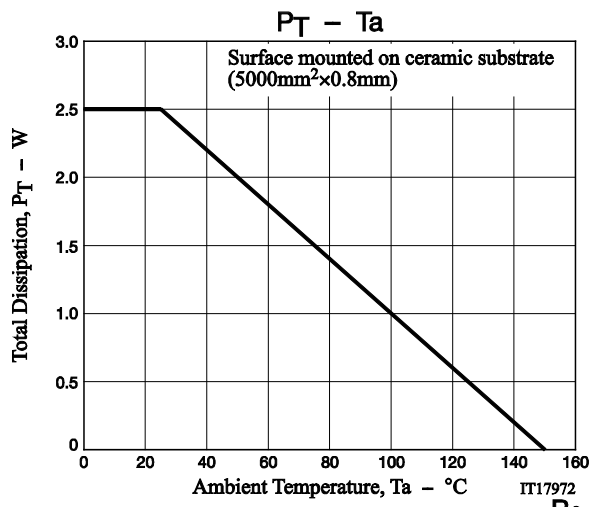
**Test Circuit 7**  
 $V_{F(S-S)}$



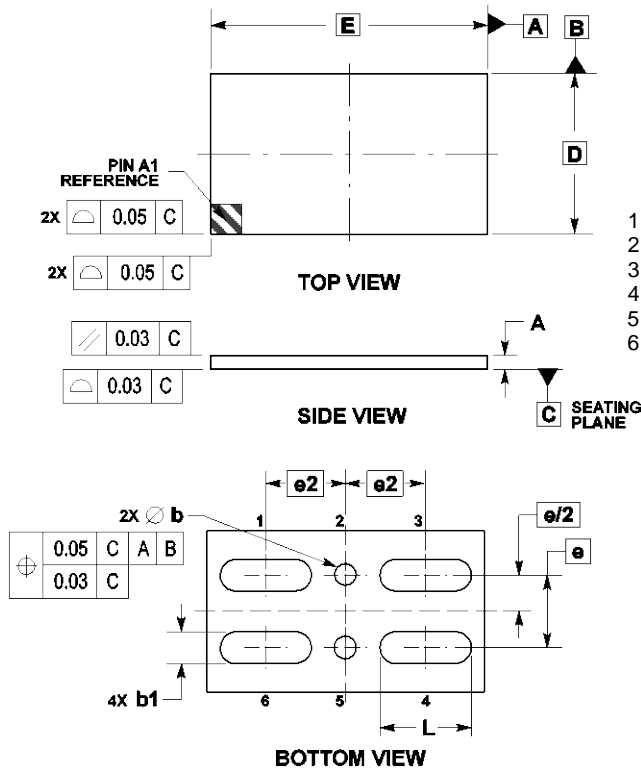
When FET1 is measured, +4.5V is added to  $V_{GS}$  of FET2.

When FET2 is measured, the position of FET1 and FET2 is switched.





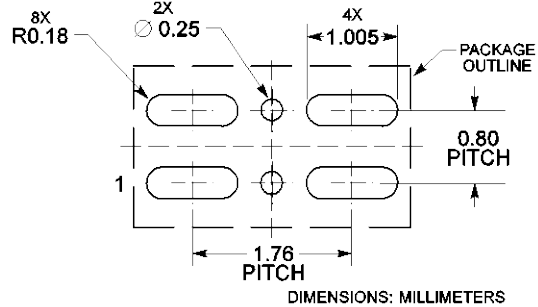
**WLCSP6, 1.77x3.05**  
**CASE 567KS**  
**ISSUE 0**



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.  
2. CONTROLLING DIMENSION: MILLIMETERS.

| MILLIMETERS |            |       |
|-------------|------------|-------|
| DIM         | MIN        | MAX   |
| A           | ---        | 0.145 |
| b           | 0.22       | 0.28  |
| b1          | 0.32       | 0.38  |
| D           | 1.77 BSC   |       |
| E           | 3.05 BSC   |       |
| e           | 0.80 BSC   |       |
| e2          | 0.8775 BSC |       |
| L           | 0.975      | 1.035 |

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ORDERING INFORMATION**

| Device         | Marking | Package   | Shipping (Qty / Packing) |
|----------------|---------|---|--------------------------|
| EFC3J018NUZTDG | MT      | WLCSP6, 1.77 × 3.05<br>(Pb-Free / Halogen Free) | 5,000 / Tape & Reel      |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. [http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

Note on usage : Since the EFC3J018NUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

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