

EFC4C002NL

Power MOSFET for 3-Cells Lithium-ion Battery Protection 30V, 2.6mΩ, 30A, Dual N-Channel, WLCSP8



ON Semiconductor®

www.onsemi.com

This N-Channel Power MOSFET is produced using ON Semiconductor's trench technology, which is specifically designed to minimize gate charge and ultra low on resistance.

This device is suitable for applications of DRONE or NOTEBOOK PC.

Features

- Ultra Low On-Resistance
- Low Gate Charge
- Common-Drain type
- Pb-Free, Halogen Free and RoHS compliance

Applications

- 3-Cells Lithium-ion Battery Charging and Discharging Switch

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS at Ta = 25°C (Note 1, 2)

Parameter	Symbol	Value	Unit
Source to Source Voltage	VSSS	30	V
Gate to Source Voltage	VGSS	±20	V
Source Current (DC)	IS	30	A
Source Current (Pulse) PW≤10μs, duty cycle≤1%	ISP	120	A
Total Dissipation (Note 2)	PT	2.6	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

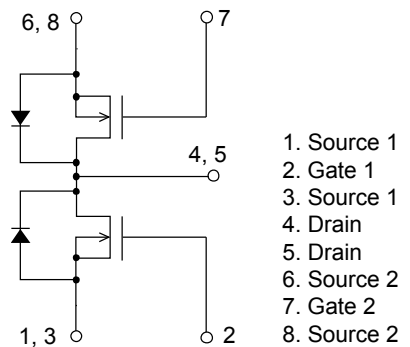
THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction to Ambient (Note 2)	RθJA	48	°C/W

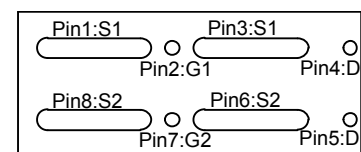
Note 2 : Surface mounted on ceramic substrate(5000mm² × 0.8mm).

VSSS	RSS(on) Max	IS Max
30V	2.6mΩ@ 10V	30A
	3.3mΩ@ 8V	
	5.1mΩ@ 4.5V	

ELECTRICAL CONNECTION N-Channel

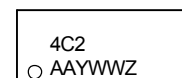


PIN ASSIGNMENT



BOTTOM VIEW

MARKING DIAGRAM



4C2 = Specific Device Code
AA = Assembly Location
Y = Year
WW = Work Week
Z = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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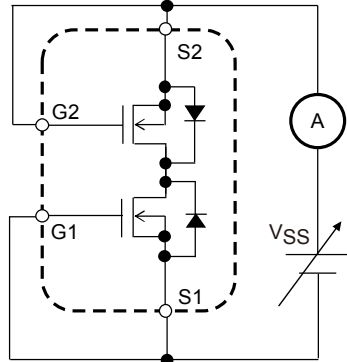
ELECTRICAL CHARACTERISTICS at Ta = 25°C (Note 3)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Source to Source Breakdown Voltage	V(BR)SSS	IS=1mA, VGS=0V Test Circuit 1	30			V
Zero-Gate Voltage Source Current	ISSS	VSS=24V, VGS=0V Test Circuit 1			1	μA
Gate to Source Leakage Current	IGSS	VGS=20V, VSS=0V Test Circuit 2			200	nA
Gate Threshold Voltage	VGS(th)	VSS=10V, IS=1mA Test Circuit 3	1.3		2.2	V
Forward Transconductance	gFS	VSS=10V, IS=10A Test Circuit 4		16		S
Static Source to Source On-State Resistance	RSS(on)	VGS=10V, IS=10A Test Circuit 5	1.5	2.0	2.6	mΩ
		VGS=8V, IS=10A Test Circuit 5	1.6	2.1	3.3	mΩ
		VGS=4.5V, IS=10A Test Circuit 5	2.2	2.9	5.1	mΩ
Static Drain to Source On-State Resistance	RDS(on)	VGS=10V, IS=1A		10		mΩ
Gate Resistance	RG			3		Ω
Turn-ON Delay Time	t _{d(on)}	VSS=15V, VGS=10V, IS=10A Test Circuit 6		40		ns
Rise Time	t _r			750		ns
Turn-OFF Delay Time	t _{d(off)}			280		ns
Fall Time	t _f			105		ns
Input Capacitance	Ciss		VSS=15V, VGS=0V, f=1MHz		6,200	
Total Gate Charge	Qg	VSS=15V, VGS=4.5V, IS=15A Test Circuit 7		45		nC
Forward Source to Source Voltage	VF(S-S)	IS=10A, VGS=0V Test Circuit 8		0.75	1.2	V

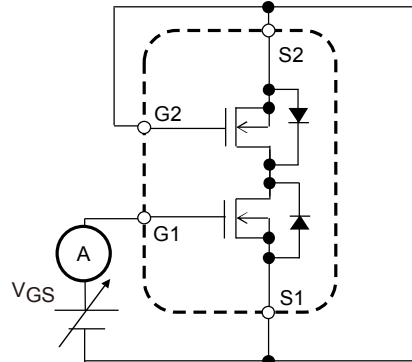
Note 3 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test circuits are example of measuring FET1 side

Test Circuit 1
V_{SSS} / I_{SSS}

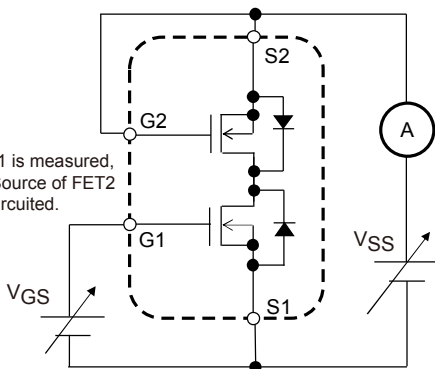


Test Circuit 2
I_{GSS}



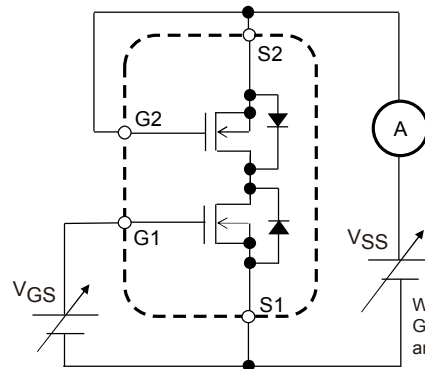
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
V_{GS(th)}



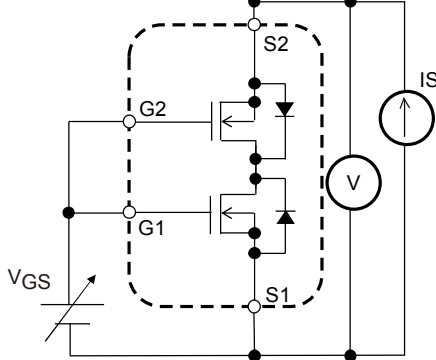
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
g_{FS}

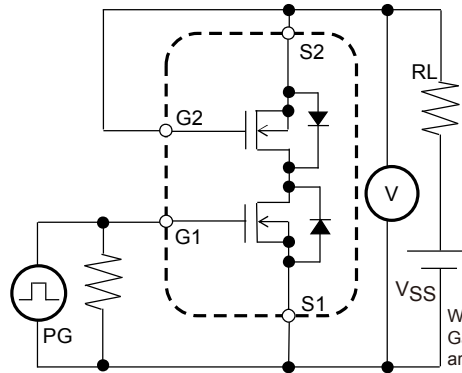


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
R_{SS(on)}

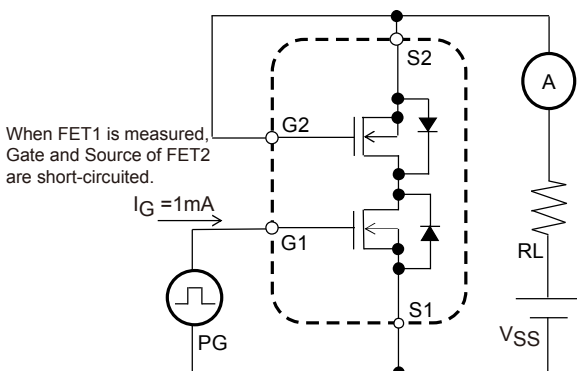


Test Circuit 6
t_{d(on)}, t_r, t_{d(off)}, t_f



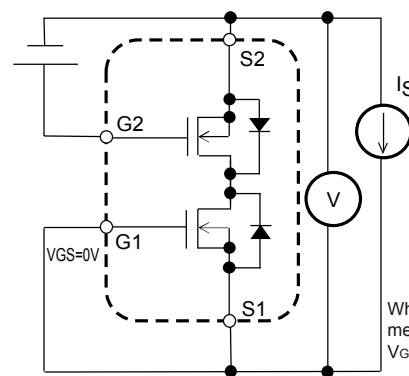
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 7
Q_g



When FET1 is measured, Gate and Source of FET2 are short-circuited.

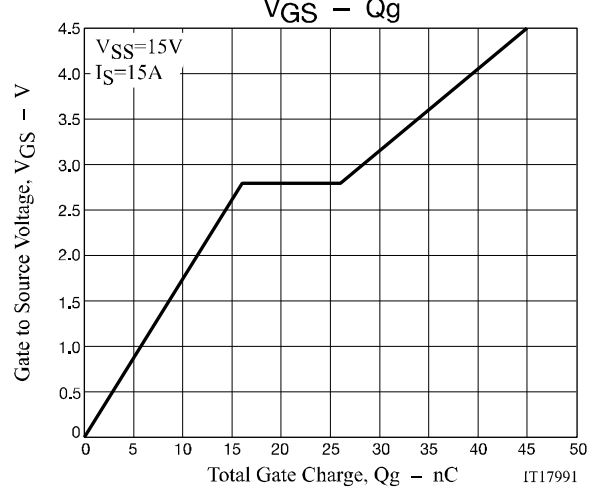
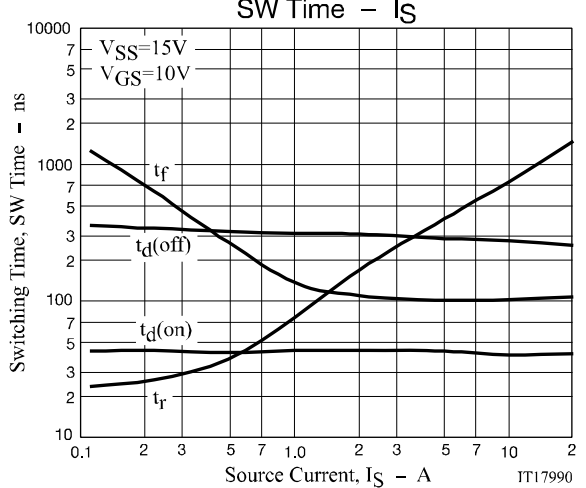
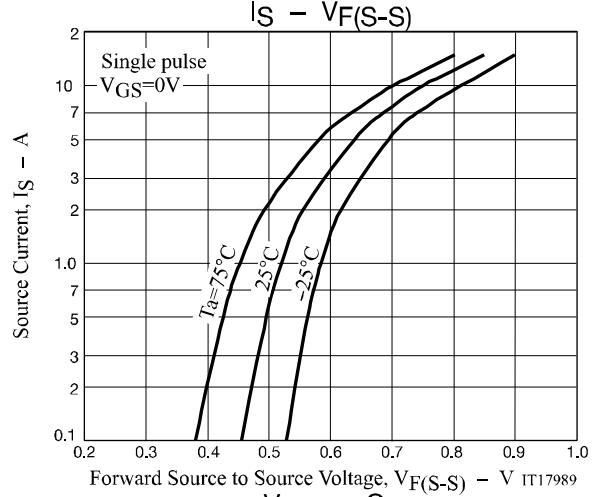
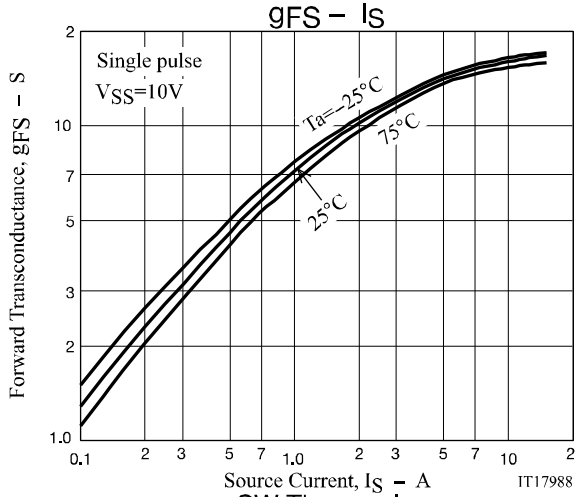
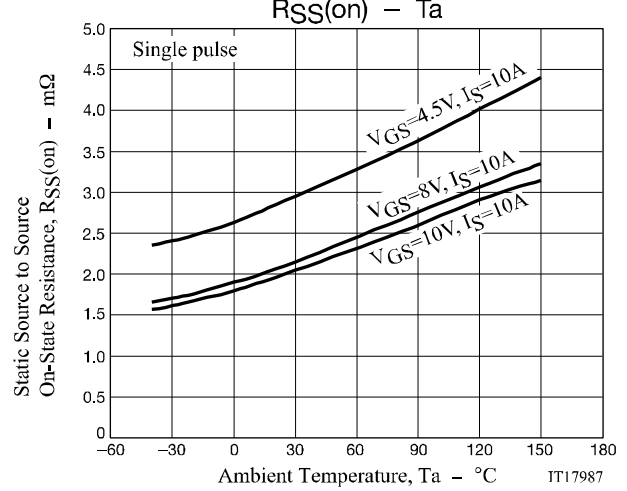
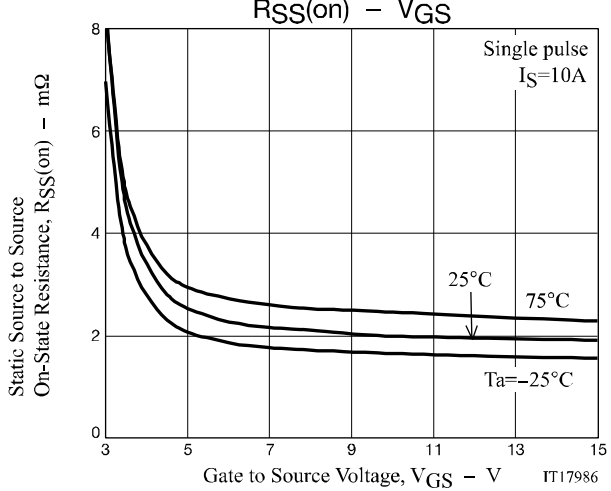
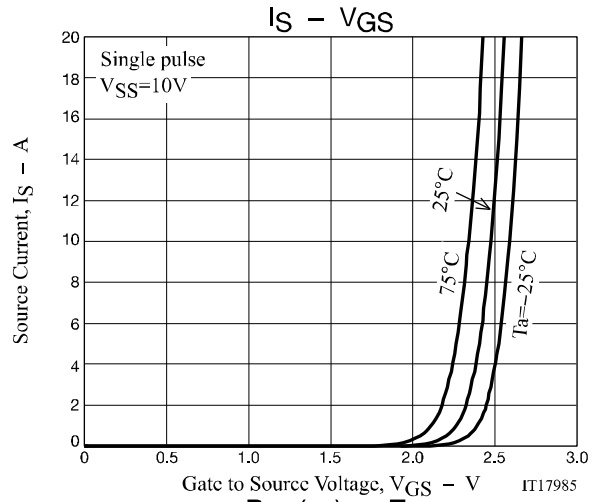
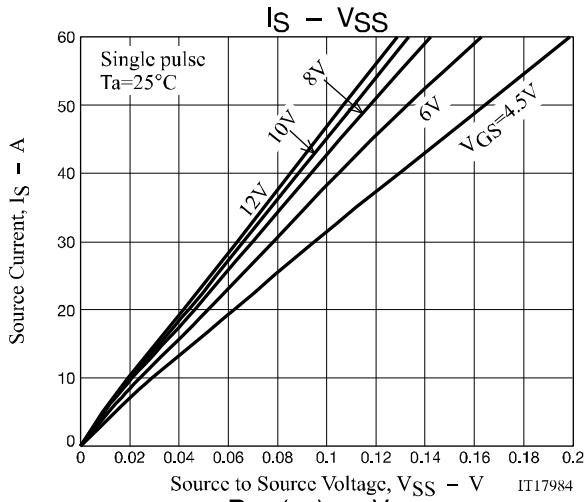
Test Circuit 8
V_{F(S-S)}



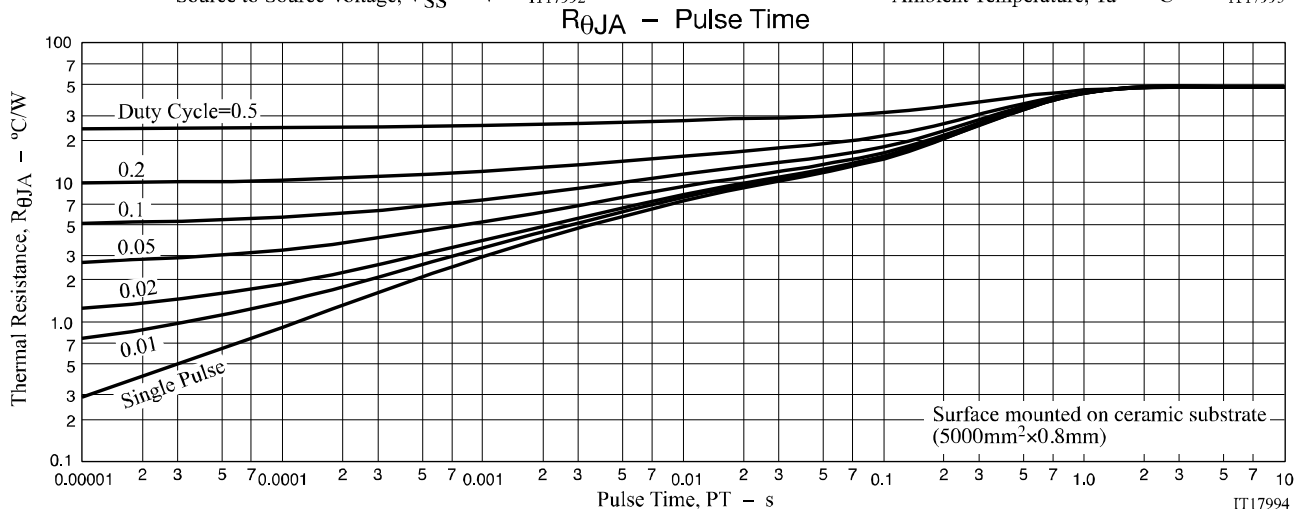
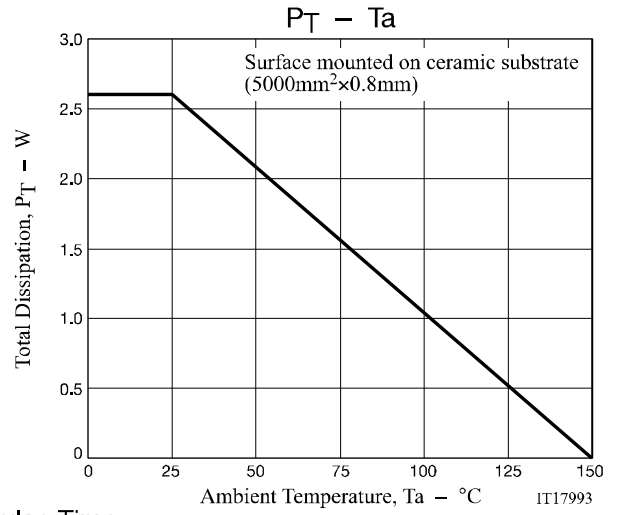
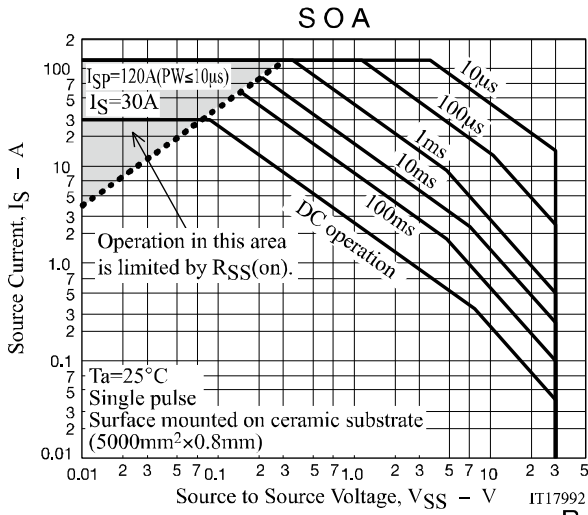
When FET1 is measured, +10V is added to V_{GS} of FET2.

When FET2 is measured, the position of FET1 and FET2 is switched.

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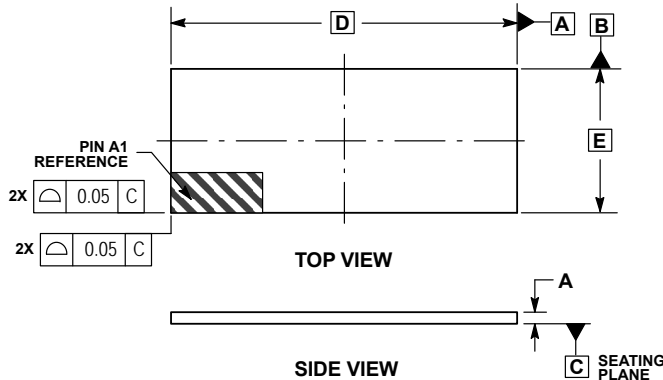
PACKAGE DIMENSIONS

unit : mm

WLCSP8, 6.00x2.50 / EFCP6025-8EGJ-021

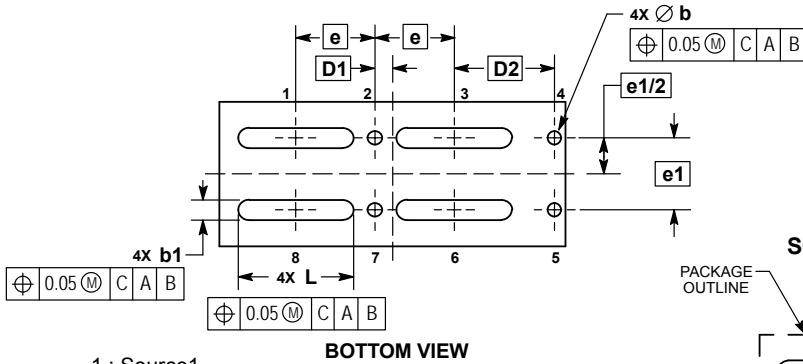
CASE 567MC

ISSUE O



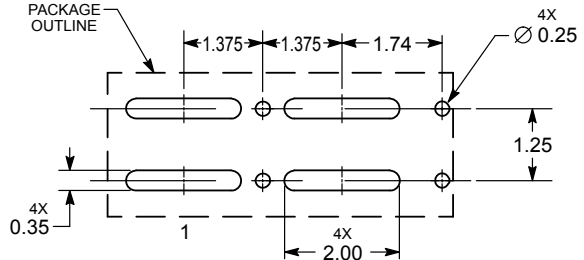
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.19	0.23
b	0.22	0.28
b1	0.32	0.38
D	5.95	6.05
D1	0.305 BSC	
D2	1.740 BSC	
E	2.45	2.55
e	1.375 BSC	
e1	1.25 BSC	
L	1.97	2.03



- 1 : Source1
- 2 : Gate1
- 3 : Source1
- 4 : Drain
- 5 : Drain
- 6 : Source2
- 7 : Gate2
- 8 : Source2

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)
EFC4C002NLTDG	4C2	WLCSP8, 6.00 x 2.50 EFCP6025-8EGJ-021 (Pb-Free / Halogen Free)	5,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

Note on usage : Since the EFC4C002NL is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

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[MH](#) [SS30-TE-L-E](#) [STK531-345A-E](#) [STK581U3A0D-E](#) [STK58AUNP0D-E](#) [STK621-068C-E](#) [STK621-140C](#) [STK621-728S-E](#) [STK625-728-](#)
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