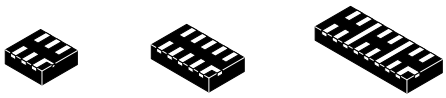
EMI8141, EMI8142, EMI8143

Common Mode Filter with ESD Protection

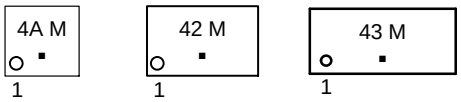
ON Semiconductor®

http://onsemi.com



XDFN6 CASE 711AV | XDFN10 CASE 711AU | XDFN16 CASE 711AW

MARKING DIAGRAMS



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

Functional Description

The EMI814x is a family of Common Mode Filters (CMF) with integrated ESD protection, a first in the industry. Differential signaling I/Os can now have both common mode filtering and ESD protection in one package. The EMI814x protects against ESD pulses up to ±15 kV contact per the IEC61000−4−2 standard.

The EMI814x is well−suited for protecting systems using high−speed differential ports such as USB 3.0, MIPI D−PHY; corresponding ports in removable storage, and other applications where ESD protection are required in a small footprint package.

The EMI814x is available in a RoHS−compliant, XDFN6 for 1 Differential Pair, XDFN−10 for 2 Differential Pair and XDFN−16 package for 3 Differential Pair.

Features

- Total Insertion Loss DM_{LOSS} < 2.5 dB at 2.5 GHz
- Large Differential Mode Cutoff Frequency f_{3dB} > 5 GHz
- High Common Mode Stop Band Attenuation: > 10 dB at 500 MHz , 15 dB at 700 MHz
- Low Channel Resistance 6.0 Ω
- Provides ESD Protection to IEC61000−4−2 Level 4, ±15 kV Contact
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- USB 3.0
- MHL 2.0
- μSD Card
- eSATA
- HDMI/DVI Display in Mobile Phones
- MIPI D−PHY (CSI−2, DSI, etc) in Mobile Phones and Digital Still Cameras

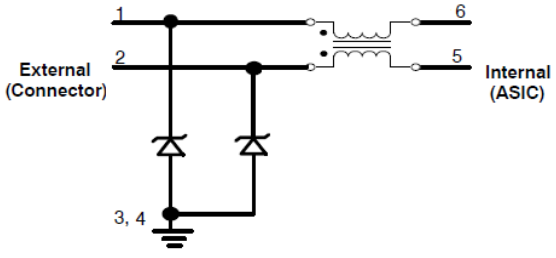
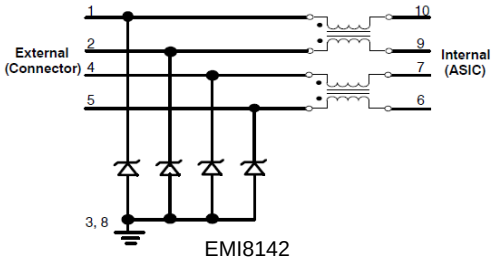
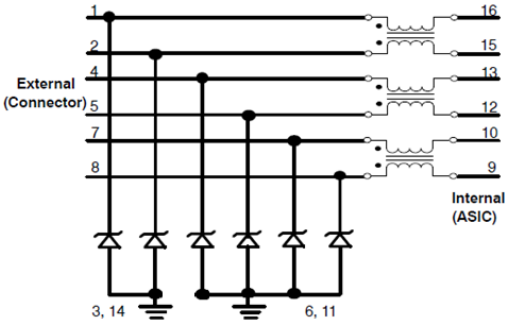


Figure 1. EMI8141 Electrical Schematic

ELECTRICAL SCHEMATICS



EMI8142



EMI8143

ORDERING INFORMATION

Device	Package	Shipping†
EMI8141MUTAG	XDFN6	3000 / Tape & Reel
EMI8142MUTAG	XDFN10	3000 / Tape & Reel
EMI8143MUTAG	XDFN16	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin Name	Device Pin			Type	Description
	EMI8141	EMI8142	EMI8143		
In_1+	1	1	1	I/O	CMF Channel 1+ to Connector (External)
In_1−	2	2	2	I/O	CMF Channel 1− to Connector (External)
Out_1+	6	10	16	I/O	CMF Channel 1+ to ASIC (Internal)
Out_1−	5	9	15	I/O	CMF Channel 1− to ASIC (Internal)
In_2+	NA	4	4	I/O	CMF Channel 2+ to Connector (External)
In_2−	NA	5	5	I/O	CMF Channel 2− to Connector (External)
Out_2+	NA	7	13	I/O	CMF Channel 2+ to ASIC (Internal)
Out_2−	NA	6	12	I/O	CMF Channel 2− to ASIC (Internal)
In_3+	NA	NA	7	I/O	CMF Channel 3+ to Connector (External)
In_3−	NA	NA	8	I/O	CMF Channel 3− to Connector (External)
Out_3+	NA	NA	10	I/O	CMF Channel 3+ to ASIC (Internal)
Out_3−	NA	NA	9	I/O	CMF Channel 3− to ASIC (Internal)
V_N	3,4	3, 8	3,6,14,11	GND	Ground

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Operating Temperature Range	T_{OP}	−40 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Lead Temperature for Soldering Purposes (1/8” from Case for 10 seconds)	T_L	260	°C
DC Current per Line	I_{LINE}	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 3)		3.3		V
V_{BR}	Breakdown Voltage	I_T = 1 mA; (Note 4)	4.0		9.0	V
I_{LEAK}	Channel Leakage Current	T_A = 25°C, V_{IN} = 3.3 V, GND = 0 V			1.0	μA
R_{CH}	Channel Resistance (Pins 1−6, 2−5) − EMI8141 (Pins 1−10, 2−9, 4−7 and 5−6) − EMI8142 (Pins 1−16, 2−15, 4−13, 5−12, 7−10 and 8−9) − EMI8143			6.0		Ω
DM_{LOSS}	Differential Mode Insertion Loss	@ 2.5 GHz		2.5		dB
f_{3dB}	Differential Mode Cut-off Frequency	50 Ω Source and Load Termination		5.0		GHz
F_{atten}	Common Mode Stop Band Attenuation	@ 700 MHz		15		dB
V_{ESD}	In-system ESD Withstand Voltage a) Contact discharge per IEC 61000-4-2 standard, Level 4 **(External Pins)** b) Contact discharge per IEC 61000-4-2 standard, Level 1 **(Internal Pins)**	(Notes 1 and 2)	 ±15 ±2			kV
V_{CL}	TLP Clamping Voltage	Forward I_{PP} = 8 A Forward I_{PP} = 16 A Forward I_{PP} = −8 A Forward I_{PP} = −16 A		7.26 11.8 −3.5 −6.7		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Standard IEC61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330, GND grounded.
2. These measurements performed with no external capacitor.
3. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at pulse test current I_T.

TYPICAL CHARACTERISTICS

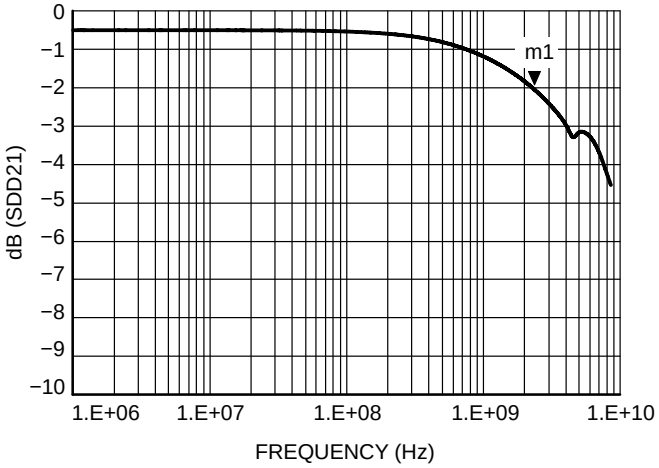


Figure 2. Typical Differential Mode Attenuation vs. Frequency

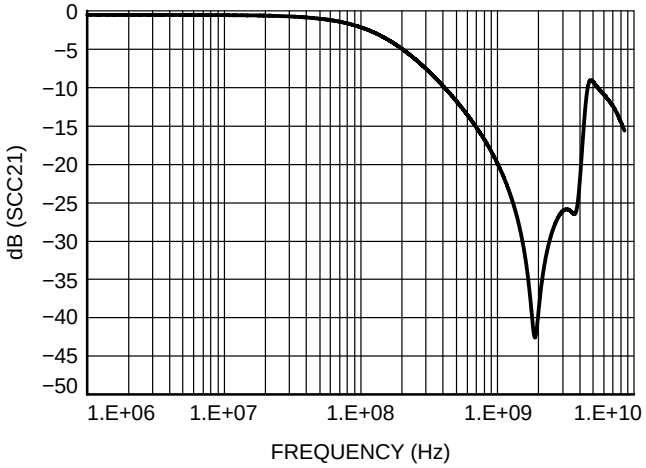


Figure 3. Typical Common Mode Attenuation vs. Frequency

Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	ESD814x Insertion Loss (dB)
USB 3.0	5	2.5 (m1)	m1 = 2.13

TRANSMISSION LINE PULSE (TLP) MEASUREMENTS

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 4. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10 s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 5 where an 8 kV IEC61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. Typical TLP I−V curves for the EMI814x are shown in Figure 4.

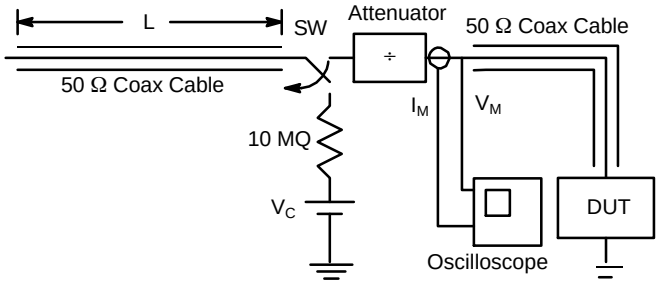


Figure 4. Simplified Schematic of a Typical TLP System

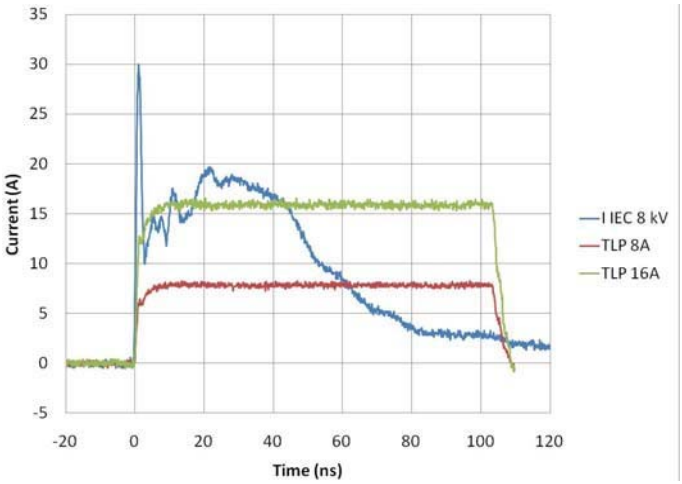


Figure 5. Comparison Between 8 kV IEC61000-4-2 and 8 A and 16 A TLP Waveforms

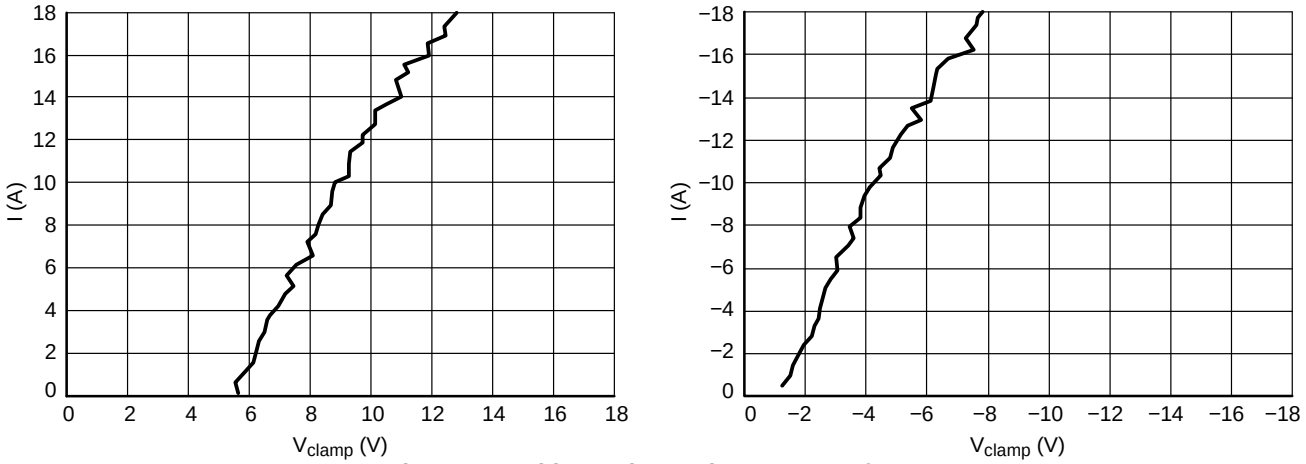


Figure 6. Positive and Negative TLP Waveforms

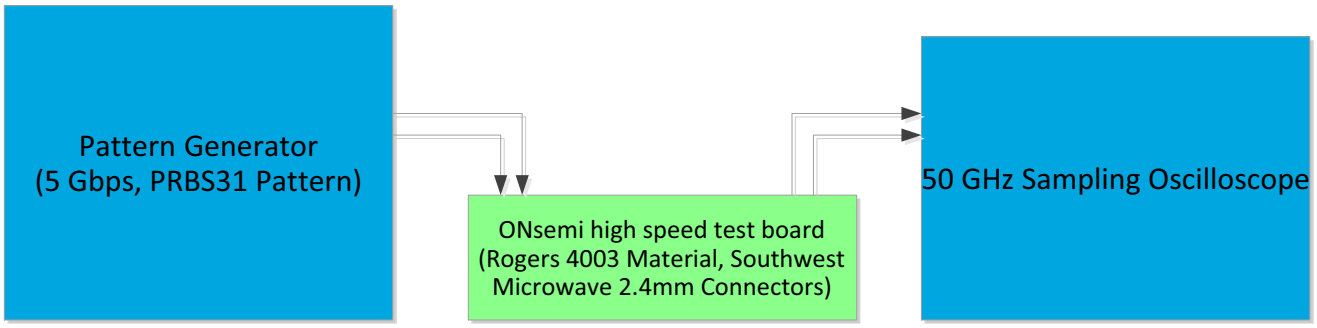


Figure 7. Eye Diagram Test Setup for 5Gbps Data Rate

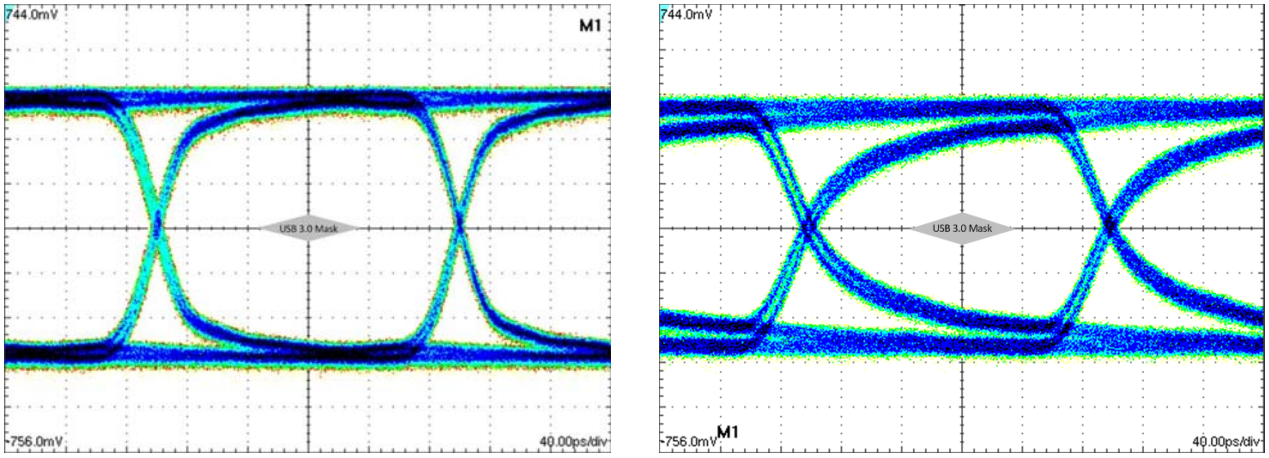


Figure 8. Eye Diagram 5Gbps with and without EMI814x

	Eye Height (mVppd)	Rise Time (ps)	Fall Time (ps)	Jrms (ps)	Jpp (ps)
Reference (No Device)-Left Figure	724	30.4	29.6	1.997	9.6
EMI814x Right Figure	405	60	60.8	3.484	16

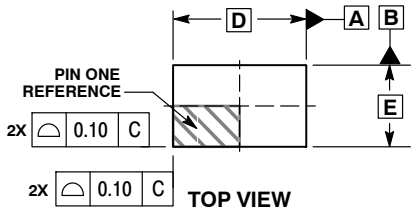
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

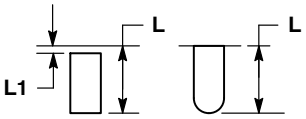
ON Semiconductor®

SCALE 4:1

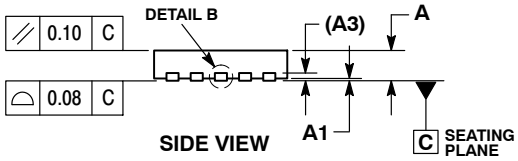
XDFN10 2.2x1.35, 0.4P
CASE 711AU
ISSUE B

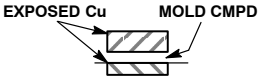
DATE 17 JUN 2014



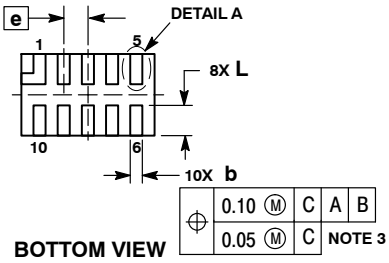


DETAIL A
ALTERNATE CONSTRUCTIONS





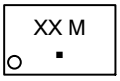
DETAIL B
ALTERNATE CONSTRUCTION



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.40	0.50
A1	0.00	0.05
A3	0.15 REF	
b	0.15	0.25
D	2.20 BSC	
E	1.35 BSC	
e	0.40 BSC	
L	0.40	0.60
L1	---	0.15

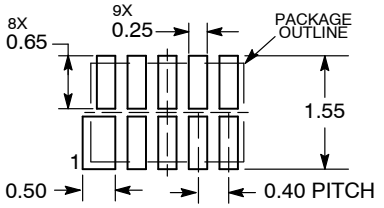
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**XDFN10 2.2X1.35, 0.4P**		**PAGE 1 OF 1**

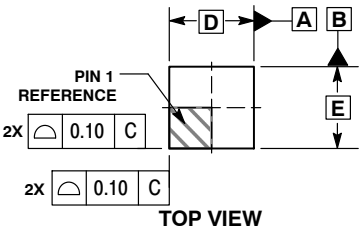
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

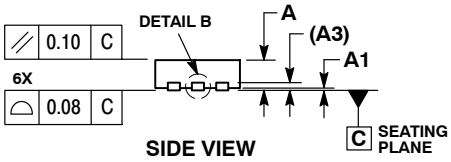
SCALE 4:1

XDFN6 1.40x1.35, 0.4P
CASE 711AV
ISSUE A

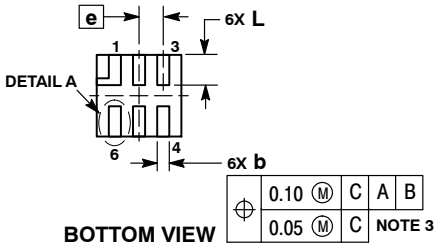
DATE 04 JUN 2014



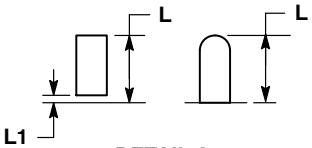
TOP VIEW



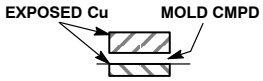
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

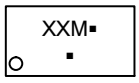


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.40	0.50
A1	0.00	0.05
A3	0.15 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.35 BSC	
e	0.40 BSC	
L	0.40	0.60
L1	---	0.15

GENERIC MARKING DIAGRAM*



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(Note: Microdot may be in either location)

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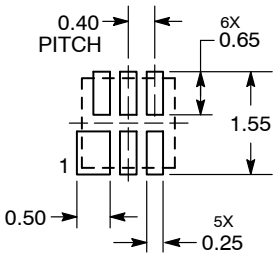
RECOMMENDED MOUNTING FOOTPRINT



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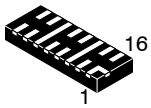
DESCRIPTION:	XDFN6 1.40X1.35, 0.4P	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

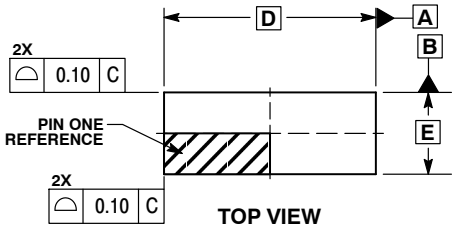
ON Semiconductor®



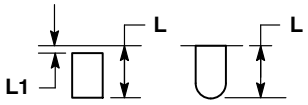
SCALE 4:1

XDFN16 3.5x1.35, 0.4P
CASE 711AW
ISSUE A

DATE 17 JUN 2014



TOP VIEW



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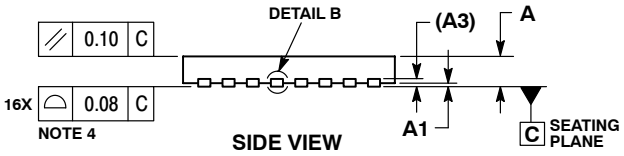
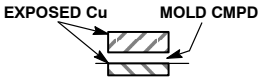
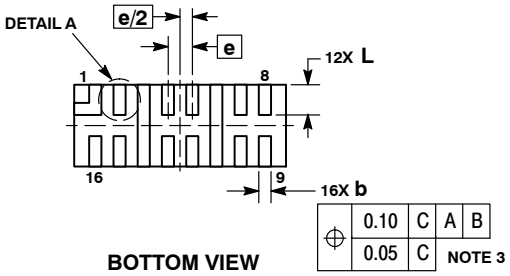
ALTERNATE TERMINAL CONSTRUCTIONS



SIDE VIEW



DETAIL B
ALTERNATE CONSTRUCTION



BOTTOM VIEW

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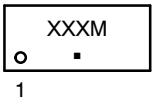

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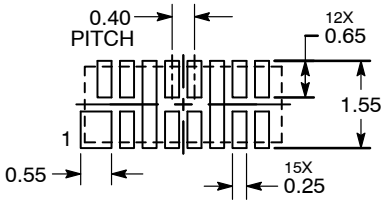
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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