ESD Protection Diode, Ultra-Low Capacitance

ESD9P5.0ST5G

The ESD9P Series is designed to protect voltage sensitive components that require low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs that utilize high-speed lines such as USB.

Specification Features:

- Low Capacitance 1.3 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.039" x 0.024" (1.00 mm x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 5 V
- Low Leakage
- Response Time is Typically < 1.0 ns
- IEC61000-4-2 Level 4 ESD Protection
- AEC-Q101 Qualified
- These Devices are Pb-Free and are RoHS Compliant

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V-0 LEAD FINISH: 100% Matte Sn (Tin) MOUNTING POSITION: Any QUALIFIED MAX REFLOW TEMPERATURE: 260°C Device Meets MSL 1 Requirements

MAXIMUM RATINGS

Rating	Symbol	Value	Unit	
IEC 61000-4-2 (ESD)	Contact Air		±10 ±15	kV
Total Power Dissipation on FR- (Note 1) @ T _A = 25°C	PD	150	mW	
Junction and Storage Temperat	T _J , T _{stg}	–55 to +150	°C	
Lead Solder Temperature – Max (10 Second Duration)	ΤL	260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

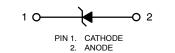
1. $FR-5 = 1.0 \times 0.75 \times 0.62$ in.

See Application Note AND8308/D for further description of survivability specs.



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MARKING DIAGRAM



T = Specific Device Code M = Date Code

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]			
ESD9P5.0ST5G	SOD-923 (Pb-Free)	8000/Tape & Reel			
+For information on tape and reel specifications,					

including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

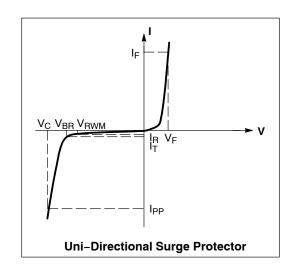
DEVICE MARKING INFORMATION

See specific marking information in the device marking column of the Electrical Characteristics tables starting on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$

Symbol	Parameter			
I _{PP}	Maximum Reverse Peak Pulse Current			
V _C	Clamping Voltage @ IPP			
V _{RWM}	Working Peak Reverse Voltage			
I _R	Maximum Reverse Leakage Current @ V_{RWM}			
V _{BR}	Breakdown Voltage @ I _T			
Ι _Τ	Test Current			
١ _F	Forward Current			
V _F	Forward Voltage @ I _F			
P _{pk}	Peak Power Dissipation			
С	Max. Capacitance @ $V_R = 0$ and f = 1.0 MHz			



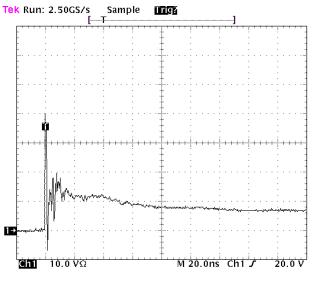
*See Application Note AND8308/D for detailed explanations of datasheet parameters.

ELECTRICAL CHARACTERISTICS (T _A	$_{\rm A}$ = 25°C unless otherwise noted,	$I, V_F = 1.0 V Max. @ I_F = 10 mA for all types)$
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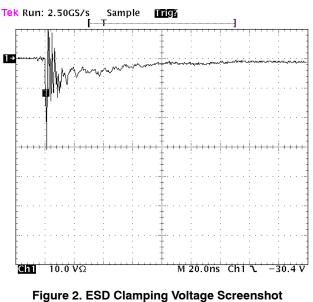
		V _{RWM} (V)	I _R (μΑ) @ V _{RWM}	V _{BR} (V) @ I _T (Note 2)	ե	C (pF)	V _C (V) @ I _{PP} = 1 A (Note 4)	v _c
Device	Device Marking	Max	Max	Min	mA	Max	Мах	Per IEC61000-4-2 (Note 3)
ESD9P5.0ST5G	Т	5.0	1.0	5.8	1.0	1.3	9.8	Figures1and 2 See Below

*Other voltages available upon request.
2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

4. Surge current waveform per Figure 5.









ESD9P5.0ST5G

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

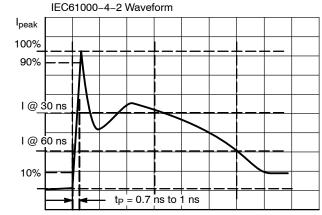


Figure 3. IEC61000-4-2 Spec

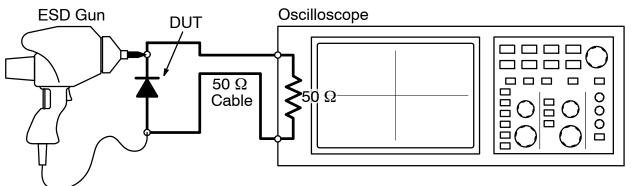


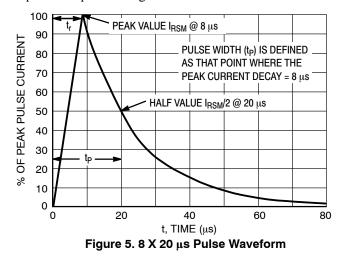
Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

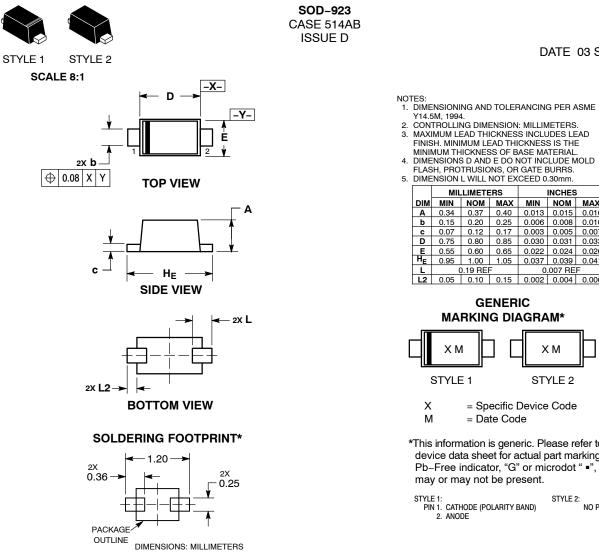
For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000–4–2 waveform. Since the IEC61000–4–2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.



MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



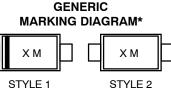
See Application Note AND8455/D for more mounting details

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



DATE 03 SEP 2020

	MIL	LIMETE	RS	INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
С	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
HE	0.95	1.00	1.05	0.037	0.039	0.041
L	0.19 REF			0	.007 RE	F
L2	0.05	0.10	0.15	0.002	0.004	0.006



= Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ",

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