May 2014

FAN25801
250 mA, Low-I_Q, Low-Noise, LDO Regulator

Features

- V_{IN}: 2.3 V to 5.5 V
- V_{OUT} = 5.14 V (I_{OUT} Max. = 250 mA)
- Output Noise Density at 250 mA and 10 kHz = 20 nV/√Hz (Integrated 10 µVrms)
- Low I_Q of 17 µA in Regulation and Low-I_Q Dropout Mode with Optimized Dropout Transitions
- <70 mV Dropout Voltage at 250 mA Load
- Controlled Soft-Start to Reduce Inrush Current
- Thermal Shutdown Protection (TSD)
- Input Under-Voltage Lockout (UVLO)
- Short-Circuit Protection (SCP)
- Stable with Two 1.5 µF, 0201 Ceramic Capacitors at VOUT
- 4-Ball WLCSP, 0.65 mm x 0.65 mm, 0.35 mm Pitch, Plated Solder, 330 µm Maximum Thickness

Applications

- WiFi Modules
- PDA Handsets
- Smart Phones, Tablets, Portable Devices

Description

The FAN25801 is a linear low-dropout regulator with a high PSRR (80 dB typical at 100 Hz) and low output noise (typically 10 µV_{RMS} over a 10 Hz to 100 kHz bandwidth). The LDO can provide up to 250 mA of output current.

The enable control pin can be used to shut down the device and disconnect the output load from the input. During shutdown, the supply current drops below 1 µA.

The FAN25801 is designed to be stable with space-saving ceramic capacitors as small as 0201 case size. The FAN25801 is available in a 4-bump, 0.35 mm pitch, WLCSP package.

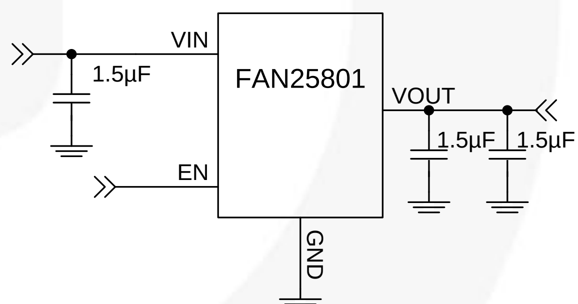


Figure 1. Typical Application

Ordering Information

Part Number	V_{OUT}	I_{OUT} Max.	Operating Temperature	Package	Packing Method
FAN25801AUC514X	5.14 V	250 mA	-40°C to 85°C	4-Bump, WLCSP, 0.65 x 0.65 mm, 0.35 mm Pitch	Tape & Reel

Block Diagram

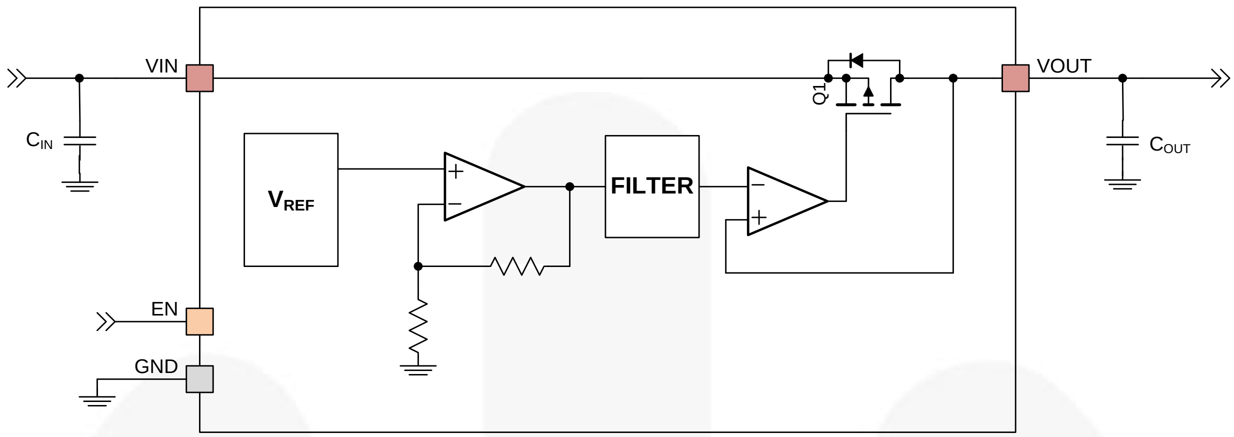


Figure 2. IC and System Block Diagram

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Unit
C_{IN}	1.5 µF, 6.3 V, X5R, 0201	Murata GRM033R60J155M	C	1.5(1)	µF
C_{OUT}	2x1.5 µF, 6.3 V, X5R, 0201	Murata GRM033R60J155M		1.5(1)	µF
$C_{Alternative}$(2)	1.0 µF, 6.3 V, X5R, 0201	Murata GRM033R60J105M		1.0(1)	µF

Notes:

1. Capacitance value does not reflect effects of bias, tolerance, and temperature. *See Recommended Operating Conditions and Operation Description sections for more information.*
2. $C_{Alternative}$ can be used for both C_{IN} and C_{OUT}. FAN25801 is stable with one 1 µF at C_{IN} and one 1 µF at C_{OUT}.

Pin Configuration

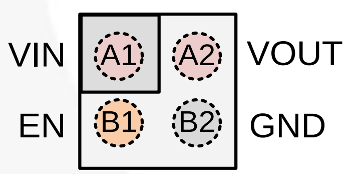


Figure 3. Top-Through View

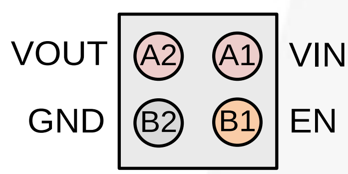


Figure 4. Bottom View

Pin Definitions

Pin #	Name	Description
A1	VIN	**Input Voltage**. Connect to input power source and C_{IN}.
A2	VOUT	**Output Voltage**. Connect to C_{OUT} and load.
B1	EN	**Enable**. The device is in Shutdown Mode when this pin is LOW. No internal pull-down. Do not leave this pin floating. Recommended to not tie EN pin directly to VIN.(3)
B2	GND	**Ground**. Power and IC ground. All signals are referenced to this pin.

Note:

3. EN can be tied to VIN, but it is recommended to tie a 1.8 V logic voltage to drive it.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Input Voltage with Respect to GND		-0.3	6.0	V
V_{CC}	Voltage on Any Other Pin (with Respect to GND)		-0.3	V_{IN}+0.3(4)	V
T_J	Junction Temperature		-40	+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	4000		V
		Charged Device Model per JESD22-C101	1500		
LU	Latch Up		JESD 78D		

Note:

4. Lesser of 6.0 V or V_{IN} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage	2.3		5.5(5)	V
I_{OUT}	Output Current (V_{OUT} = 5.14 V)			250	mA
C_{IN}	Input Capacitor (Effective Capacitance)(6)	0.4	0.8		µF
C_{OUT}	Output Capacitor (Effective Capacitance)(6)	0.4	0.8	15.0	µF
T_A	Ambient Temperature	–40		+85	°C
T_J	Junction Temperature	–40		+125	°C

Notes:

5. For V_{IN} ≥ 5V, thermal properties of the device must be taken into account at maximum load of 250 mA; refer to θ_{JA} thermal properties.
6. Effective capacitance, including the effects of bias, tolerance, and temperature. *See the Operation Description section for more information.*

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature, $T_{J(max)}$, at a given ambient temperature, T_A.

Symbol	Parameter	Typ.	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	180	°C/W
Ψ_{JB}	Junction-to-PCB Thermal Resistance	50	°C/W

Electrical Specifications

Minimum and maximum values are at V_{IN} = V_{OUT} + 0.3 V; T_A = -40°C to +85°C; and test circuit shown in Figure 1. Typical values are at V_{IN} = V_{OUT} + 0.3 V, T_A = 25°C, I_{LOAD} = 10 mA, and V_{EN} = 1.8 V, unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
LDO							
I_{IN}	V_{IN} Supply Current	5.4 V ≤ V_{IN} ≤ 5.5 V, I_{LOAD} = 0 mA			17.0	25.0	µA
		Dropout(8), I_{LOAD} = 0 mA			18.5	30.0	
PSRR	Power Supply Rejection Ratio(7)	I_{OUT} = 10 mA, V_{IN} = 3.6 V	f = 50 Hz		80		dB
			f = 100 Hz		80		
			f = 1 kHz		80		
			f = 10 kHz		76		
e_n	Output Noise Voltage Density(7)	f = 10 kHz	I_{OUT} = 10 mA		16		nV/√Hz
			I_{OUT} = 250 mA		20		
e_{n_bw}	Output Noise Voltage (Integrated)(7)	f = 10 Hz – 100 kHz	I_{OUT} = 10 mA		7		$µV_{RMS}$
			I_{OUT} = 250 mA		10		
V_{DO}	V_{OUT} Dropout Voltage(8)	V_{OUT} = V_{OUT_TARGET} – 100 mV, I_{OUT} = 250 mA			70	110	mV
ΔV_{OUT}	V_{OUT} Voltage Accuracy	5 mA ≤ I_{OUT} ≤ 250 mA, V_{IN} = 5.4 V to 5.5 V		-1.9		+1.9	%
ΔV_{OUT_LOAD}	Load Regulation	I_{OUT} = 5 mA to 250 mA, V_{OUT} = 5.14 V			8	35	µV/mA
I_{LIM}	V_{OUT} Current Limit	I_{OUT} = 0 mA → Current Limit, V_{OUT} Drops by 2%, V_{OUT} = 5.14 V		275	323	400	mA
I_{SD}	Shutdown Supply Current	V_{EN} = 0 V, 2.9 V ≤ V_{IN} ≤ 4.8 V			0.125	1.000	µA
V_{UVLO}	Under-Voltage Lockout Threshold	Rising V_{IN}			2.1	2.3	V
V_{UVHYS}	Under-Voltage Lockout Hysteresis				150		mV
t_{START}	Startup Time	Rising EN to 95% V_{OUT}, I_{OUT} = 10 mA			250	500	µs
TSD	Thermal Shutdown	Rising Temperature			150		°C
		Hysteresis			20		
Logic Levels: EN							
V_{IH}	Enable High-Level Input Voltage			1.05			V
V_{IL}	Enable Low-Level Input Voltage					0.4	V
I_{EN}	Input Bias Current	V_{EN} = 1.8 V			0.04	1.00	µA

Notes:

7. Guaranteed by design; not tested in production.
8. Dropout voltage = V_{IN} - V_{OUTx} when V_{OUT} drops more than 100 mV below the nominal regulated V_{OUT} level.

Typical Characteristics

Unless otherwise specified; $V_{IN} = V_{OUT} + 0.3$ V, $V_{OUT} = 5.14$ V, $V_{EN} = 1.8$ V, and $T_A = +25°C$.

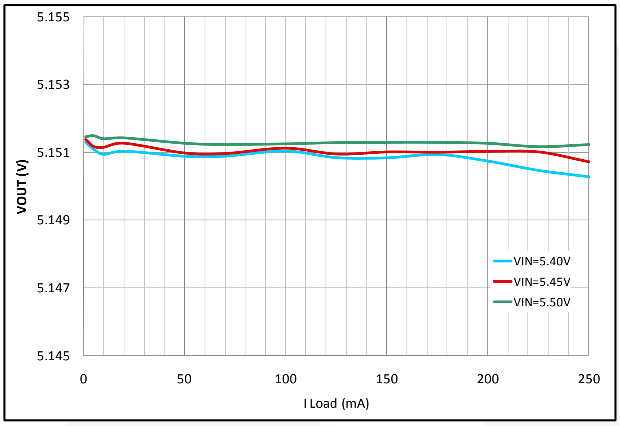


Figure 5. Output Regulation vs. Load Current and Input Voltage

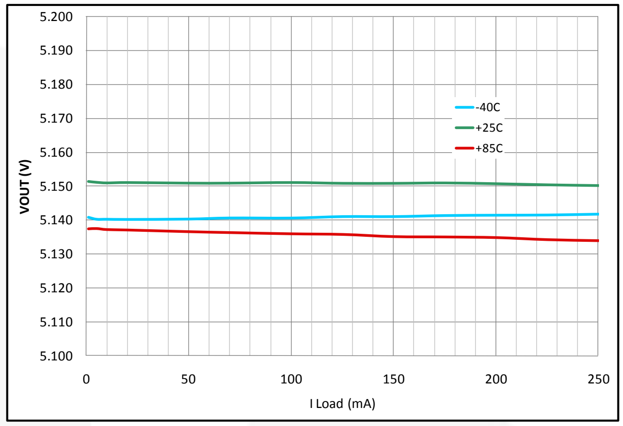


Figure 6 Output Regulation vs. Load Current and Temperature

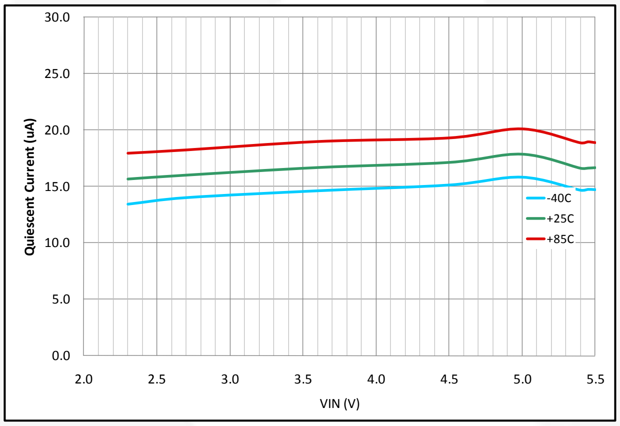


Figure 7. Quiescent Current vs. Input Voltage and Temperature

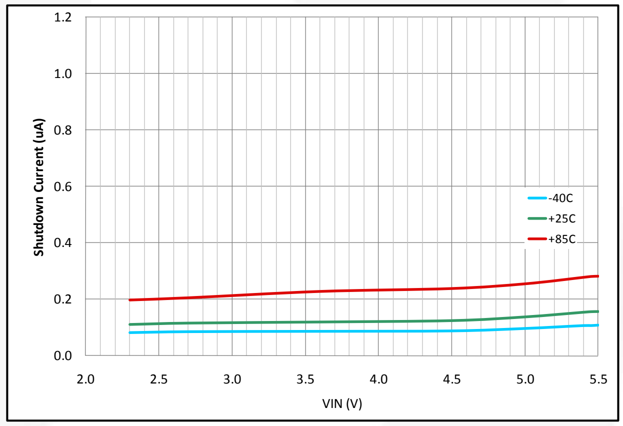


Figure 8. Shutdown Current vs. Input Voltage and Temperature

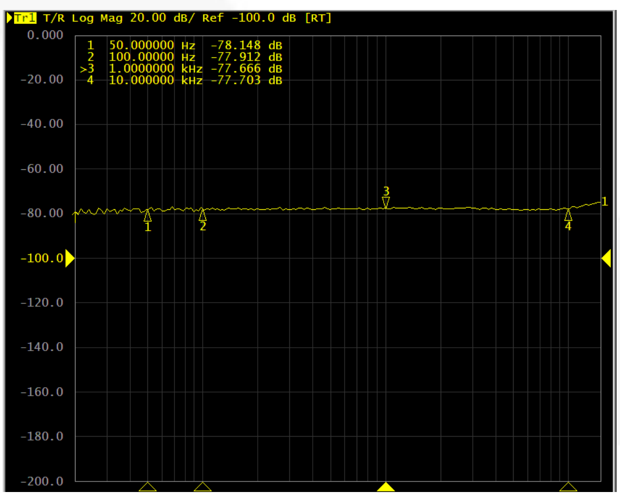


Figure 9. PSRR vs. Frequency, 10 mA Load

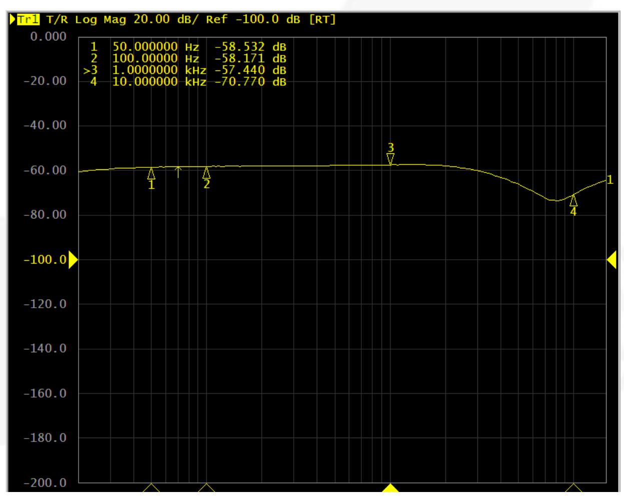


Figure 10. PSRR vs. Frequency, 250 mA Load

Typical Characteristics

Unless otherwise specified; $V_{IN} = V_{OUT} + 0.3$ V, $V_{OUT} = 5.14$ V, $V_{EN} = 1.8$ V, and $T_A = +25°C$.

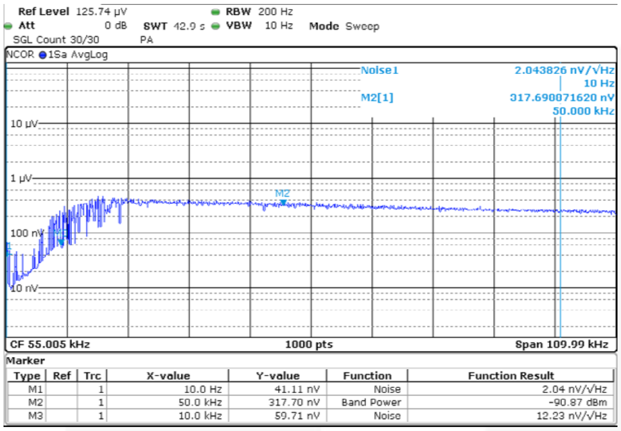


Figure 11. Output Noise Voltage vs. Frequency, 10 mA Load

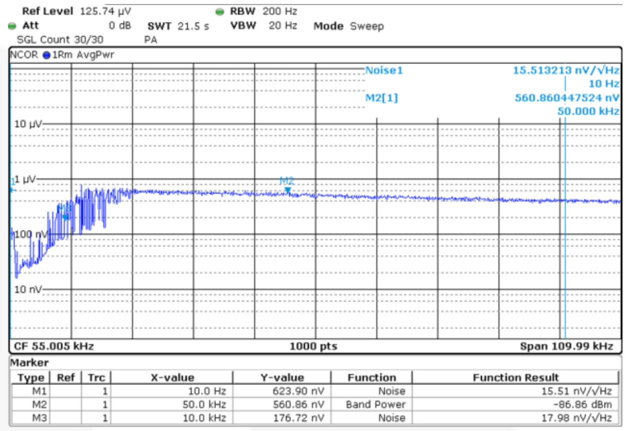


Figure 12. Output Noise Voltage vs. Frequency, 250 mA Load

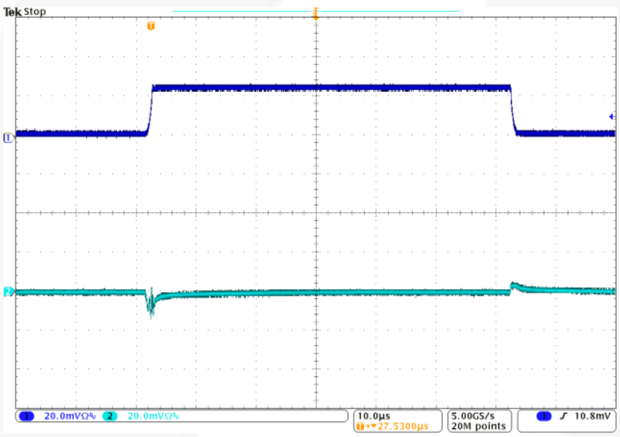


Figure 13. Load Transient, I_{OUT} = 10 mA ↔ 250 mA, t_R=t_F=1 µs

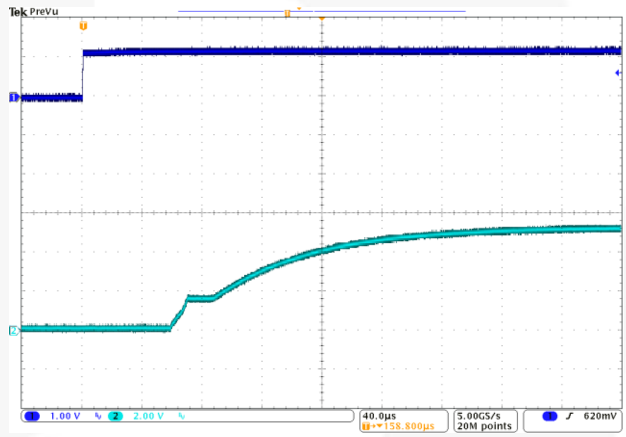


Figure 14. Startup, 10 mA Load

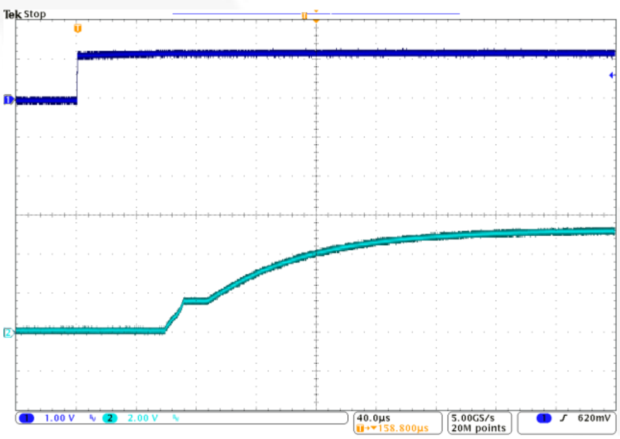


Figure 15. Startup, 250 mA Load

Circuit Description

The FAN25801 is a linear low-dropout (LDO) regulator that has high PSRR and low output noise. The enable control pin can be used to shut down the device and disconnect the output load from the input. During shutdown, the supply current drops below 1 µA. The LDO is designed to be stable with space-saving ceramic capacitors as small as 0201 case size.

Enable and Soft-Start

When EN is LOW, all circuits are off and the IC draws <550 nA of current. The EN pin does not have an internal pull-down resistor and must not be left floating. When EN is HIGH and V_{IN} is above the UVLO threshold, the regulator begins a soft-start cycle for the output. The soft-start cycle controls inrush current, limiting it to the I_{LIM} peak current limit.

Short-Circuit and Thermal Protection

The output current is short-circuit protected. When an output fault occurs, the output current is automatically limited to I_{LIM} and V_{OUT} drops. The resultant V_{OUT} is equal to I_{LIM} multiplied by the fault impedance.

Short-circuit fault or output overload may cause the die temperature to increase and exceed the maximum rating due to power dissipation. In such cases (depending upon the ambient temperature; the V_{IN}, load current, and thermal resistance (θ_{JB}) of the mounted die), the device may enter thermal shutdown.

If the die temperature exceeds the thermal shutdown temperature threshold, the onboard thermal protection disables the output until the temperature drops below its hysteresis value. At that point, the output is re-enabled and a new soft-start sequence occurs.

Thermal Considerations

For best performance, the die temperature and the power dissipated should be kept at moderate values. The maximum power dissipated can be evaluated based on the following relationship:

$$P_{D(\max)} = \left\{ \frac{T_{J(\max)} - T_A}{\Theta_{JA}} \right\} \quad (1)$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die; T_A is the ambient operating temperature; and θ_{JA} is dependent on the surrounding PCB layout and can be improved by providing a heat sink of surrounding copper ground.

The addition of backside copper with through-holes, stiffeners, and other enhancements can help reduce θ_{JA}. The heat contributed by the dissipation of devices nearby must be included in design considerations.

Capacitor Selection

An output capacitor with an effective capacitance between 400 nF and 15 µF is required for loop stability. The ESR value should be within 3 to 100 mΩ. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and the case size of the capacitor. Figure 16 is a typical derating curve for a 0201 case size, 1.5 µF, 6.3 V, X5R capacitor.

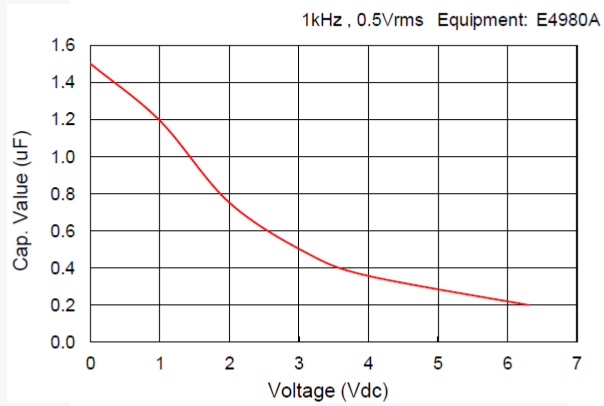


Figure 16. Capacitor DC Bias Characteristics

PCB Layout Recommendations

Capacitors should be placed as close to the IC as possible. All power and ground pins should be routed to their capacitors using top copper. The copper area connecting to the IC should be maximized to improve thermal performance.

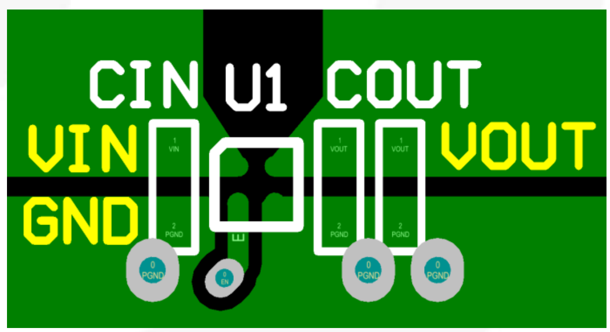
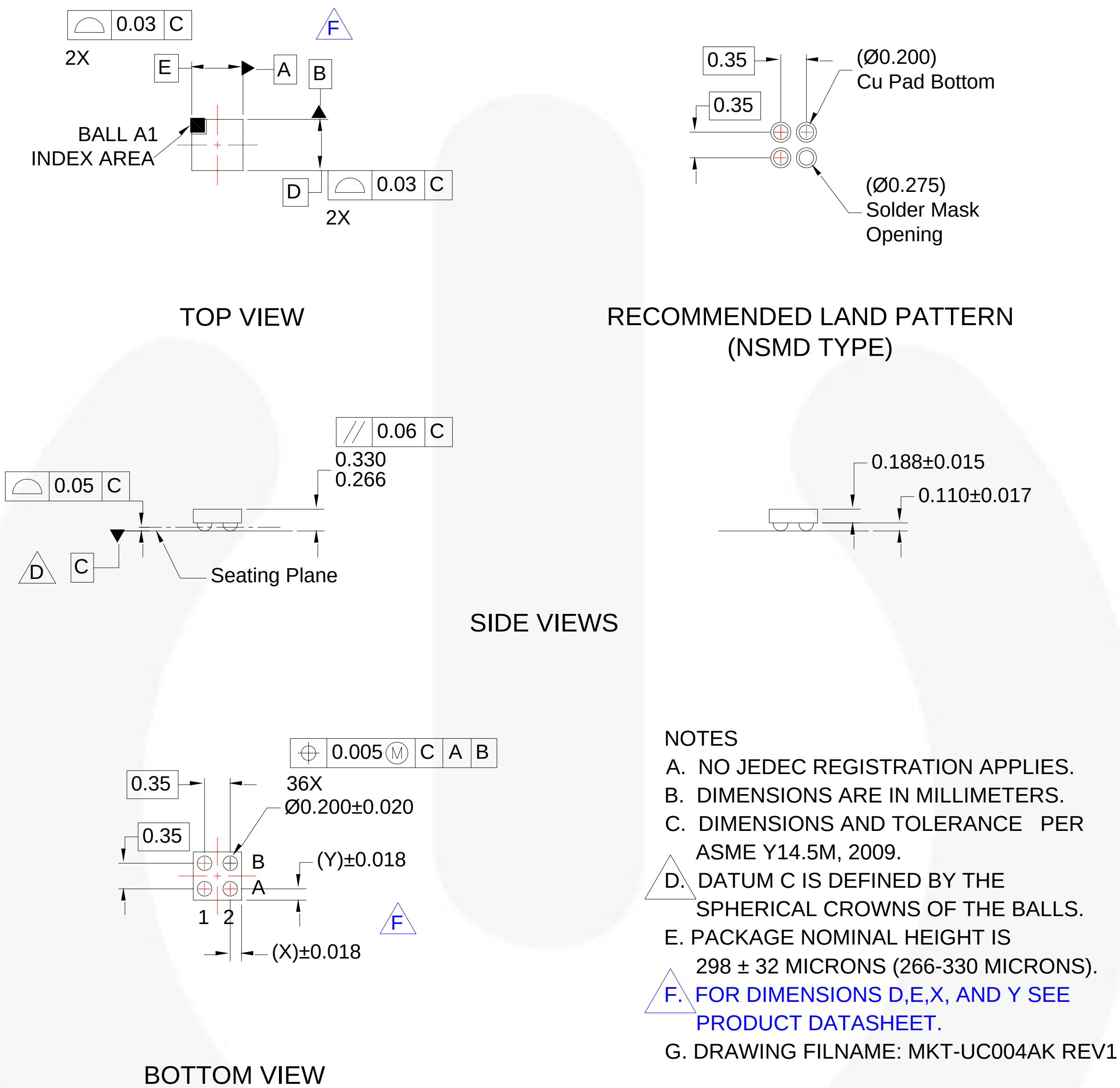


Figure 17. Recommended Layout

Physical Dimensions



NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 298 ± 32 MICRONS (266-330 MICRONS).

F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004AK REV1

Figure 17. 4-Ball, Wafer-Level, Chip-Scale Package (WLCSP), 0.35 mm Pitch

Product-Specific Dimensions

D	E	X	Y
0.65 ±0.025 mm	0.65 ±0.025 mm	0.15 mm	0.15 mm

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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