2 A Low-Voltage PMOS-NMOS Bridge Driver

FAN3268-F085

Description

The FAN3268 dual 2 A gate driver is optimized to drive a high−side P−channel MOSFET and a low−side N−channel MOSFET in motor control applications operating from a voltage rail up to 18 V. The driver has TTL input thresholds and provides buffer and level translation functions from logic inputs. Internal circuitry provides an under−voltage lockout function that prevents the output switching devices from operating if the V_{DD} supply voltage is below the operating level. Internal 100 kΩ resistors bias the non−inverting output low and the inverting output to V_{DD} to keep the external MOSFETs off during startup intervals when logic control signals may not be present.

The FAN3268 driver incorporates MillerDrive™ architecture for the final output stage. This bipolar−MOSFET combination provides high current during the Miller plateau stage of the MOSFET turn−on / turn−off process to minimize switching loss, while providing rail−to−rail voltage swing and reverse current capability.

The FAN3268 has two independent enable pins that default to on if not connected. If the enable pin for non− inverting channel A is pulled low, OUTA is forced low; if the enable pin for inverting channel B is pulled low, OUTB is forced high. If an input is left unconnected, internal resistors bias the inputs such that the external MOSFETs are off.

Features

- 4.5 V to 18 V Operating Range
- Drives High−Side PMOS and Low−Side NMOS in Motor Control or Buck Step−Down Applications
- Inverting Channel B Biases High−Side PMOS Device Off (with internal 100 kΩ Resistor) when V_{DD} is below UVLO Threshold
- TTL Input Thresholds
- 2.4 A Sink / 1.6 A Source at V_{OUT} = 6 V
- Internal Resistors Turn Driver Off If No Inputs
- MillerDrive Technology
- 8−Lead SOIC Package
- Rated from –40°C to +125°C Ambient
- AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Applications

- Motor Control with PMOS / NMOS Half−Bridge Configuration
- Buck Converters with High−Side PMOS Device; 100% Duty Cycle Operation Possible
- Logic−Controlled Load Circuits with High−Side PMOS Switch
- AEC−Q100 Qualified and PPAP Capable

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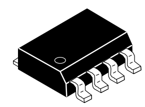
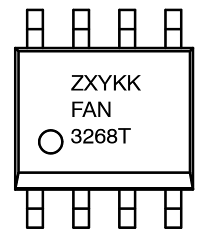


SOIC8
CASE 751EB

MARKING DIAGRAM



FAN3268T	=	Specific Device Code
Z	=	Assembly Plant Code
XY	=	2−Digit Data Code
KK	=	−Digits Lo Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Related Resources

AN−6069 − Application Review and Comparative Evaluation of Low−Side Gate Drivers

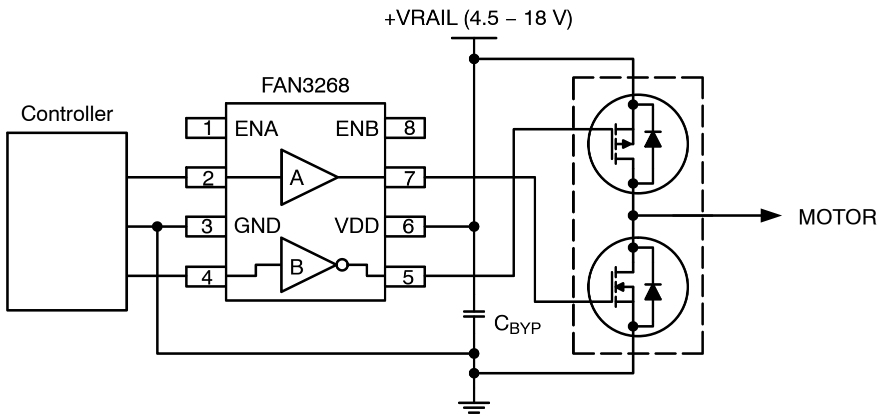


Figure 1. Typical Motor Drive Application

PACKAGE OUTLINE

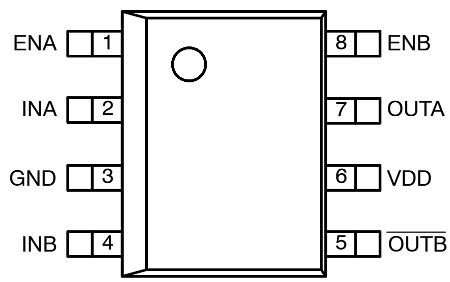


Figure 2. Pin Configuration (Top View)

THERMAL CHARACTERISTICS (Note 1)

Package	Θ_{JL} (Note 2)	Θ_{JL} (Note 3)	Θ_{JL} (Note 4)	Ψ_{JL} (Note 5)	Ψ_{JL} (Note 6)	Units
8−Pin Small Outline Integrated Circuit (SOIC)	40	31	89	43	3	°C/W

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top−side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51−2, JESD51−5, and JESD51−7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOIC−8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

PIN DEFINITIONS

Pin No.	Name	Description
1	ENA	*Enable Input for Channel A.* Pull pin low to inhibit driver A. ENA has TTL thresholds.
8	ENB	*Enable Input for Channel B.* Pull pin low to inhibit driver B. ENB has TTL thresholds.
3	GND	*Ground.* Common ground reference for input and output circuits.
2	INA	*Input to Channel A.*
4	INB	*Input to Channel B.*
7	OUTA	*Gate Drive Output A*: Held low unless required input(s) are present and V_{DD} is above the UVLO threshold.
5	$\overline{OUTB}$	*Gate Drive Output B* (inverted from the input): Held high unless required input is present and V_{DD} is above UVLO threshold.
6	VDD	*Supply Voltage*. Provides power to the IC.

OUTPUT LOGIC

FAN3268 (Channel A)		
ENA	**INA**	**OUTA**
0	0 (Note 7)	0
0	1	0
1 (Note 7)	0 (Note 7)	0
1 (Note 7)	1	1

FAN3268 (Channel B)		
ENB	**INB**	**$\overline{OUTB}$**
0	0 (Note 7)	1
0	1	1
1 (Note 7)	0 (Note 7)	1
1 (Note 7)	1	0

7. Default input signal if no external connection is made.

BLOCK DIAGRAM

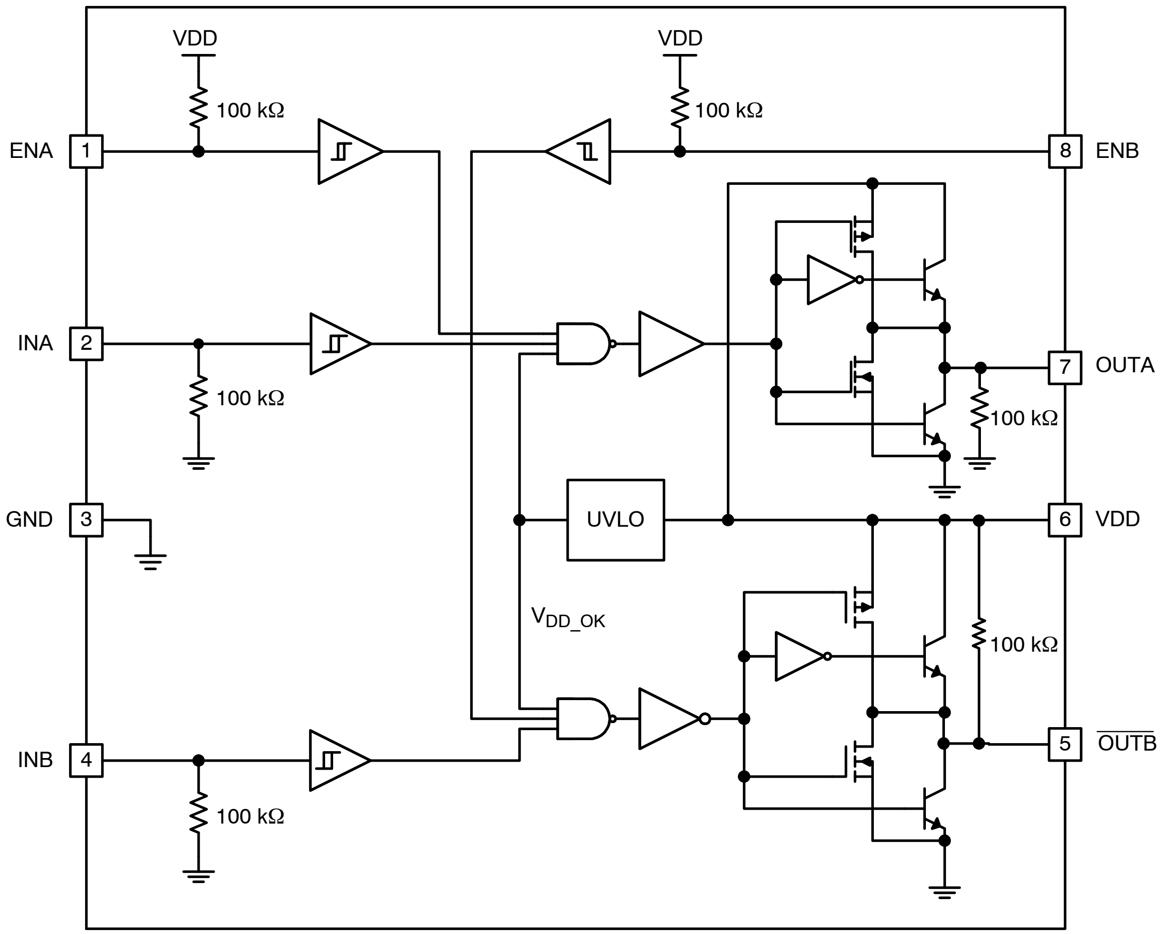


Figure 3. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD to GND	−0.3	20.0	V
V_{EN}	ENA, ENB to GND	GND − 0.3	V_{DD} + 0.3	V
V_{IN}	INA, INB to GND	GND − 0.3	V_{DD} + 0.3	V
V_{OUT}	OUTA, OUTB to GND	GND − 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)	–	+260	°C
T_J	Junction Temperature	−55	+150	°C
T_{STG}	Storage Temperature	−65	+150	°C

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{EN}	Enable Voltage (ENA, ENB)	0	V_{DD}	V
V_{IN}	Input Voltage (INA, INB)	0	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	Operating Range		4.5	–	18.0	V
I_{DD}	Supply Current Inputs / EN Not Connected		–	0.75	1.20	mA
V_{ON}	Device Turn−On Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	3.3	3.9	4.5	V
V_{OFF}	Device Turn−Off Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	3.1	3.7	4.3	V
INPUT (Note 8)						
V_{IL}	INx Logic Low Threshold		0.8	1.2	–	V
V_{IH}	INx Logic High Threshold		–	1.6	2.0	V
V_{HYS}	Logic Hysteresis Voltage		0.1	0.4	0.8	V
ENABLE						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	0.8	1.2	–	V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V	–	1.6	2.0	V
V_{HYS}	Logic Hysteresis Voltage (Note 9)		–	0.4	–	V
R_{PU}	Enable Pull−up Resistance (Note 9)		–	100	–	kΩ
OUTPUT						
I_{SINK}	Out Current, Mid−Voltage, Sinking (Note 9)	Out at VDD/2, C_{LOAD} = 0.1 μF, f = 1 kHz	–	2.4	–	A
I_{SOURCE}	Out Current, Mid−Voltage, Sourcing (Note 9)	Out at VDD/2, C_{LOAD} = 0.1 μF, f = 1 kHz	–	−1.6	–	A
I_{PK_SINK}	Out Current, Peak, Sinking (Note 9)	C_{LOAD} = 0.1 μF, f = 1 kHz	–	3	–	A
I_{PK_SOURCE}	Out Current, Peak, Sourcing (Note 9)	C_{LOAD} = 0.1 μF, f = 1 kHz	–	−3	–	A
t_{RISE}	Output Rise Time (Note 10)	C_{LOAD} = 1000 pF	–	12	22	ns
t_{FALL}	Output Fall Time (Note 10)	C_{LOAD} = 1000 pF	–	9	17	ns
t_{D1}	Propagation Delay	0 – 5 V_{IN}, 1 V/ns Slew Rate	7	14	32	ns
t_{D2}	Propagation Delay	0 – 5 V_{IN}, 1 V/ns Slew Rate	8	19	34	ns
V_{OH}	High Level Output Voltage	$V_{OH} = V_{DD} − V_{OUT}$, I_{OUT} = 1 mA	–	15	40	mV
V_{OL}	Low Level Output Voltage	I_{OUT} = 1 mA	–	10	25	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. EN inputs have TTL thresholds; refer to the ENABLE section.
9. Not tested in production.
10. *See the Timing Diagrams of Figure 4 and Figure 5.*

TIMING DIAGRAMS

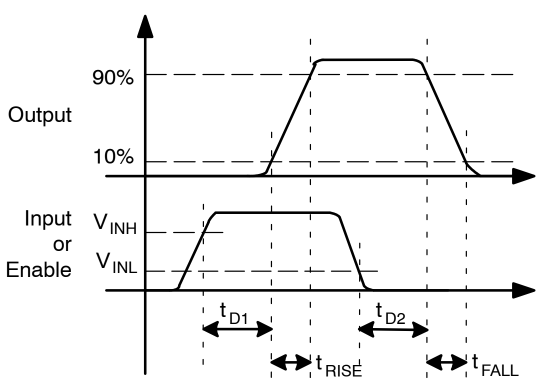


Figure 4. Non−Inverting

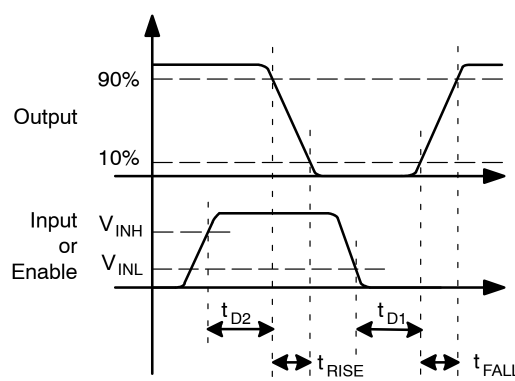


Figure 5. Inverting

TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at T_A = 25°C and V_{DD} = 12 V unless otherwise noted.)

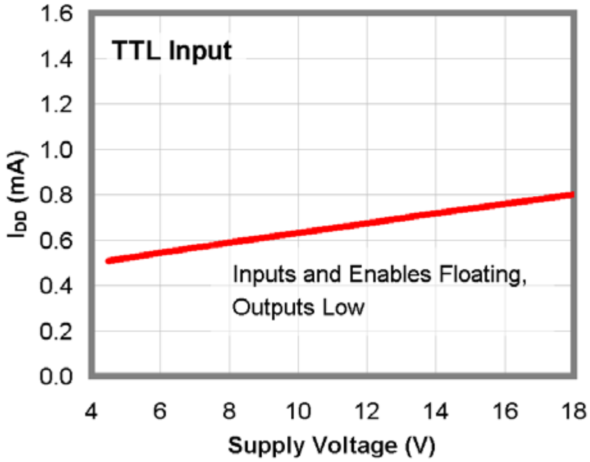


Figure 6. I_{DD} (Static) vs. Supply Voltage (Note 11)

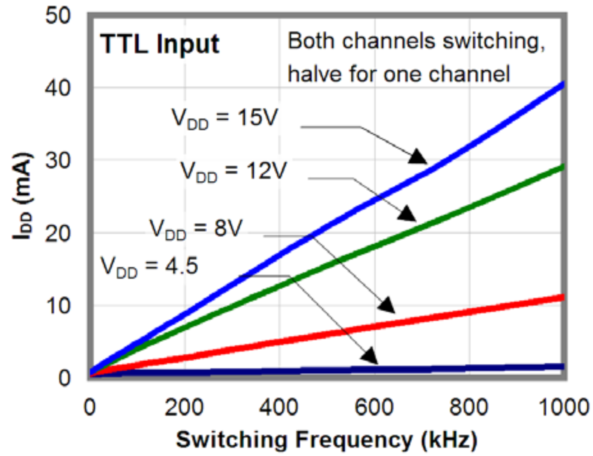


Figure 7. I_{DD} (No−Load) vs. Frequency

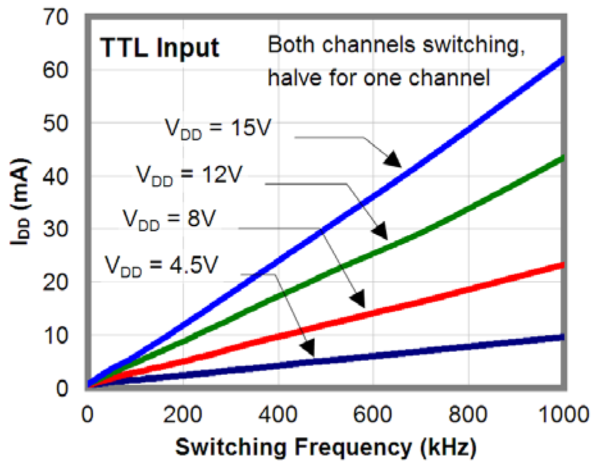


Figure 8. I_{DD} (1 nF Load) vs. Frequency

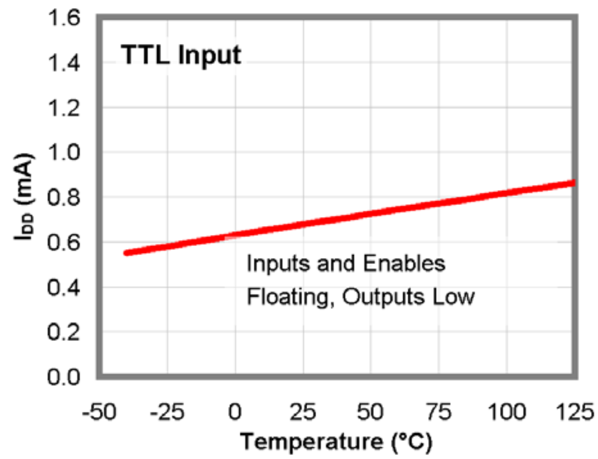


Figure 9. I_{DD} (Static) vs. Temperature (Note 11)

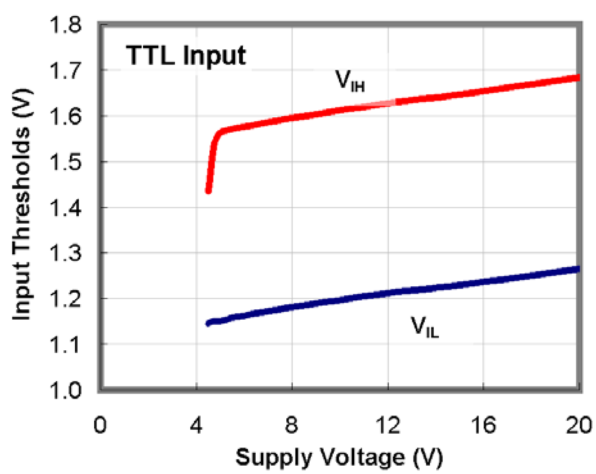


Figure 10. Input Thresholds vs. Supply Voltage

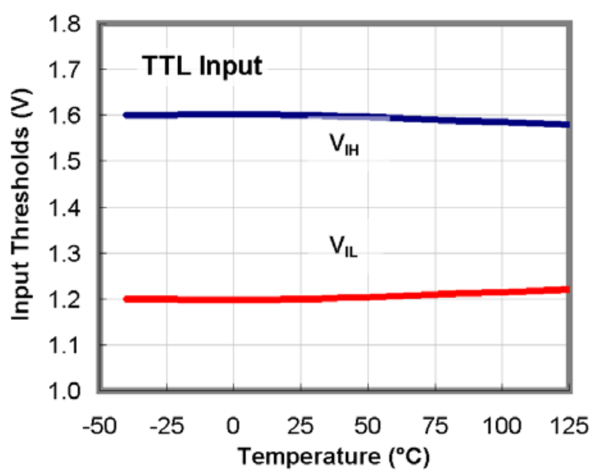


Figure 11. Input Thresholds vs. Temperature

NOTE:
11. For any inverting inputs pulled low, non−inverting inputs pulled high, or outputs driven high, static I_{DD} increases by the current flowing through the corresponding pull−up/down resistor shown in the block diagram in Figure 3.

TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at T_A = 25°C and V_{DD} = 12 V unless otherwise noted.) (continued)

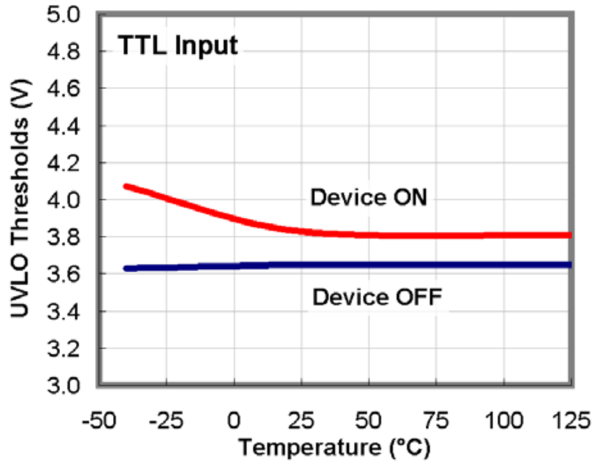


Figure 12. UVLO Threshold vs. Temperature

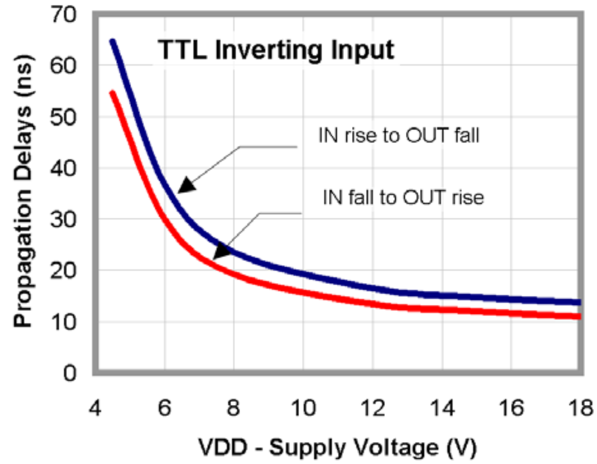


Figure 13. Propagation Delays vs. Supply Voltage

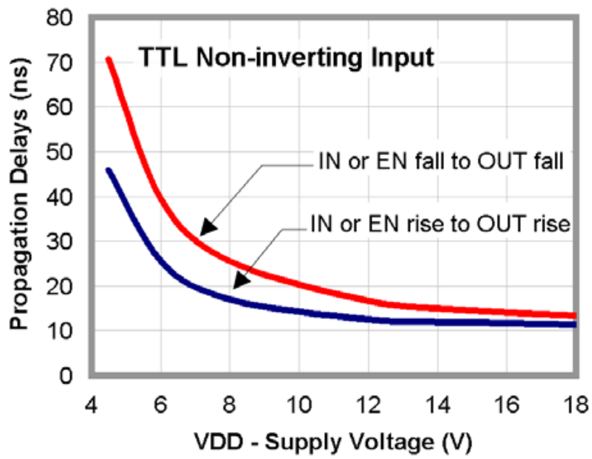


Figure 14. Propagation Delays vs. Supply Voltage

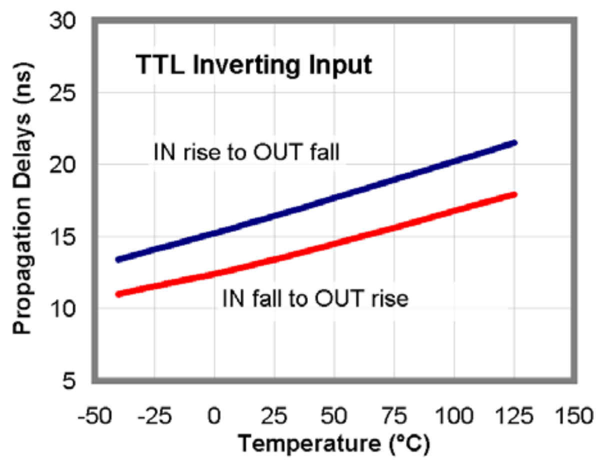


Figure 15. Propagation Delays vs. Temperature

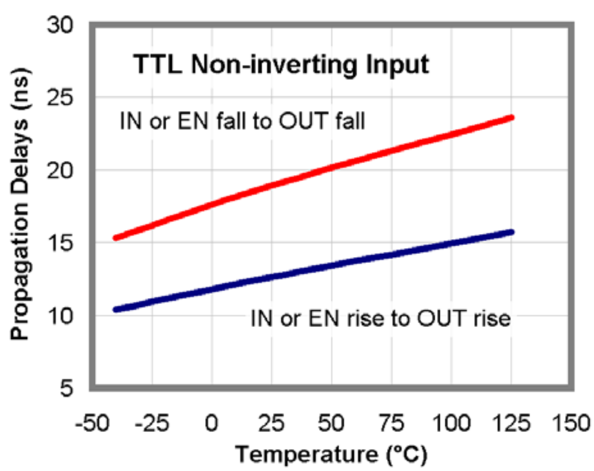


Figure 16. Propagation Delays vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at T_A = 25°C and V_{DD} = 12 V unless otherwise noted.) (continued)

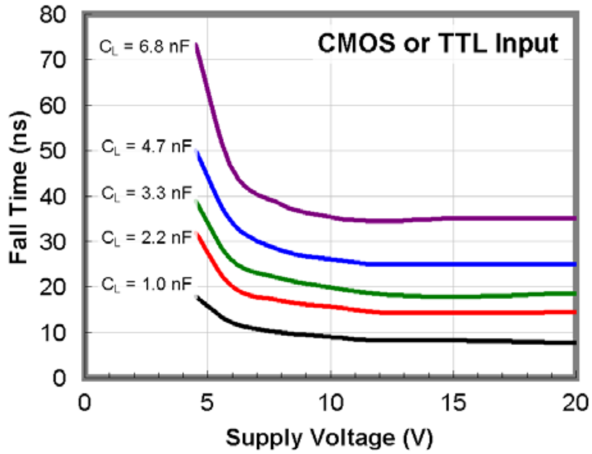


Figure 17. Fall Time vs. Supply Voltage

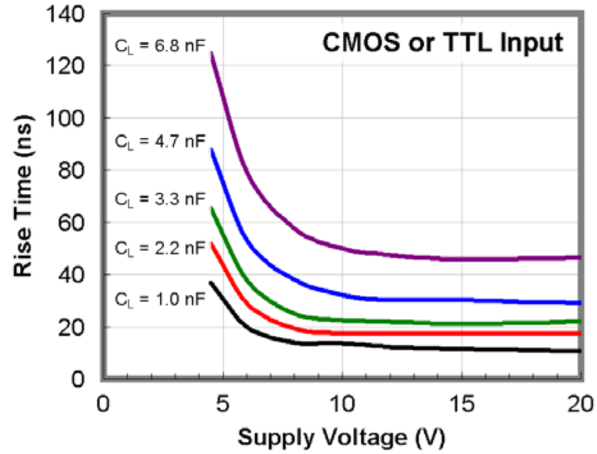


Figure 18. Rise Time vs. Supply Voltage

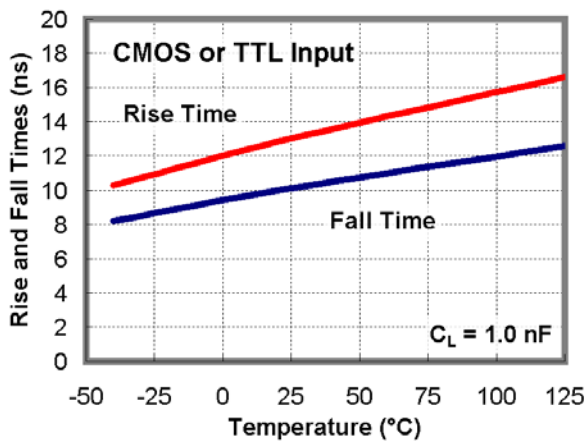


Figure 19. Rise and Fall Times vs. Temperature

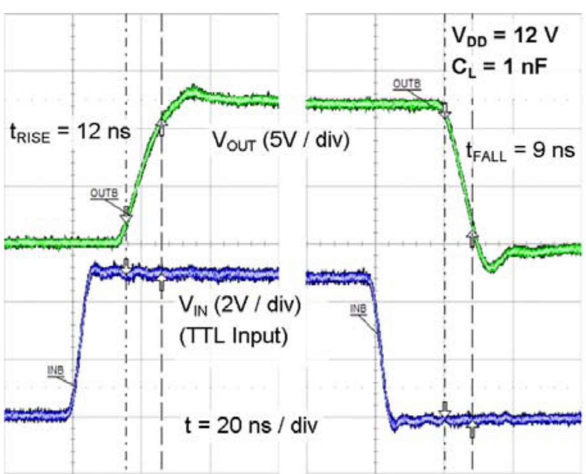


Figure 20. Rise/Fall Waveforms with 1 nF Load

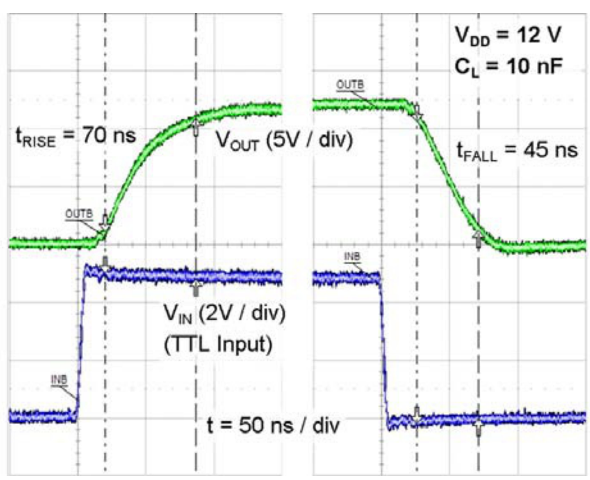


Figure 21. Rise/Fall Waveforms with 10 nF Load

TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at T_A = 25°C and V_{DD} = 12 V unless otherwise noted.) (continued)

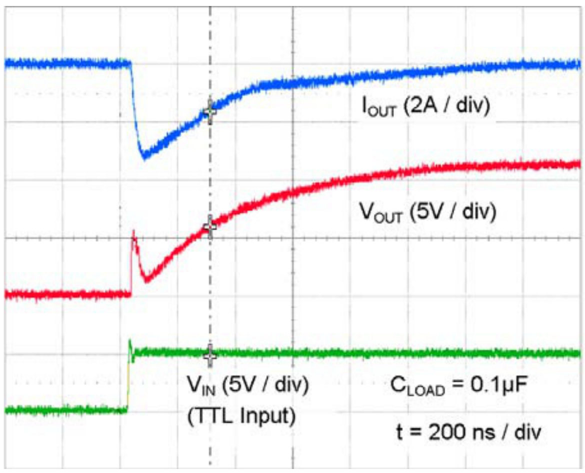


Figure 22. Quasi−Static Source Current with V_{DD} = 12 V

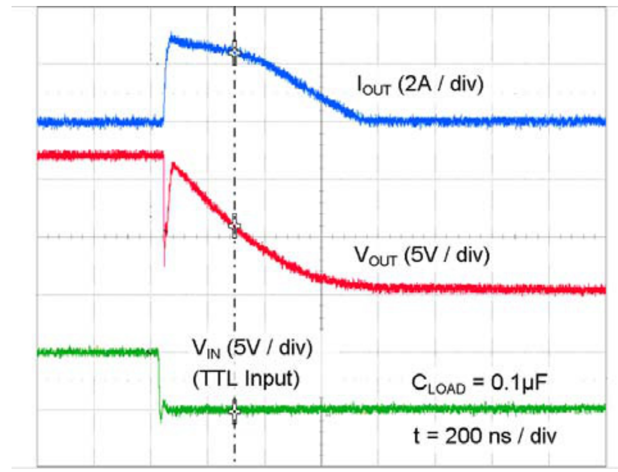


Figure 23. Quasi−Static Sink Current with V_{DD} = 12 V

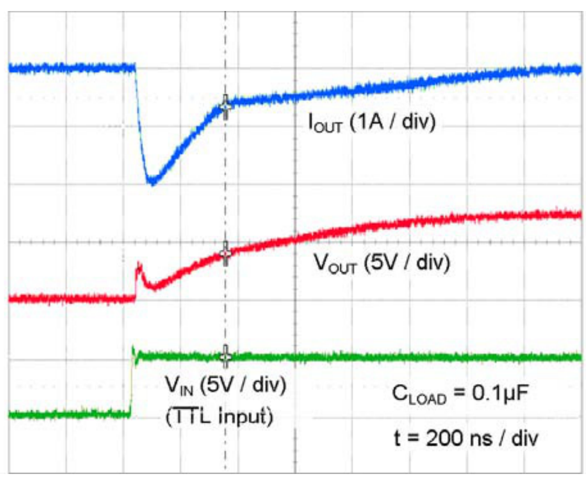


Figure 24. Quasi−Static Source Current with V_{DD} = 8 V

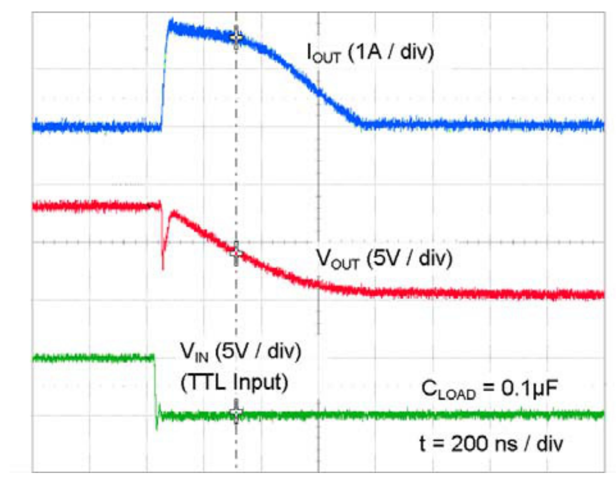


Figure 25. Quasi−Static Sink Current with V_{DD} = 8 V

TEST CIRCUIT

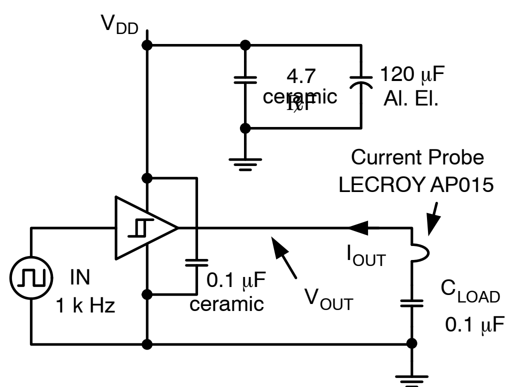


Figure 26. Quasi−Static I_{OUT} / V_{OUT} Test Circuit

APPLICATIONS INFORMATION

Input Thresholds

The FAN3268 driver has TTL input thresholds and provides buffer and level translation functions from logic inputs. The input thresholds meet industry−standard TTL−logic thresholds, independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic high. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/μs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

Static Supply Current

In the I_{DD} (static) typical performance characteristics *(see Figure 6)*, the curve is produced with all inputs / enables floating (OUT is low) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagram *(see Figure 3)*. In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

MillerDrive Gate Drive Technology

FAN3268 gate drivers incorporate the MillerDrive architecture shown in Figure 1. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between one and two thirds V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive architecture is to speed up switching by providing high current during the Miller plateau region when the gate−drain capacitance of the MOSFET is being charged or discharged as part of the turn−on / turn−off process.

For applications with zero voltage switching during the MOSFET turn−on or turn−off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.

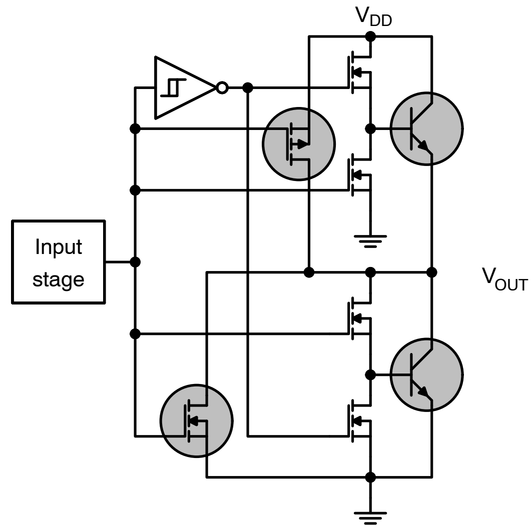


Figure 27. MillerDrive Output Architecture

Under−Voltage Lockout

Internal circuitry provides an under−voltage lockout function that prevents the output switching devices from operating if the V_{DD} supply voltage is below the operating level. When V_{DD} is rising, but below the 3.9 V operational level, internal 100 kΩ resistors bias the non−inverting output low and the inverting output to V_{DD} to keep the external MOSFETs off during startup intervals when logic control signals may not be present. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching.

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a device on quickly, a local high−frequency bypass capacitor C_{BYP} with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF commonly found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance C_{EQV}, defined here as Q_{GATE}/V_{DD}. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R, with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50 − 100 times the C_{EQV} or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1 − 10 nF mounted closest to the VDD and GND pins to carry the higher frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the C_{BYP} would be twice as large as when a single channel is switching.

Layout and Connection Guidelines

The FAN3268 gate driver incorporates fast−reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 2 A to facilitate voltage transition times from under 10ns to over 150 ns. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate from logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds at driver inputs and enable pins.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high−speed switching, while reducing the loop area that can radiate EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 100 kΩ resistors indicated on block diagrams command a low output (channel A) or a high output (channel B). In noisy environments, it may be necessary to tie inputs or enables of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re−triggering. These effects can be obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn−on and turn−off current paths should be minimized.

Operational Waveforms

Figure 28 shows startup waveforms for non−inverting channel A. At power−up, the driver output for channel A remains low until the V_{DD} voltage reaches the UVLO turn−on threshold, then OUTA operates in−phase with INA.

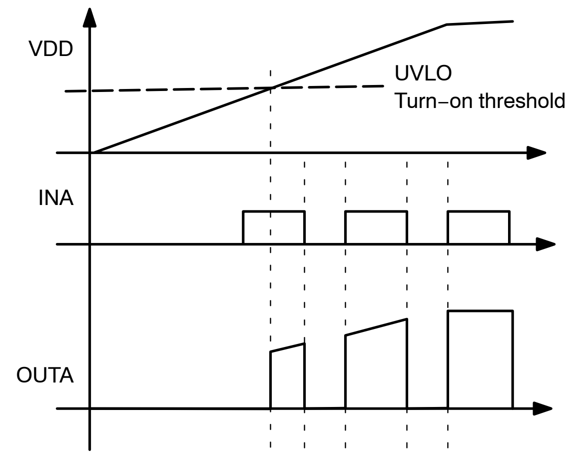


Figure 28. Non−Inverting Startup Waveforms

Figure 29 illustrates startup waveforms for inverting channel B. At power−up, the driver output for channel B is tied to V_{DD} through an internal 100 kΩ resistor until the V_{DD} voltage reaches the UVLO turn−on threshold, then OUTB operates out of phase with INB.

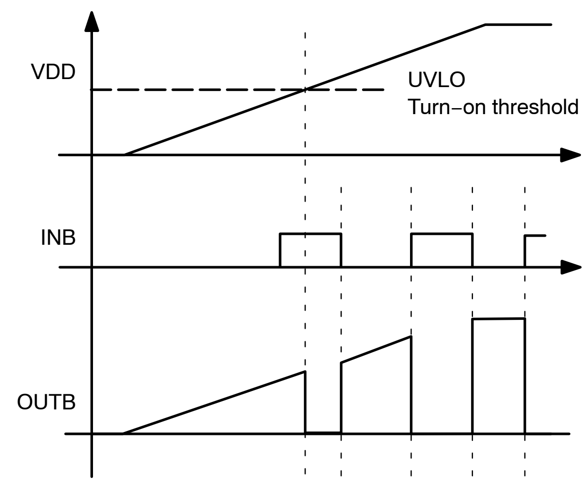


Figure 29. Inverting Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate−source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \times V_{GS} \times f_{SW} \times n \quad \text{(eq. 2)}$$

where n is the number of driver channels in use (1 or 2).

Dynamic Pre−drive / Shoot−through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up / pull−down resistors, can be obtained using the “I_{DD} (No−Load) vs. Frequency” graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \times V_{DD} \times n \quad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming Ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \times \Psi_{JB} + T_B \quad \text{(eq. 4)}$$

where:

T_J = driver junction temperature
Ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation
T_B = board temperature in location defined in Note 1 under Thermal Resistance table.

As an example of a power dissipation calculation, consider an application driving two MOSFETs with a gate charge of 60 nC with $V_{GS} = V_{DD} = 7$ V. At a switching frequency of 500 kHz, the total power dissipation is:

$$P_{GATE} = 60\text{ nC} \times 7\text{ V} \times 500\text{ kHz} \times 2 = 0.42\text{ W} \quad \text{(eq. 5)}$$

$$P_{DYNAMIC} = 3\text{ mA} \times 7\text{ V} \times 2 = 0.042\text{ W} \quad \text{(eq. 6)}$$

$$P_{TOTAL} = 0.46\text{ W} \quad \text{(eq. 7)}$$

The SOIC−8 has a junction−to−board thermal characterization parameter of Ψ_{JB} = 43°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_B = T_J - P_{TOTAL} \times \Psi_{JB} \quad \text{(eq. 8)}$$

$$T_B = 120°\text{C} \times 0.46\text{ W} \times 43°\text{C/W} = 100°\text{C} \quad \text{(eq. 9)}$$

Table 1. RELATED PRODUCTS

Part Number	Type	Gate Drive (Note 12) (Sink/Src)	Input Threshold	Logic	Package
FAN3226C	Dual 2 A	+2.4 A / −1.6 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8
FAN3226T	Dual 2 A	+2.4 A / −1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8
FAN3227C	Dual 2 A	+2.4 A / −1.6 A	CMOS	Dual Non−Inverting Channels + Dual Enable	SOIC8
FAN3227T	Dual 2 A	+2.4 A / −1.6 A	TTL	Dual Non−Inverting Channels + Dual Enable	SOIC8
FAN3228C	Dual 2 A	+2.4 A / −1.6 A	CMOS	Dual Channels of Two−Input/One−Output, Pin Config.1	SOIC8
FAN3228T	Dual 2 A	+2.4 A / −1.6 A	TTL	Dual Channels of Two−Input/One−Output, Pin Config.1	SOIC8
FAN3229C	Dual 2 A	+2.4 A / −1.6 A	CMOS	Dual Channels of Two−Input/One−Output, Pin Config.2	SOIC8
FAN3229T	Dual 2 A	+2.4 A / −1.6 A	TTL	Dual Channels of Two−Input/One−Output, Pin Config.2	SOIC8
FAN3268T	*Dual 2 A*	*+2.4 A / −1.6 A*	*TTL*	*Non−Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables*	*SOIC8*
FAN3223C	Dual 4 A	+4.3 A / −2.8 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8
FAN3223T	Dual 4 A	+4.3 A / −2.8 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8
FAN3224C	Dual 4 A	+4.3 A / −2.8 A	CMOS	Dual Non−Inverting Channels + Dual Enable	SOIC8
FAN3224T	Dual 4 A	+4.3 A / −2.8 A	TTL	Dual Non−Inverting Channels + Dual Enable	SOIC8
FAN3225C	Dual 4 A	+4.3 A / −2.8 A	CMOS	Dual Channels of Two−Input/One−Output	SOIC8
FAN3225T	Dual 4 A	+4.3 A / −2.8 A	TTL	Dual Channels of Two−Input/One−Output	SOIC8
FAN3121C	Single 9 A	+9.7 A / −7.1 A	CMOS	Single Inverting Channel + Enable	SOIC8
FAN3121T	Single 9 A	+9.7 A / −7.1 A	TTL	Single Inverting Channel + Enable	SOIC8
FAN3122T	Single 9 A	+9.7 A / −7.1 A	CMOS	Single Non−Inverting Channel + Enable	SOIC8
FAN3122C	Single 9 A	+9.7 A / −7.1 A	TTL	Single Non−Inverting Channel + Enable	SOIC8

12. Typical currents with OUT at 6 V and V_{DD} = 12 V.
13. Thresholds proportional to an externally supplied reference voltage.

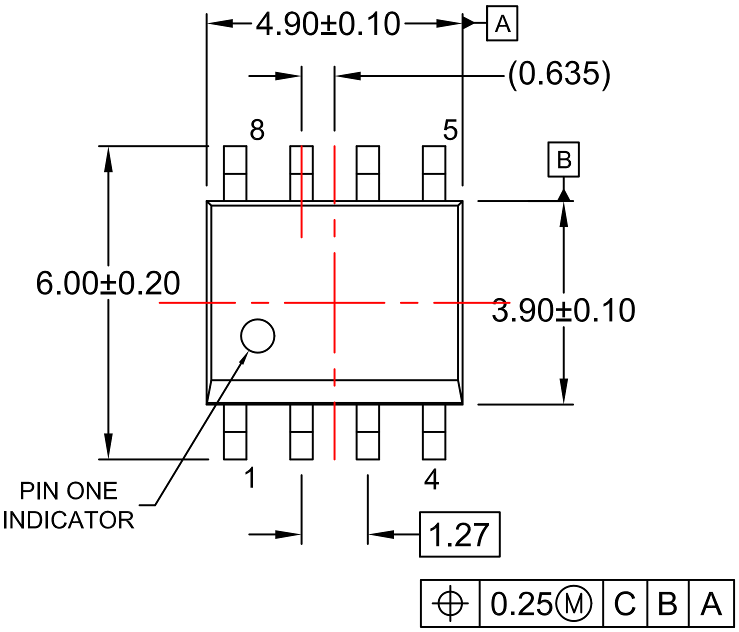
ORDERING INFORMATION

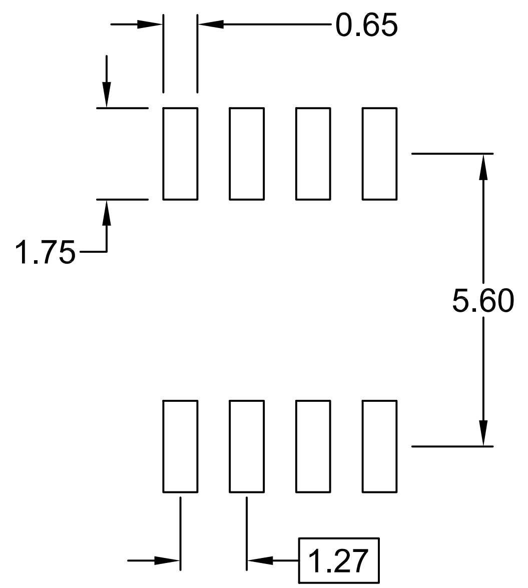
Device	Logic	Package	Input Threshold	Shipping†
FAN3268TMX−F085	Non−Inverting Channel and Inverting Channel + Dual Enables	SOIC8 (Pb−Free)	TTL	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

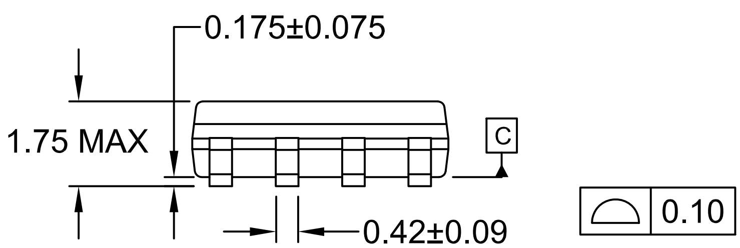
SOIC8
CASE 751EB
ISSUE A

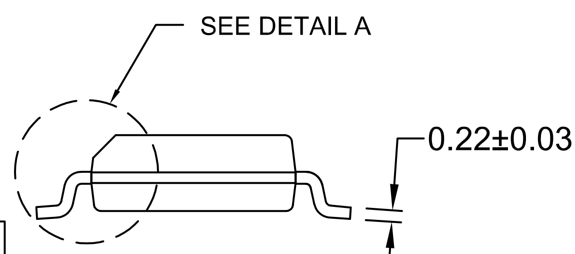
DATE 24 AUG 2017



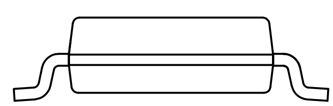


LAND PATTERN RECOMMENDATION

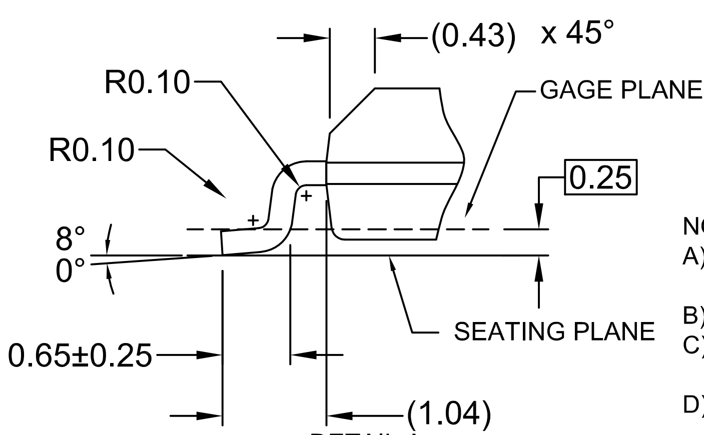




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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