Buck Regulator, 3.0 A

FAN53527

Descriptions

The FAN53527 is a step−down switching voltage regulator with an input voltage supply range of 2.5 V to 5.5 V. Device settings can be programmed through an I^2C interface, or the IC can be operated in stand−alone mode with pin controls for enable, output voltage, and Auto PFM or Forced PWM operation.

Using a proprietary architecture with synchronous rectification, the FAN53527 is capable of delivering 3.0 A continuous at over 80% efficiency, and maintain that efficiency with load currents as low as 10 mA. At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power−Save Mode where excellent transient response is maintained. In Shutdown Mode, the supply current drops below 1 μA, further reducing power consumption. At higher loads, the device automatically transitions to fixed−frequency PWM control, operating typically at 2.4 MHz.

The FAN53527 is available in a 15−bump, 1.310 mm x 2.015 mm, 0.4 mm ball pitch, Wafer−Level Chip−Scale Package (WLCSP).

Features

- I^2C Compatible Interface or Stand−Alone Operation
- Fixed−Frequency PWM Operation: 2.4 MHz
- Auto PFM Mode for High Efficiency at Light−Load
- Best−in−Class Load Transient Response
- Wide Input Voltage Range: 2.5 V to 5.5 V
- Continuous Output Current Capability: 3.0 A
- Low Quiescent Current: 48 μA
- Low Shutdown Current: <1 μA
- Input Under−Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- Programmable/ Selectable Output Voltage:
  - 1 V to 1.39375 V in 6.25 mV Steps (I^2C Programmable)
  - 1.125 V & 1.081 V (Pin Selectable Values)
- Programmable Output Voltage Transition Slew Rate

Applications

- Application, Graphic, and DSP Processors
- Hard Disk Drives, LPDDR4, LPDDR5
- Smart Phones
- Gaming Devices
- Tablets, Netbooks, Ultra−Mobile PCs

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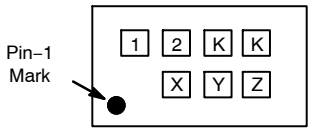
WLCSP−15
CASE 567QS

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2−Weeks Date Code
Z	= Assembly Plant Code

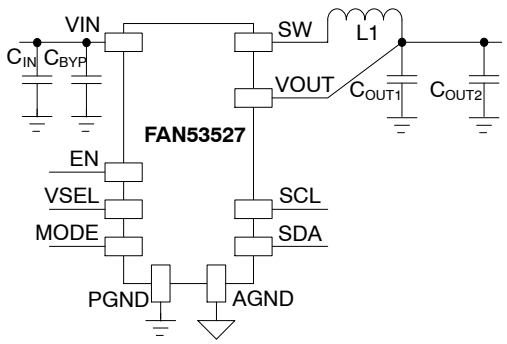


Figure 1. Typical Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Table 1. ORDERING INFORMATION

Part Number	Power−Up Defaults		DVS Range / Step Size	Temperature Range	Package	Packing Method	Device Marking
	VSEL0	VSEL1					
FAN53527UC84X	1.125 V	1.081 V	1.000 V to 1.39375 V / 6.25 mV	−40 to 85°C	WLCSP	Tape & Reel	LQ

Table 2. RECOMMENDED EXTERNAL COMPONENTS

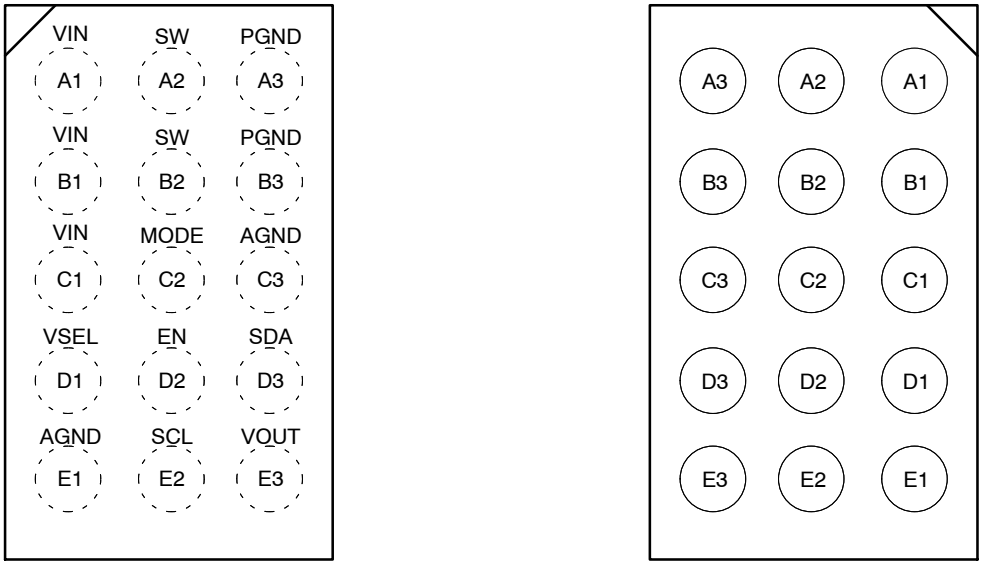
Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
C_{IN}	TDK	C1608X5R1A475K	4.7 μF	0603	10 V
$C_{OUT1/2}$	Murata	GRM188R61A226ME15D	2 x 22 μF	0603/1608 (1.6 mm x 0.8 mm)	10 V
C_{BYP}	Murata	GRM033R60J104KE19D	0.1 μF	0201	6.3 V
L1	Toko	DFE201612E−R47N	0.47 μH ISAT = 6.1 A DCR = 21 mΩ	0805/2012 (2.0 mm x 1.2 mm) Max Height: 0.8 mm	

Table 3. RECOMMENDED ALTERNATE COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
$C_{OUT1/2}$	Murata	GRM188R60J476ME15	2 x 47 μF	0603/1608 (1.6 mm x 0.8 mm)	6.3 V
L1	SEMCO	CLIGT2016URM47MNE	0.47 μH ISAT = 4.0 A DCR = 30 mΩ	2.0 x 1.6 x 1.0 mm	

NOTE: C_{BYP} is optional and used to filter any high frequency component on VIN bus.

PIN CONFIGURATION



Top View

Bottom View

Figure 2. Pin Configuration

Table 4. PIN DEFINITIONS

Pin	Name	Description
A1, B1, C1	VIN	Input Voltage Power input to converter. Place input decoupling capacitor, CIN, as close to this pin as
A2, B2	SW	Switching Node Connect to one side of the inductor.
A3, B3	PGND	Power Ground The low−side MOSFET is referenced to this pin. CIN and COUT should be returned to this pin with minimal path resistance.
C3	AGND	Analog Ground Ground pin for control circuitry.
E2	SCL	Serial Interface Clock I^2C Clock input pin. Avoid routing near noise sensitive traces.
D3	SDA	Serial Interface Data I^2C input/output data line pin. Do not leave this pin floating.
E3	VOUT	Output Voltage Feedback Connect to positive side of output capacitor.
D1	VSEL	Output Voltage Selection Selects between registers VSEL0 or VSEL1 programmed voltages. LOW = VSEL0 and HIGH = VSEL1.
C2	MODE	PFM/PWM MODE Selects between Automatic PFM/PWM (Auto PFM) operation and Forced PWM operation. LOW = Auto PFM/PWM and HIGH = Forced PWM.

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Parameter	Min	Max	Unit
V_{IN}	Voltage on SW, VIN Pins	IC Not Switching	−0.3	7.0	V
		IC Switching	−0.3	5.0	
	Voltage on EN Pin		−0.3	VIN (Note 1)	
	Voltage on All Other Pins	IC Not Switching	−0.3	VIN (Note 1)	
V_{OUT}	Voltage on VOUT Pin		−0.3	5.0	V
V_{INOV_SLEW}	Maximum Slew Rate of V_{IN} > 6.5V, PWM Switching			100	V/ms
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012		2000		V
	Charged Device Model per JESD22−C101		1000		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 7V or V_{IN} + 0.3 V.

Table 6. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Supply Voltage Range	2.5		5.5	V
I_{OUT}	Output Current	0		3.0	A
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 7. THERMAL PROPERTIES

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance		42		°C/W

NOTE: Junction−to−ambient thermal resistance is a function of application and board layout. This data is simulated with four−layer 2s2p boards with vias in accordance to JESD51− JEDEC standard. Special attention must be paid not to exceed the junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Table 8. ELECTRICAL CHARACTERISTICS Minimum and maximum values are at V_{IN} = 3.6 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.6 V, and V_{OUT} = 1.081 V.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES						
I_Q	Quiescent Current	EN Pin = V_{IN}, Auto PFM, No Load		48		μA
		EN Pin = V_{IN}, Forced PWM, No Load		13		mA
I_{SD}	H/W Shutdown Supply Current	EN Pin = GND, SDA/SCL = V_{IN} or GND, 2.5 V ≤ V_{IN} ≤ 5.5 V		0.1	3.0	μA
	Sleep	EN Pin = V_{IN}, [BUCK_ENx] = “0”, SDA/SCL = V_{IN} or GND, 2.5 V ≤ V_{IN} ≤ 5.5 V		0.1	3.0	μA
V_{UVLO}	Under−Voltage Lockout Threshold	V_{IN} Rising		2.32	2.45	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			350		mV
EN, VSEL, MODE, SDA, SCL						
V_{IH}	high−Level Input Voltage	2.5 V ≤ V_{IN} ≤ 5.5 V	1.1			V
V_{IL}	low−Level Input Voltage	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or VIN		0.01	1	μA
V_{OUT} REGULATION						
V_{REG}	Output Voltage Accuracy (Note 2)	Auto PFM, V_{OUT} = 1.0000 to 1.39375 V, I_{OUT} = 0 to 3 A, 2.5 V ≤ V_{IN} ≤ 5.5 V	−2.5		2.5	%
		Forced PWM, V_{OUT} = 1.0000 to 1.39375 V, I_{OUT} = 0 to 3A, 2.5 V ≤ V_{IN} ≤ 5.5 V	−1.5		1.5	
$\Delta V_{OUT} / \Delta I_{LOAD}$	Load Regulation (Note 2)	I_{OUT} = 1 A to 3 A		±0.02		%/A
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation (Note 2)	2.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 A		±0.02		%/V
V_{TRSP}	Transient Response (Note 2)	I_{LOAD} Step 1 mA ⇔ 500 mA, $t_r = t_f$ = 100 ns, Forced PWM		±15		mV
		I_{LOAD} Step 1 mA ⇔ 500 mA, $t_r = t_f$ = 100 ns, Auto PFM		±19		
		I_{LOAD} Step 1 mA ⇔ 3 A, $t_r = t_f$ = 100 ns, Forced PWM		±60		
		I_{LOAD} Step 1 mA ⇔ 3 A, $t_r = t_f$ = 100 ns, Auto PFM		±70		
POWER SWITCH / PROTECTION						
I_{LIMPK}	P−MOS Peak Current Limit		4.00	4.75	5.50	A
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			17		°C
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.15		V
		Falling Threshold	5.50	5.73		
DAC						
	Resolution			7		Bits
	Differential Nonlinearity (Note 2)				0.5	LSB
SOFT−START						
t_{SS}	Regulator Enable to Regulated V_{OUT}	R_{LOAD} > 5Ω, From EN Rising Edge to 95% V_{OUT} and C_{OUT} = 2x22 μF		75		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by Design. Characterized on the ATE or Bench.

Table 9. I²C TIMING SPECIFICATIONS Minimum and maximum values are at V_{IN} = 3.6 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.6 V, and V_{OUT} = 1.081 V. Guaranteed by Design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES						
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High−Speed Mode, $C_B \le 100$ pF			3400	
		High−Speed Mode, $C_B \le 400$ pF			1700	
t_{BUF}	Bus−Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
$t_{HD;STA}$	START or REPEATED START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		
		High−Speed Mode		160		
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
		High−Speed Mode, $C_B \le 100$ pF		160		ns
		High−Speed Mode, $C_B \le 400$ pF		320		
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		
		High−Speed Mode, $C_B \le 100$ pF		60		
		High−Speed Mode, $C_B \le 400$ pF		120		
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		
		High−Speed Mode		160		
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High−Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		Fast Mode Plus	0		450	
		High−Speed Mode, $C_B \le 100$ pF	0		70	
		High−Speed Mode, $C_B \le 400$ pF	0		150	
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, $C_B \le 100$ pF		10	80	
		High−Speed Mode, $C_B \le 400$ pF		20	160	

Table 9. I²C TIMING SPECIFICATIONS Minimum and maximum values are at V_{IN} = 3.6 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.6 V, and V_{OUT} = 1.081 V. Guaranteed by Design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POWER SUPPLIES						
t_{FCL}	SCL Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	40	
		High−Speed Mode, $C_B \le 400$ pF		20	80	
t_{RCL1}	Rise Time of SCL After a REPEATED START Condition and After ACK Bit	High−Speed Mode, $C_B \le 100$ pF		10	80	ns
		High−Speed Mode, $C_B \le 400$ pF		20	160	
t_{RDA}	SDA Rise Time	Standard Mode		$20+0.1C_B$	1000	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	80	
		High−Speed Mode, $C_B \le 400$ pF		20	160	
t_{FDA}	SDA Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		Fast Mode Plus		$20+0.1C_B$	120	
		High−Speed Mode, $C_B \le 100$ pF		10	80	
		High−Speed Mode, $C_B \le 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		
		High−Speed Mode		160		
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

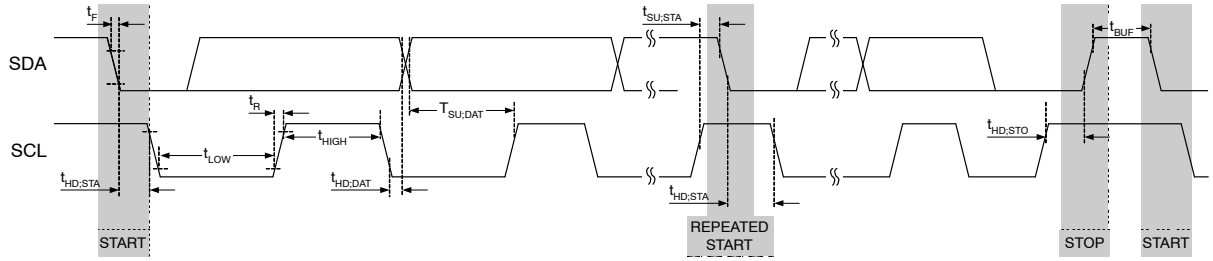
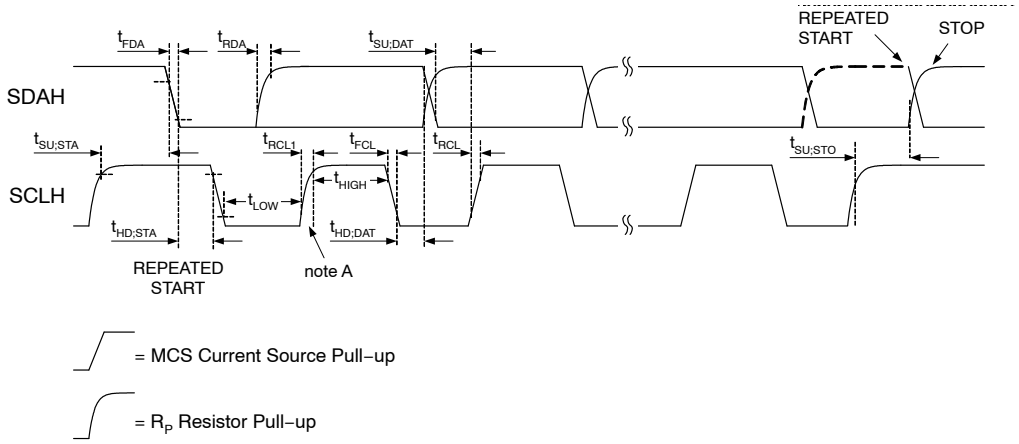


Figure 3. I²C Interface Timing for Fast Plus, Fast, and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 4. I²C Interface Timing for High−Speed Mode

TYPICAL CHARACTERISTICS

Unless otherwise specified; circuit per Typical Application using Recommended External Components,
T_A = 25°C, V_{IN} = 3.6 V, V_{OUT} = 1.081 V, Auto PFM Mode

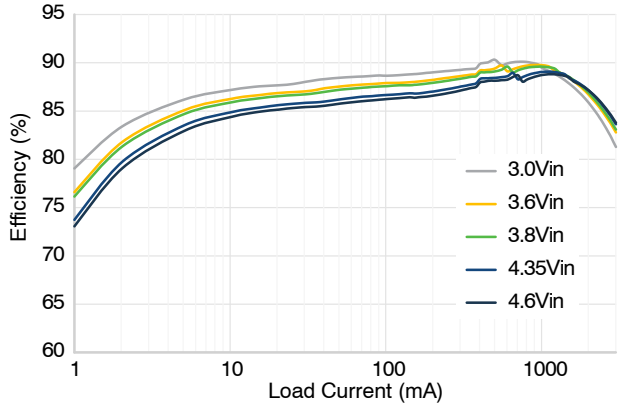


Figure 5. Efficiency versus Load Current and Input Voltage

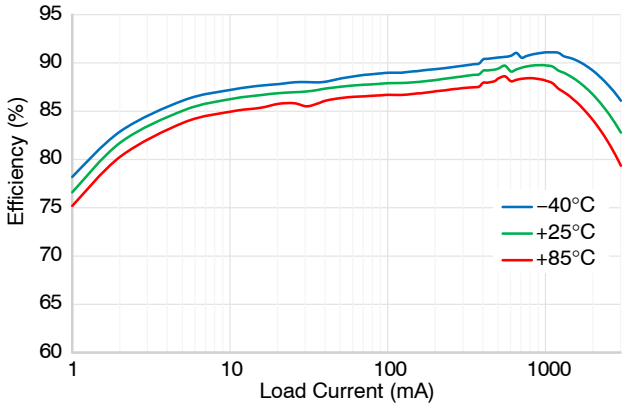


Figure 6. Efficiency versus Load Current and Temperature

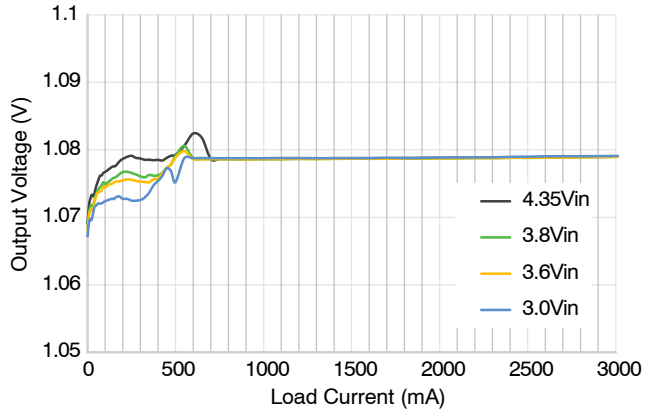


Figure 7. Output regulation versus Load Current and Input Voltage

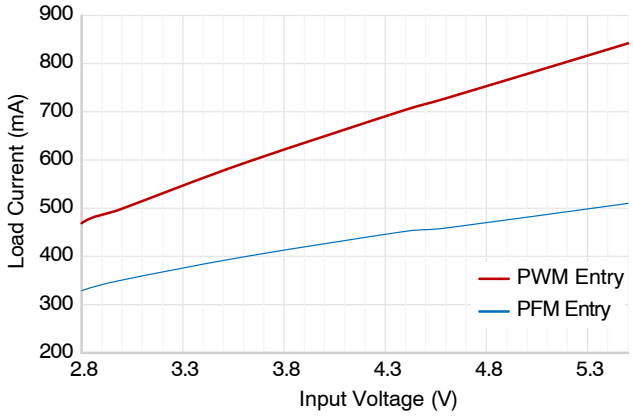


Figure 8. PWM/PFM Entry Level versus Input Voltage

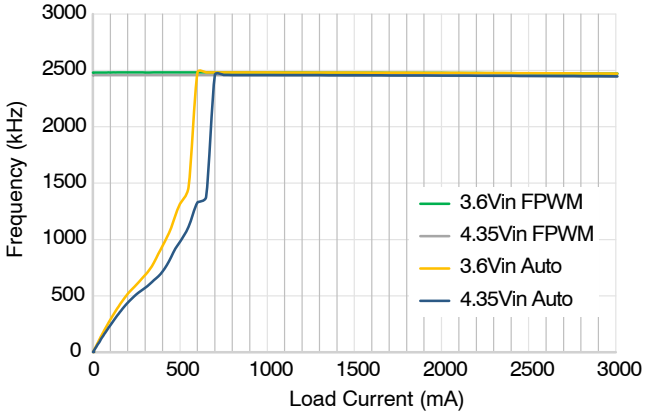


Figure 9. Frequency versus Load Current versus Auto PFM and Forced PWM

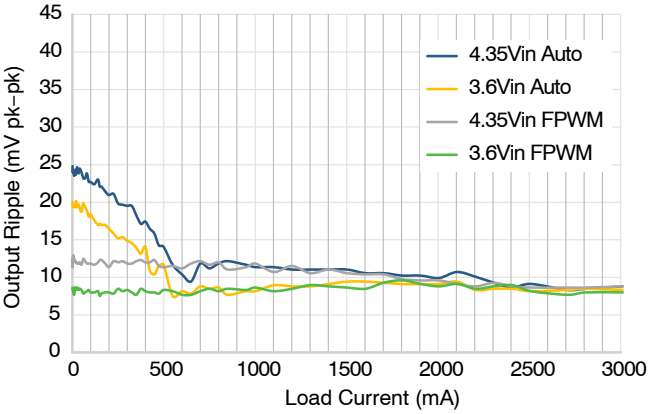


Figure 10. Output Ripple versus Load Current versus Auto PFM and Forced PWM

TYPICAL CHARACTERISTICS

Unless otherwise specified; circuit per Typical Application using Recommended External Components,
T_A = 25°C, V_{IN} = 3.6 V, V_{OUT} = 1.081 V, Auto PFM Mode

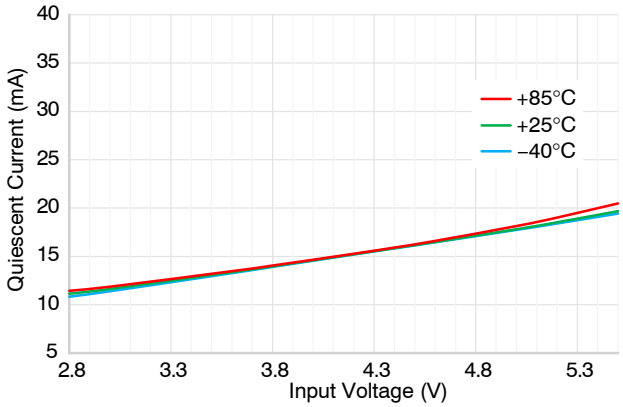


Figure 11. Quiescent Current versus Input Voltage and Temperature in Forced PWM

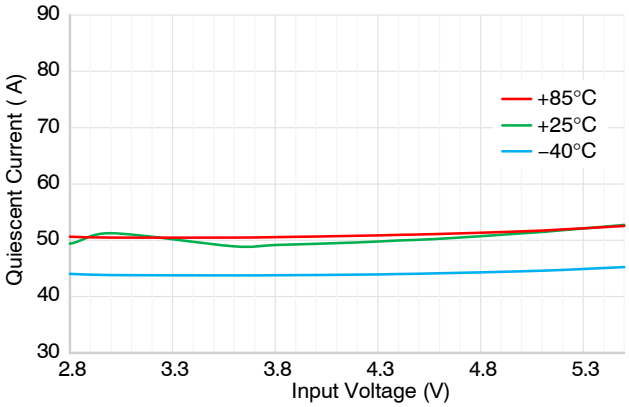


Figure 12. Quiescent Current versus Input Voltage and Temperature in Auto PFM

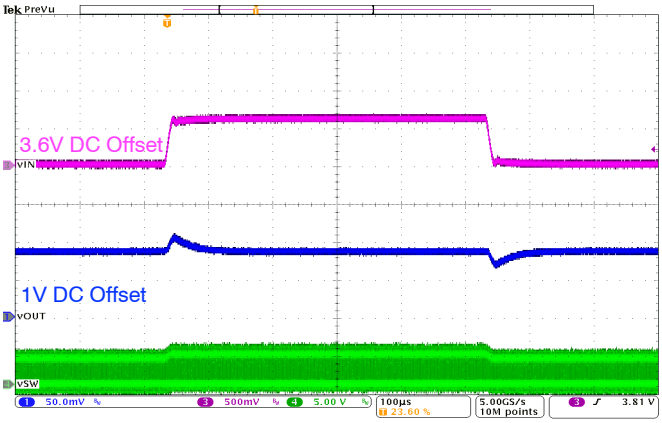


Figure 13. Line Transient, 3.6 V↔4.2 V, 1A, 10 μs Edge

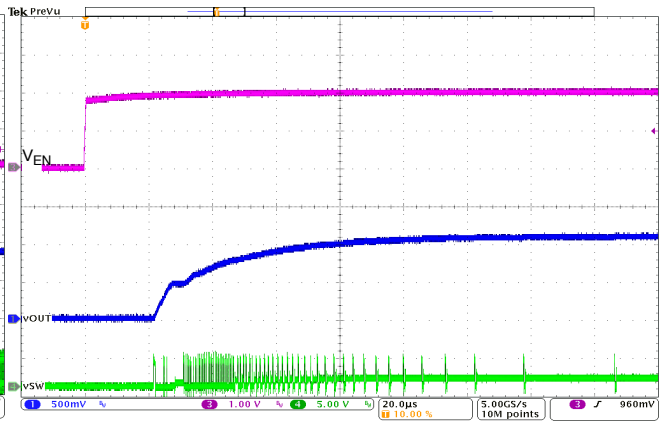


Figure 14. Start−Up into 5.4 kΩ Load

TYPICAL CHARACTERISTICS

Unless otherwise specified; circuit per Typical Application using Recommended External Components,
T_A = 25°C, V_{IN} = 3.6 V, V_{OUT} = 1.081 V, Auto PFM Mode

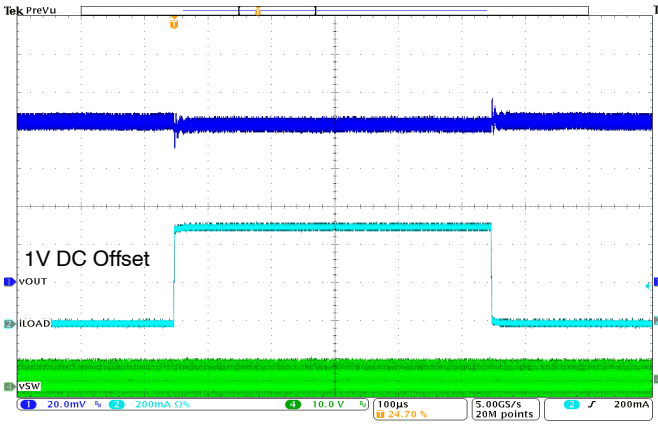


Figure 15. Load Transient, 1 mA↔500 mA, 100 ns Edge, Forced PWM

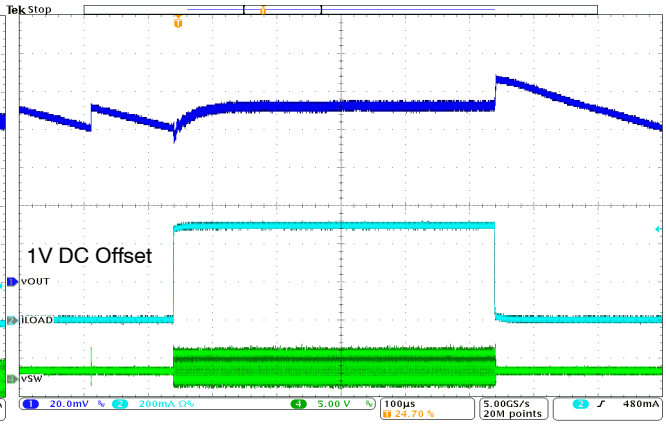


Figure 16. Load Transient, 1 mA↔500 mA, 100 ns Edge, Auto PFM

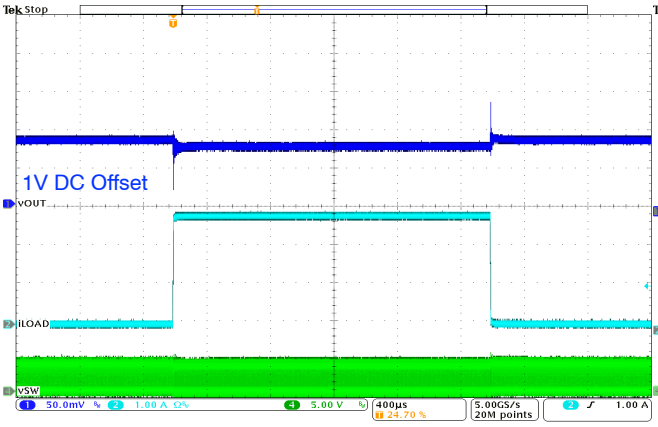


Figure 17. Load Transient, 1 mA↔3 A, 100 ns Edge, Forced PWM

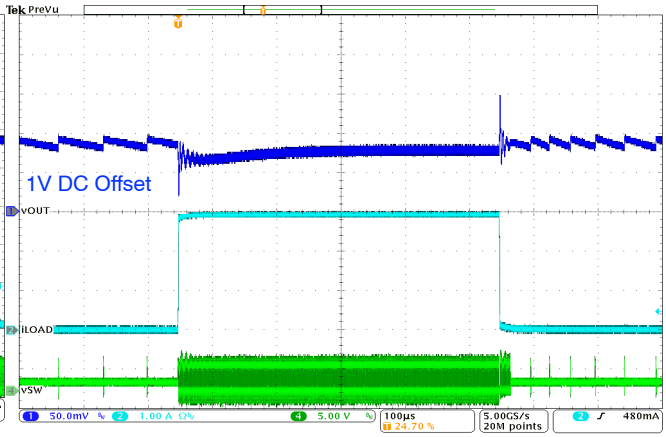


Figure 18. Load Transient, 1 mA↔3 A, 100 ns Edge, Auto PFM

Operating Description

The FAN53527 is a step−down switching voltage regulator that delivers a programmable output voltage from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53527 is capable of delivering 3.0 A at over 80% efficiency. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 330 nH or 470 nH for the output inductor and 44 μF for the output capacitor. High efficiency is maintained at light load with single−pulse PFM.

An I^2C−compatible interface allows transfers up to 3.4 Mbps. This communication interface can be used to:

- Dynamically re−program the output voltage in 6.25 mV increments;
- Reprogram the mode to enable or disable PFM;
- Control voltage transition slew rate; or
- Enable / disable the regulator

Control Scheme

The FAN53527 uses a proprietary non−linear, fixed−frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53527 operates in Discontinuous Current Mode (DCM) single−pulse PFM, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and CCM Modes.

PFM can be disabled by programming the MODE bits in the CONTROL register in combination with the state of the VSEL pin or simply by setting the MODE pin high. See Table 2.

Enable and Soft−Start

When the EN pin is LOW; the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, I^2C can be written to or read from as long as input voltage is above the UVLO. The registers keep the content when the EN pin is LOW. The registers are reset to default values during a Power On Reset (POR). When the OUTPUT_DISCHARGE bit in the Control register is enabled (logic HIGH) and the EN pin is LOW or the BUCK_ENx bit is LOW, an 11 W load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft−start cycle. During soft−start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited, allowing the IC to start into a pre−charged capacitive load.

If large values of output capacitance are used, the regulator may fail to start. The maximum C_{OUT} capacitance for starting with a heavy constant−current load is approximately:

$$C_{OUTMAX} \approx (I_{LMPK} - I_{LOAD}) \cdot \frac{320\mu}{V_{OUT}} \quad \text{(eq. 1)}$$

where C_{OUTMAX} is expressed in μF and I_{LOAD} is the load current during soft−start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters tri−state before reattempting soft−start 1700 μs later. This limits the duty cycle of full output current during soft−start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both set to "1" by default. These options start after a POR, regardless of the state of the VSEL pin.

Table 10. HARDWARE AND SOFTWARE ENABLE

Control Pins			BUCK_ENx Bits				
EN	VSEL	MODE	BUCK_EN0	BUCK_EN1	Mode Bits	Operation	V_{OUT}
0	X	X	X	X	XX	Shutdown	N/A
1	X	X	0	0	XX	Shutdown	N/A
1	0	0	1	X	X0	Auto PFM	NSEL0
1	0	0	1	X	X1	Forced PWM	NSEL0
1	1	0	X	1	0X	Auto PFM	NSEL1
1	1	0	X	1	1X	Forced PWM	NSEL1
1	0	X	0	X	XX	Shutdown	N/A
1	0	1	1	X	XX	Forced PWM	NSEL0
1	1	X	X	0	XX	Shutdown	N/A
1	1	1	X	1	XX	Forced PWM	NSEL1

VSEL Pin and I²C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output is given as:

$$V_{OUT} = 1.000\ V + \left[(NSELx - 64) \cdot 6.25\ mV\right] \quad \text{(eq. 2)}$$

For example, if NSEL =1010000 (80 decimal), then V_{OUT} = 1.000 + 0.100 = 1.100 V.

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages, as shown in Table 1.

Transition Slew Rate Limiting

When transitioning from a low to high voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the Control register, as shown in the table below.

Table 11. TRANSITION SLEW RATE

Decimal	Bin	Slew Rate	
0	000	64.00	mV/μs
1	001	32.00	mV/μs
2	010	16.00	mV/μs
3	011	8.00	mV/μs
4	100	4.00	mV/μs
5	101	2.00	mV/μs
6	110	1.00	mV/μs
7	111	0.50	mV/μs

Transitions from high to low voltage rely on the output load to discharge V_{OUT} to the new set point. Once the high−to−low transition begins, the IC stops switching until V_{OUT} has reached the new set point.

Under−Voltage Lockout (UVLO)

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage rises HIGH enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

Input Over−Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (~ 6.2 V), the IC stops switching to protect the circuitry from internal spikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. 16 consecutive current limit cycles in current limit, cause the regulator to shut down and stay off for about 1700 μs before attempting a restart.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 17°C hysteresis.

Monitor Register (Reg05)

The Monitor register indicates of the regulation state of the IC. If the IC is enabled and is regulating, its value is (1000 0001).

I²C Interface

The serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I²C Bus® specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

I²C Slave Address

The slave address uses the standard 7 most significant bits for defining the address and the LSB as the read/write bit. In doing so, the first word consists of bit [7:5] and the second word utilizes bits [4:1]. Thus the slave address is 60. Other slave addresses can be assigned. Contact an On Semiconductor representative.

Table 12. I²C SLAVE ADDRESS

Address	Bits							
	7	6	5	4	3	2	1	0
60	1	1	0	0	0	0	0	X

Other slave addresses can be assigned. Contact an ON Semiconductor representative.

Bus Timing

As shown in Figure 19 data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow sufficient time for the data to set up before the next SCL rising edge.

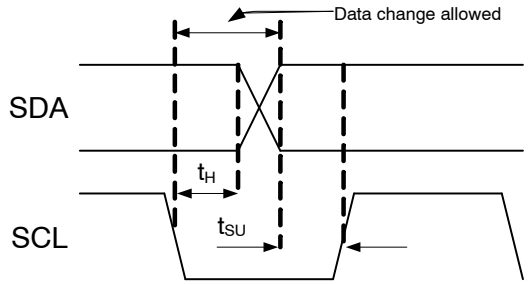


Figure 19. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 20.

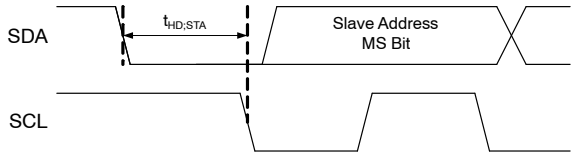


Figure 20. START Bit

A transaction ends with a STOP condition, defined as SDA transitioning from 0 to 1 with SCL high, as shown in Figure 21.

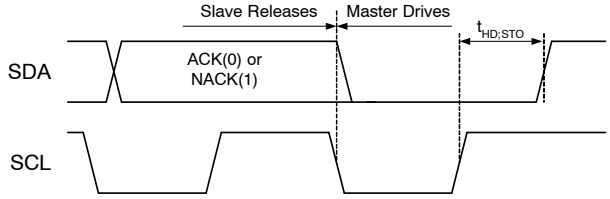


Figure 21. STOP Bit

During a read from the FAN53527, the master issues a REPEATED START after sending the register address and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 22.

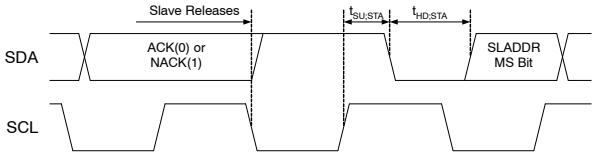


Figure 22. REPEATED START Timing

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical; except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition (Figure 20). The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 22) that causes all slaves on the bus to switch to HS Mode. The master then sends I^2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 21) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 22).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as:

- Master Drives Bus and
- Slave Drives Bus

All addresses and data are MSB first.

Table 13. I^2C BIT DEFINITIONS FOR FIGURE 23 AND FIGURE 24

Symbol	Definition
S	START, see Figure 20
P	STOP, see Figure 21
R	REPEATED START, see Figure 22
A	ACK. The slave drives SDA to 0 acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.

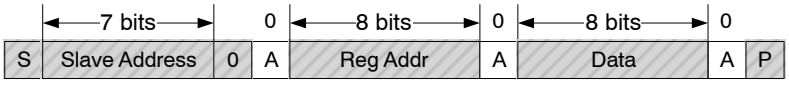


Figure 23. Write Transaction

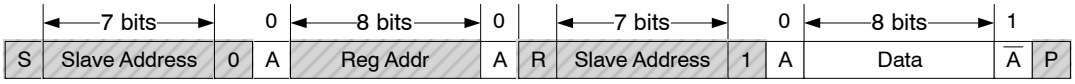


Figure 24. Write Transaction Followed by a Read Transaction

REGISTER DESCRIPTION

Table 14. REGISTER MAP

Hex Address	Name	Function	Default
00	VSEL0	Controls V_{OUT} settings when VSEL pin = LOW	11010100
01	VSEL1	Controls V_{OUT} settings when VSEL pin = HIGH	11001101
02	CONTROL	Determines whether V_{OUT} output discharge is enabled and also the slew rate of positive transitions	10000000
03	ID1	Read−only register identifies vendor and chip type	10000101
04	ID2	Read−only register identifies die revision	00000000
05	MONITOR	Indicates device status	00000000

Table 15. BIT DEFINITIONS

Bit	Name	Type	Default	Description
VSEL0				**Register Address: 00**
7	BUCK_EN0	**R/W**	1	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6:0	NSEL0	**R/W**	1010100	Sets the V_{OUT} value for VSEL0 setting. V_{OUT} = 1.000 + 6.25 mV * (d−64); where d is the decimal value of NSEL0 from 64 to 255.
VSEL1				**Register Address: 01**
7	BUCK_EN1	**R/W**	1	Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent.
6:0	NSEL1	**R/W**	1001101	Sets the V_{OUT} value for VSEL1 setting. V_{OUT} = 1.000 + 6.25 mV * (d−64); where d is the decimal value of NSEL1 from 64 to 255.
CONTROL				**Register Address: 02**
7	OUTPUT_ DISCHARGE	**R/W**	0	The internal pull−down is not enabled when the converter is disabled
			1	The internal pull−down will be activated when the converter is disabled
6:4	SLEW	**R/W**	000	Sets the slew rate for positive voltage transitions. Refer to the Transition Slew Rate Limiting section for details.
3	Reserved		0	Always reads back 0.
2	RESET	**R/W**	0	Setting to 1 resets all registers to default values. Always reads back 0.
1:0	MODE	**R/W**	00	In combination with the VSEL and MODE pin, the MODE bits configure the buck to operate in either Auto PFM or Forced PWM Mode. The bits are don't−care if the Mode pin is high. Refer to the Hardware and Software Enable table for details.
ID1				**Register Address: 03**
7:5	VENDOR	**R**	100	Signifies On Semiconductor as the IC vendor.
4	Reserved	**R**	0	Always reads back 0.
3:0	DIE_ID	**R**	0101	DIE ID − FAN53527
ID2				**Register Address: 04**
7:4	Reserved	**R**	0000	Always reads back 0000
3:0	DIE_REV	**R**	0000	FAN53527 Die Revision
MONITOR				**Register Address: 05**
7	PGOOD	**R**	0	1: Buck is enabled and soft−start is completed.

Table 15. BIT DEFINITIONS

Bit	Name	Type	Default	Description
MONITOR				**Register Address: 05**
6	UVLO	**R**	0	1: Signifies VIN is less than the UVLO threshold.
5	OVP	**R**	0	1: Signifies VIN is greater than the OVP threshold.
4	POS	**R**	0	1: Signifies a positive voltage transition is in progress and the output voltage has not yet reached its new setpoint. This bit is set to “1” during IC soft−start.
3	NEG	**R**	0	1: Signifies a negative voltage transition is in progress and the output voltage has not yet reached its new setpoint. This bit is set to “1” during IC soft−start.
2	RESET−STAT	**R**	0	1: Indicates that a register reset was performed. This bit is cleared after register 5 is read.
1	OT	**R**	0	1: Signifies the thermal shutdown is active.
0	BUCK_STATUS	**R**	0	1: Buck enabled; 0 buck disabled.

APPLICATION INFORMATION

Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}}\right) \quad \text{(eq. 3)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad \text{(eq. 4)}$$

The FAN53527 is optimized for operation with L = 470 nH, but is stable with inductances up to 1.0 μH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so decreases the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin−effect losses:

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{2} + \frac{\Delta I^2}{12}} \quad \text{(eq. 5)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs and the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs and the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Inductor Current Rating

The current-limit circuit can allow substantial peak currents to flow through L1 under worst−case conditions. If it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

Output Capacitor and V_{OUT} Ripple

Increasing C_{OUT} has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is calculated by:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right] \quad \text{(eq. 6)}$$

where C_{OUT} is the effective output capacitance.

The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT}. Equation 6 is only valid for CCM operation, which occurs in PWM Mode.

The FAN53527 can be used with either 2 x 22 μF (0603) or 2 x 47 μF (0603) output capacitor configuration. If a tighter ripple and transient specification is need from the FAN53527, then the 2 x 47 μF is recommended.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the

square−wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square−wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \cdot \frac{ESL_{COUT}}{L1} \quad \text{(eq. 7)}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value.

To minimize ESL, use capacitors with the lowest ratio of length to width. Placing additional small−value capacitors near the load also reduces the high−frequency ripple components.

Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN and PGND pins to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between CIN and the power source lead to reduce under−damped ringing that can occur between the inductance of the power source leads and C_{IN}.

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction−to−ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53527, θ_{JA} is 42°C/W when mounted on its four−layer with vias evaluation board in still air with 2 oz. outer layer copper weight and 1 oz. inner layer.

For long−term reliable operation, the junction temperature (T_J) should be maintained below 125°C.

To calculate maximum operating temperature (<125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN}, V_{OUT}, and load conditions.
2. Calculate total power dissipation using:

$$P_T = V_{OUT} \cdot I_{LOAD} \cdot \left(\frac{1}{\eta} - 1\right) \quad \text{(eq. 8)}$$

3. Estimate inductor copper losses using:

$$P_L = I_{LOAD}^2 \cdot DCR_L \quad \text{(eq. 9)}$$

4. Determine IC losses by removing inductor losses (step 3) from total dissipation:

$$P_{IC} = P_T - P_L \quad \text{(eq. 10)}$$

5. Determine device operating temperature:

$$\Delta T = P_{IC} \cdot \Theta_{JA} \quad T_{IC} = T_A + \Delta T \quad \text{(eq. 11)}$$

and

Note that the $R_{DS(ON)}$ of the power MOSFETs increases linearly with temperature at about 1.4%/°C. This causes the efficiency (η) to degrade with increasing die temperature.

Layout Recommendations

1. The input capacitor (C_{IN}) should be connected as close as possible to the VIN and GND pins. Connect to VIN and GND using only top metal. Do not route through vias.
2. Place the inductor (L) as close as possible to the IC. Use short wide traces for the main current paths.
3. The output capacitor (C_{OUT}) should be as close as possible to the IC. Connection to GND should be on top metal. Feedback signal connection to VOUT should be routed away from noisy components and traces (e.g. SW line). For remote sensing application, place one or all output capacitors near the load and if there are also output capacitors placed near the inductor, the maximum trace resistance between the inductor and the load should not exceed 30 mΩ.

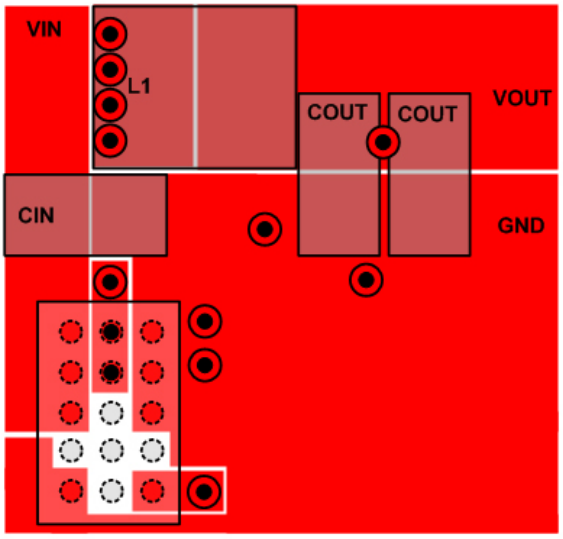


Figure 25. TOP Layer (component side)

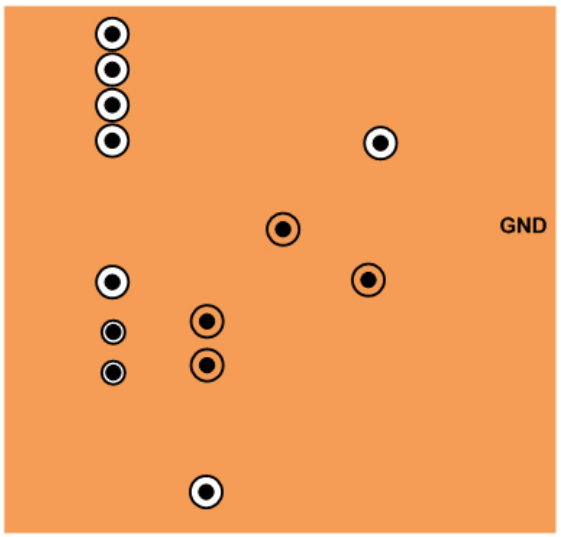


Figure 26. Mid−Layer 1

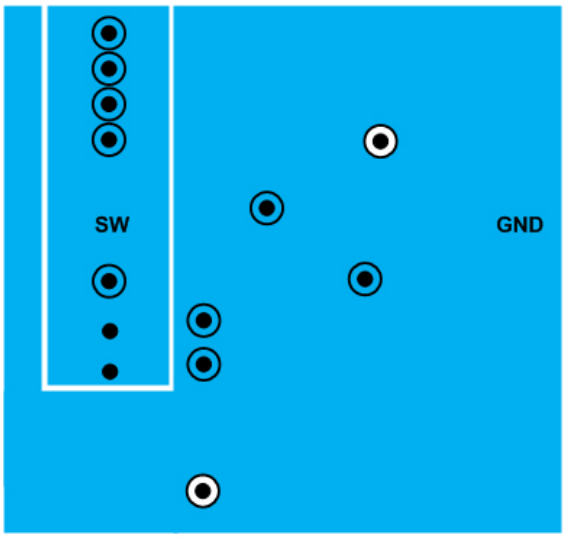


Figure 27. Mid−Layer 2

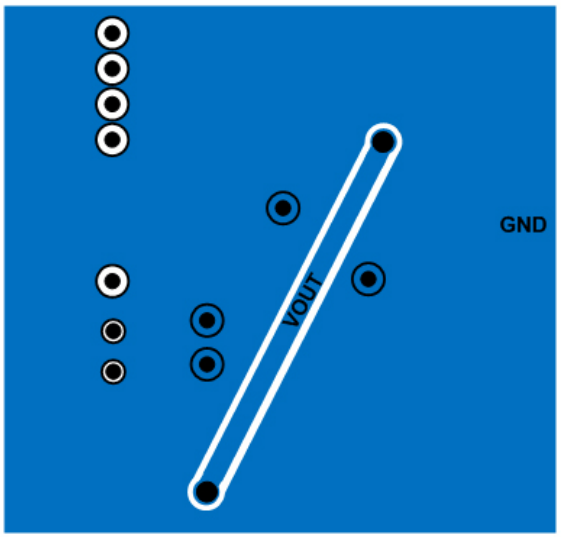


Figure 28. BOTTOM Layer

REMOTE SENSING

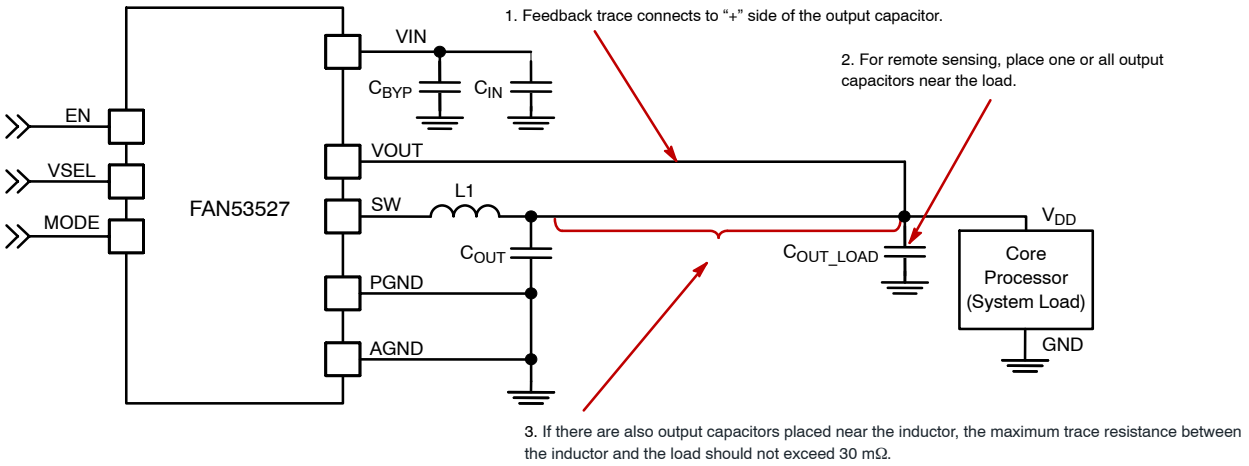


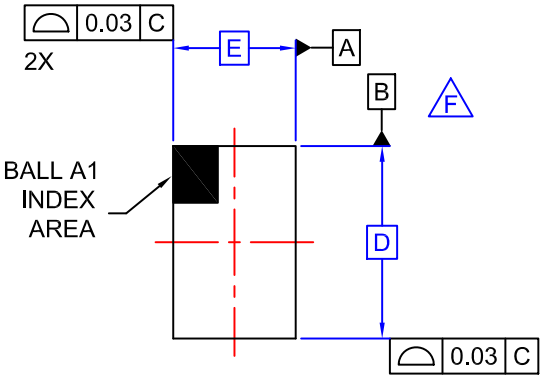
Figure 29. Remote Sensing Schematic

Table 16. PRODUCT SPECIFIC DIMENSIONS

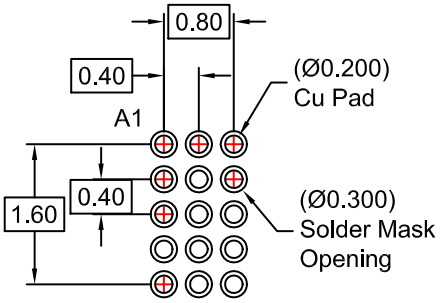
D	E	X	Y
2.015 0 ± 03 mm	1.310 ± 0.03 mm	0.255 mm	0.2075 mm

WLCSP15 2.015x1.31x0.586
CASE 567QS
ISSUE O

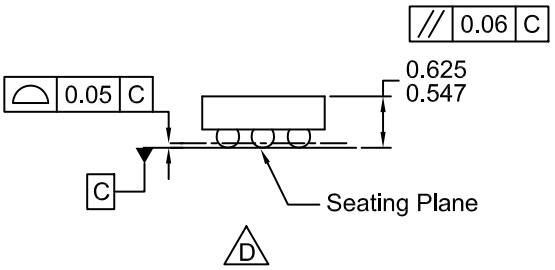
DATE 31 OCT 2016

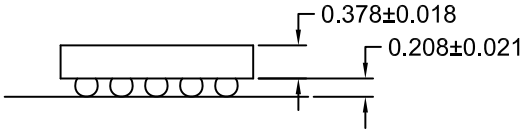


TOP VIEW

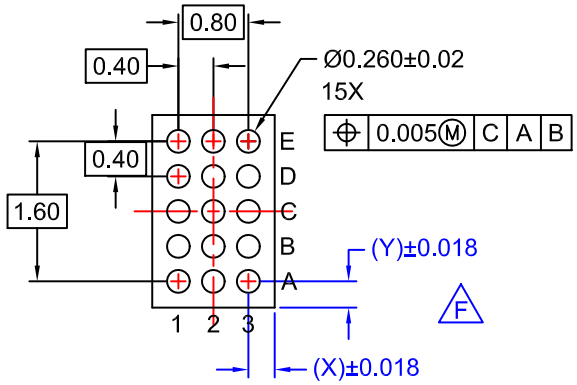


RECOMMENDED LAND PATTERN
(NSMD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASME Y14.5 - 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

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