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FAIRCHILD SEMICONDUCTOR®

May 2013

FAN5421 — Single-Cell Li-Ion Switching Charger

Features

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: ±0.5% at 25°C
  ±1% from 0 to 125°C
- ±5% Charge Current Regulation Accuracy
- 20 V Absolute Maximum Input Voltage
- 6.8 V Maximum Input Operating Voltage
- 1.5 A Maximum Charge Rate
- Charge and Mode Programmable through High-Speed I^2C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility
  - Fast Charge / Termination Current
  - Charger Voltage
  - Safety Timer
  - Termination Enable
- 3 MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small-Footprint, 1µH External Inductor
- Safety Timer with Reset Control
- Low Reverse Leakage to Prevent Battery Drain to VIN

Applications

- Cell Phones, Smart Phones, PDAs
- Digital Cameras
- Portable Media Players

Description

The FAN5421 is a highly integrated switched-mode charger that minimizes single-cell Li-Ion charging time.

The charging parameters and operating modes are programmable through an I^2C interface that operates up to 3.4 Mbps. The charger circuit switches at 3 MHz to minimize the size of external passive components.

The FAN5421 provides battery charging in three phases: conditioning, constant current, and constant voltage.

Charge termination is determined by a programmable minimum current level. A safety timer with reset control provides a safety backup for the I^2C host.

The IC automatically adapts to current-limited power sources by reducing the charge current to keep the input supply above a programmed voltage (default 4.52 V).

The IC automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode with leakage from the battery to the input prevented. Charge status is reported back to the host through the I^2C port. Charge current is reduced when the die temperature reaches 120°C.

The FAN5421 is available in a 1.96 x 1.87 mm, 20-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

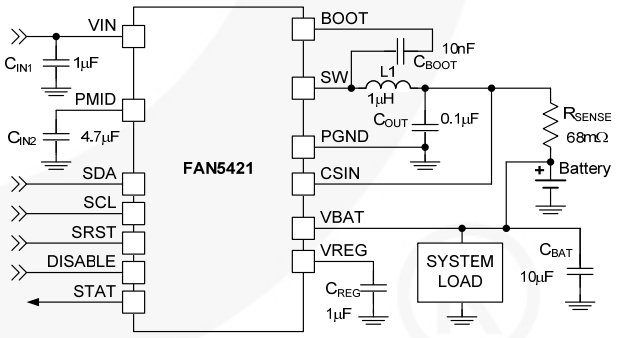


Figure 1. Typical Application

Table 1. Ordering Information

Part Number	Temperature Range	Package	PN Bits: IC_INFO[4:3]	Packing
FAN5421BUCX(1)	-40 to 85°C	WLCSP-20, 0.4 mm Pitch	00	Tape and Reel

Note:
1. Includes backside laminate

Block Diagram

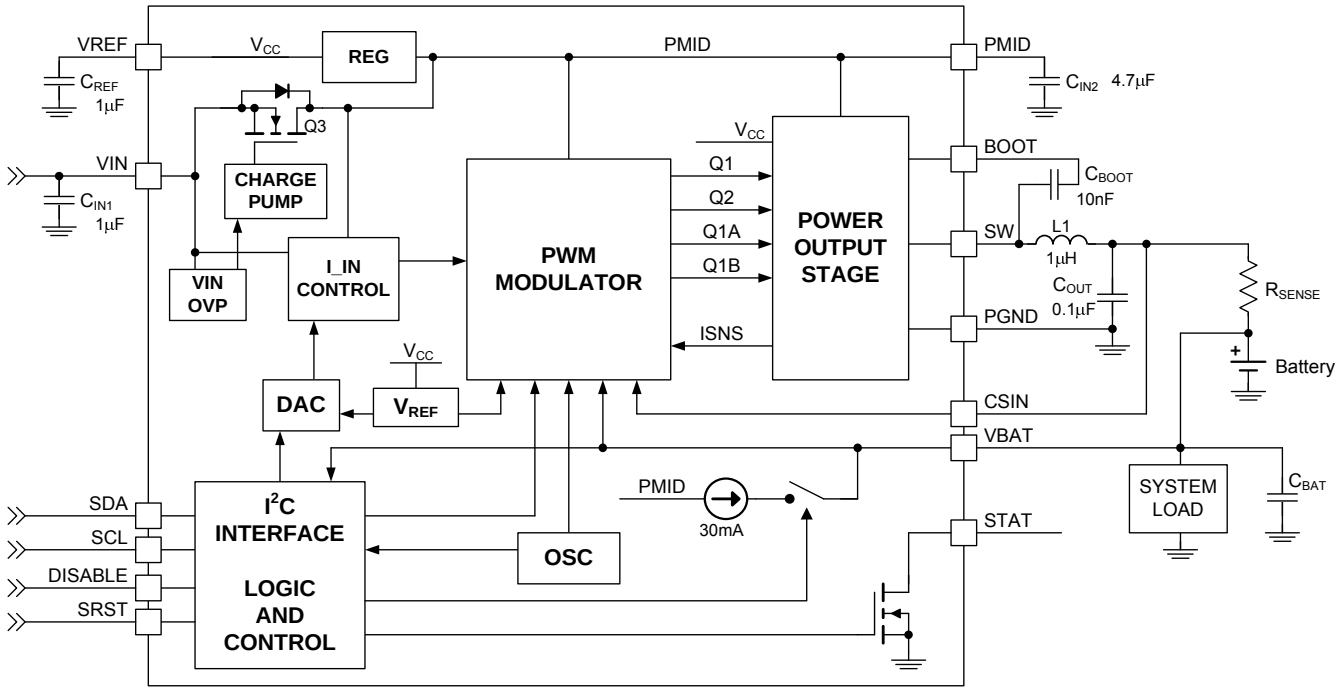


Figure 2. IC and System Block Diagram

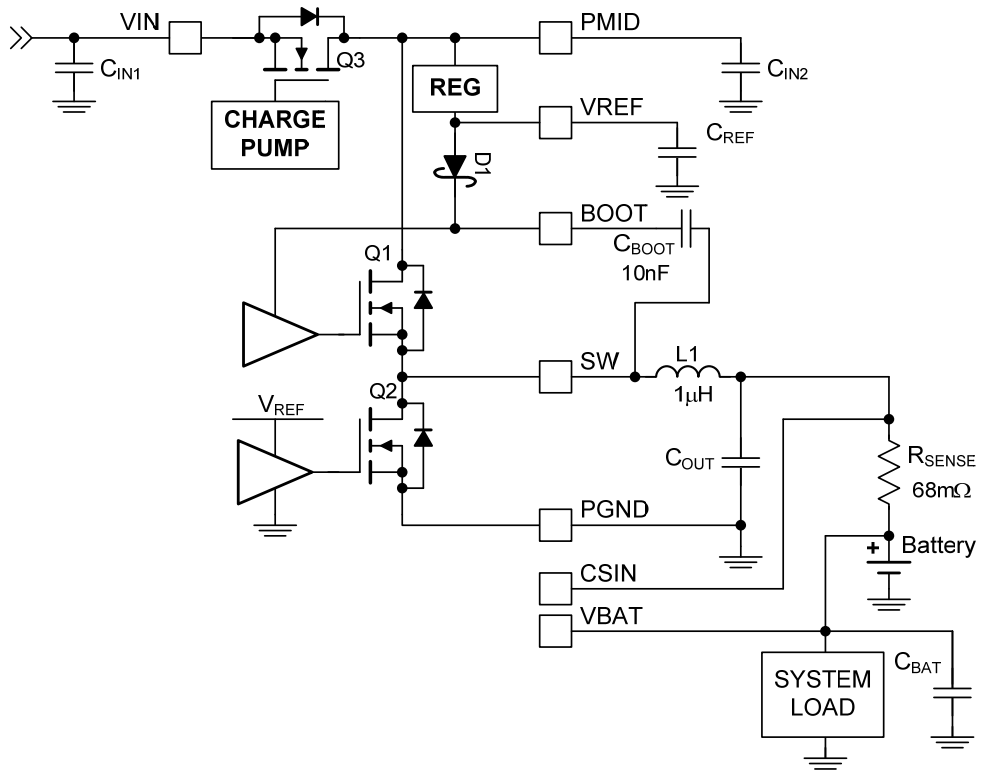


Figure 3. Power Output

Table 2. Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Units
L1	1 µH ±20%, 1.6 A DCR = 55 mΩ, 2520	Murata: LQM2HPN1R0	L	1.0	µH
	1 µH ±30%, 1.4 A DCR = 85 mΩ, 2016	Murata: LQM2MPN1R0			
C_{IN1}	1.0 µF, 10%, 25 V, X5R, 0603	Murata GRM188R61E105K TDK:C1608X5R1E105M	C	1.0	µF
C_{IN2}	4.7 µF, 10%, 25 V, X5R, 0805	Murata: GRM21BR61E475K TDK: C2012X5R1E475K	C	4.7	µF
C_{BAT}	10 µF, 20%, 6.3 V, X5R, 0603	Murata: GRM188R60J106M TDK: C1608X5R0J106M	C	10.0	µF
C_{OUT}	0.1 µF, 10%, 6.3 V, X5R, 0402	Any	C	0.1	µF
C_{BOOT}	10 nF, 10%, 6.3 V, X5R, 0402	Any	C	1.0	nF
C_{REF}	1 µF, 10%, 6.3 V, X5R, 0402	Any	C	1.0	µF

Pin Configuration

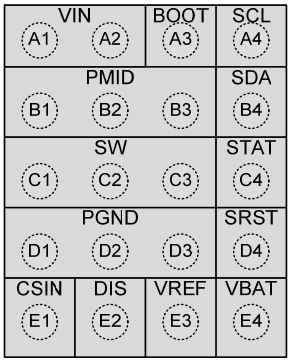


Figure 4. Top View

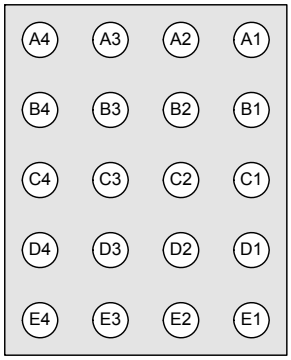


Figure 5. Bottom View

Pin Definitions

Pin #	Name	Description
A1, A2	VIN	**Charger Input Voltage**. Bypass with a 1 μF capacitor to PGND.
A3	BOOT	**BOOT**. High-side NMOS driver supply. Connect a 10nF capacitor from SW to this pin.
A4	SCL	**SCL**. I^2C interface serial clock. This pin should not be left floating.
B1-B3	PMID	**Power Input Voltage**. Power input to the charger regulator, bypass point for the high-voltage input switch. Bypass with a minimum of 4.7 μF capacitor to PGND.
B4	SDA	**SDA**. I^2C interface serial data. This pin should not be left floating.
C1-C3	SW	**Switching Node**. Connect to output inductor.
C4	STAT	**Status**. Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in process.
D1-D3	PGND	**Power GND**. Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{IN2} should be as short as possible.
D4	SRST	**Safety Reset**. When LOW, this pin resets the safety register to its default values. When HIGH, the safety register is reset when V_{BAT} drops below V_{SHORT}.
E1	CSIN	**Current Sense Input**. Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 μF capacitor to PGND.
E2	DIS	**Charge Disable**. If this pin is HIGH, charging is disabled. When LOW, charging is controlled by the I^2C registers. When this pin is HIGH, the 15-minute timer is reset; it does not affect the 32-second timer.
E3	VREF	**Bias Regulator Output**. Connect to a 1 μF capacitor to PGND. This pin supplies the internal gate drive and power supply to the IC while charging. Up to 1 mA of current can be provided from this pin to drive the external circuits.
E4	VBAT	**Battery Voltage**. Connect to the positive (+) terminal of the battery pack. Bypass with a minimum of 10 μF to PGND.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	VIN Voltage	Continuous	–1.4	20.0	V
		Pulsed, 100 ms Maximum, Non-Repetitive	–2.0	20.0	V
V_{STAT}	STAT Voltage		–0.3	20.0	V
V_I	PMID		–0.3	20.0	V
	CSIN, VBAT, DISABLE		–0.3	7.0	
V_O	Other Pins		–0.3	6.5[2]	V
$\frac{dV_{IN}}{dt}$	Maximum Rate of V_{IN} Increase Above 10 V When IC Enabled			4	V/µs
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2.5		kV
		Charged Device Model per JESD22-C101	1.0		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
2. Lesser of 6.5 V or V_{IN} + 0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	4.0	6.8	V
T_A	Ambient Temperature	–30	+85	°C
T_J	Junction Temperature	–30	+120	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature, T_A.

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	60	°C/W
θ_{JB}	Junction-to-PCB Thermal Resistance	20	°C/W

Electrical Specifications

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{IN} = 5.0 V, CE# = HZ_MODE = 0, (Charger Mode operation). SCL, SDA, and SRST = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
I_{VIN}	VIN Current	$V_{IN} > V_{IN(min)}$, PWM Switching		40		mA
		$V_{IN} > V_{IN(min)}$, PWM Not Switching		300		µA
		0°C < T_J < 85°C, HZ_MODE = 1, $V_{BAT} > V_{LOWV}$		300		µA
I_{LKG}	VBAT to VIN Leakage Current	0°C < T_J < 85°C, HZ_MODE = 1, V_{BAT} = 4.2 V			5	µA
I_{BAT}	Battery Discharge Current in High-Z Mode	0°C < T_J < 85°C, HZ_MODE = 1, V_{BAT} = 4.2 V			20	µA
		DISABLE = 1, 0°C < T_J < 85°C, V_{BAT} = 4.2 V			10	µA
Charger Voltage Regulation						
V_{OREG}	Charge Voltage Range		3.5		4.4	V
	Charge Voltage Accuracy	T_A = 25°C, <95% Duty Cycle	–0.5		+0.5	%
		T_J = 0 to 125°C, <95% Duty Cycle	–1		+1	
Charging Current Regulation						
I_{OCHRG}	Output Charge Current Range	$V_{LOWV} < V_{BAT} < V_{OREG}$, $V_{IN} > V_{SLP}$, R_{SENSE} = 68 mΩ, <95% Duty Cycle	550		1550	mA
	Charge Current Accuracy Across R_{SENSE}	20 mV ≤ V_{RSENSE} ≤ 40 mV	92	97	102	% of Setting
		V_{RSENSE} > 40 mV	94	97	100	
Weak Battery Detection						
V_{LOWV}	Weak Battery Threshold Range		3.4		3.7	V
	Weak Battery Threshold Accuracy	V_{BAT} Falling	–5		+5	%
	Weak Battery Deglitch Time	Rising Voltage, 2mV Overdrive		30		ms
Logic Levels: DISABLE, SDA, SCL, SRST						
V_{IH}	HIGH-Level Input Voltage		1.05			V
V_{IL}	LOW-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{IN}		0.01	1.00	µA
Charge Termination Detection						
$I_{(TERM)}$	Termination Current Range	$V_{BAT} > V_{OREG} – V_{RCH}$, $V_{IN} > V_{SLP}$, R_{SENSE} = 68 mΩ	50		400	mA
	Termination Current Accuracy Across R_{SENSE}	[$V_{CSIN} – V_{BAT}$] from 3 mV to 20 mV	–25		+25	%
		[$V_{CSIN} – V_{BAT}$] from 20 mV to 40 mV	–5		+5	
	Termination Current Deglitch Time	2mV Overdrive		30		ms
VREF Pin						
V_{REF}	VREF Pin Output Voltage	I_{REF} from 0 to 1 mA, PMID ≥ 5.6 V			5.4	V
		I_{REF} from 0 to 1 mA, PMID < 5.6 V		PMID – 350		mV
	Short-Circuit Current Limit			15		mA

Continued on the following page…

Electrical Specifications

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{IN} = 5.0 V, CE# = HZ_MODE = 0, (Charger Mode operation). SCL, SDA, and SRST = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Input Power Source Detection						
$V_{IN(MIN)1}$	V_{IN} Input Voltage Rising	To Start VIN Validation	4.21	4.29	4.37	V
$V_{IN(MIN)2}$	Minimum V_{IN} to Pass Validation	During VIN Validation Period	4.00	4.08	4.15	V
$V_{IN(MIN)3}$	Minimum V_{IN} During Charge	During Charging	3.63	3.71	3.78	V
t_{VIN_VALID}	V_{IN} Validation Time			30		ms
Special Charger						
V_{SP}	Special Charger Setpoint Accuracy		–3		+3	%
Battery Recharge Threshold						
V_{RCH}	Recharge Threshold	Below $V_{(OREG)}$	100	120	150	mV
t_G	Deglitch Time	V_{BAT} Falling Below V_{RCH} Threshold		130		ms
STAT Output						
$V_{STAT(OL)}$	STAT Output Low	I_{STAT} = 10 mA			0.4	V
$I_{STAT(OH)}$	STAT High Leakage Current	V_{STAT} = 5 V			1	µA
Battery Detection						
I_{DETECT}	Battery Detection Current Before Charge Done (Sink Current)(3)	Begins After Termination Detected and $V_{BAT} \le V_{OREG} - V_{RCH}$		–0.80		mA
t_{DETECT}	Battery Detection Time			262		ms
Sleep Comparator						
V_{SLP}	Sleep-Mode Entry Threshold, $V_{IN} - V_{BAT}$	2.3 V ≤ V_{BAT} ≤ V_{OREG}, V_{IN} Falling	0	0.04	0.10	V
V_{SLP_EXIT}	Sleep-Mode Exit Hysteresis	2.3 V ≤ V_{BAT} ≤ V_{OREG}	40	100	160	mV
	Deglitch Time for V_{IN} Rising Above V_{SLP} + V_{SLP_EXIT}	Rising Voltage		30		ms
Power Switches *(see Figure 3)*						
$R_{DS(ON)}$	Q3 On Resistance (VIN to PMID)			180	250	mΩ
	Q1 On Resistance (PMID to SW)			130	225	mΩ
	Q2 On Resistance (SW to GND)			175	225	mΩ
Charger PWM Modulator						
f_{SW}	Oscillator Frequency		2.7	3.0	3.3	MHz
D_{MAX}	Maximum Duty Cycle				99.6	%
D_{MIN}	Minimum Duty Cycle		0			%
I_{SYNC}	Synchronous to Non-Synchronous Current Cut-Off Threshold(4)	Low-Side MOSFET Cycle-by-Cycle Current Limit		170		mA
V_{IN} Load Resistance						
R_{VIN}	VIN to PGND Resistance	Normal Operation	650	1300	1950	KΩ
		Charger Validation	50	110	175	Ω

Continued on the following page…

Electrical Specifications

Unless otherwise specified: circuit of Figure 1, recommended operating temperature range for T_J and T_A, V_{IN} = 5.0 V, CE# = HZ_MODE = 0, (Charger Mode operation). SCL, SDA, and SRST = 0 or 1.8 V; typical values are for T_J = 25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Protection and Timers						
V_{INOVP}	V_{IN} Over-Voltage Shutdown	V_{IN} Rising	6.83	7.03	7.23	V
	Hysteresis	V_{IN} Falling		130		mV
$I_{LIMPK(CHG)}$	Q1 Cycle-by-Cycle Peak Current Limit	Charge Mode		2.3		A
V_{SHORT}	Battery Short-Circuit Threshold	V_{BAT} Rising	1.95	2.00	2.05	V
	Hysteresis	V_{BAT} Falling		100		
I_{SHORT}	Short-Circuit Current	$V_{BAT} < V_{SHORT}$	20	30	40	mA
$T_{SHUTDWN}$	Thermal Shutdown Threshold(5)	T_J Rising		165		°C
	Hysteresis(5)	T_J Falling		10		
T_{CF}	Thermal Regulation Threshold(5)	Charge Current Reduction Begins		120		°C
t_{INT}	Detection Interval			2.1		s
t_{32SEC}	32-Second Timer	32-Second Mode(6)	21.0		31.5	s
t_{15MIN}	15-Minute Timer	15-Minute Mode	12.0	13.5	15.0	min

Notes:
3. Negative current is current flowing from the battery to the VIN pin (discharging the battery).
4. Q2 always turns on for 60 ns, then turns off if current is below I_{SYNC}.
5. Guaranteed by design.
6. This tolerance applies to all timers on the IC, including soft-start and deglitching timers.

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, C_B ≤ 100 pF			3400	
		High-Speed Mode, C_B ≤ 400 pF			1700	
t_{BUF}	Bus-Free Time Between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		High-Speed Mode, C_B ≤ 100 pF		160		ns
		High-Speed Mode, C_B ≤ 400 pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, C_B ≤ 100 pF		60		ns
		High-Speed Mode, C_B ≤ 400 pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, C_B ≤ 100 pF	0		70	ns
		High-Speed Mode, C_B ≤ 400 pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, C_B ≤ 100 pF		10	80	
		High-Speed Mode, C_B ≤ 400 pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, C_B ≤ 100 pF		10	40	
		High-Speed Mode, C_B ≤ 400 pF		20	80	
t_{RDA} t_{RCL1}	SDA Rise Time, Rise Time of SCL After a Repeated START Condition and After ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, C_B ≤ 100 pF		10	80	
		High-Speed Mode, C_B ≤ 400 pF		20	160	

Continued on the following page…

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{FDA}	SDA Fall Time	Standard Mode		$20+0.1C_B$	300	ns
		Fast Mode		$20+0.1C_B$	300	
		High-Speed Mode, $C_B \le 100$ pF		10	80	
		High-Speed Mode, $C_B \le 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

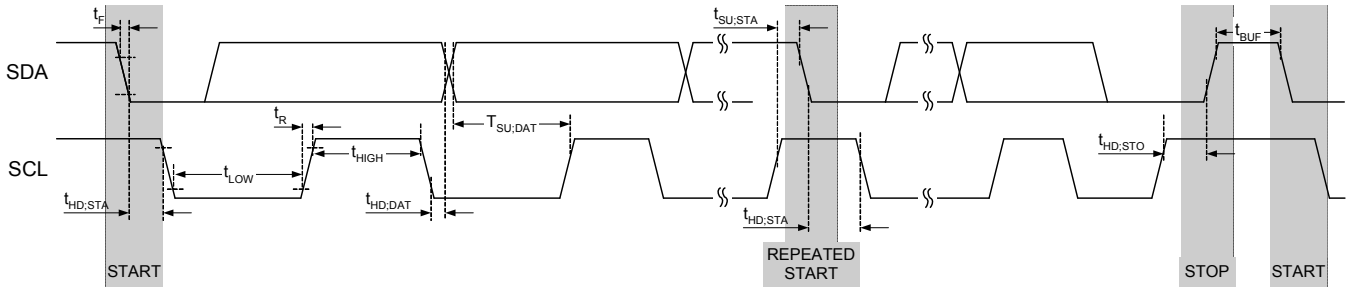
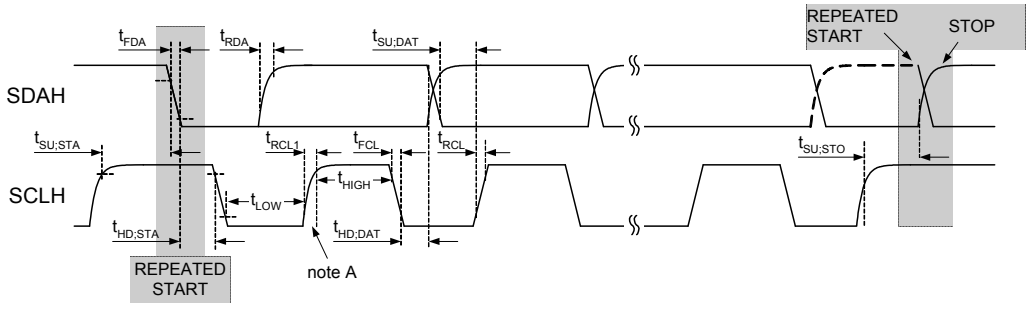


Figure 6. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 7. I²C Interface Timing for High-Speed Mode

Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.2 V, V_{IN} = 5.0 V, and T_A=25°C.

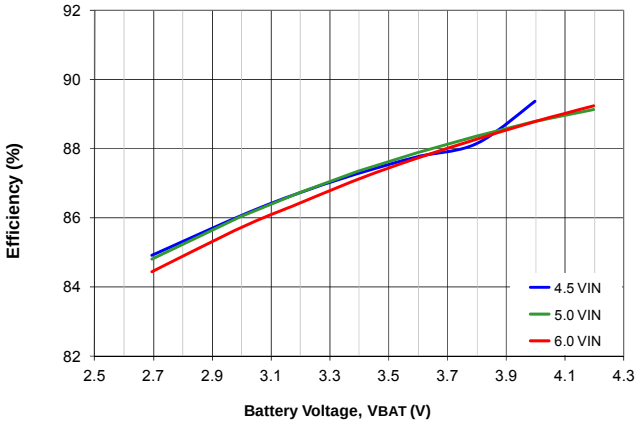


Figure 8. Charger Efficiency, $I_{OCHARGE}$=950 mA

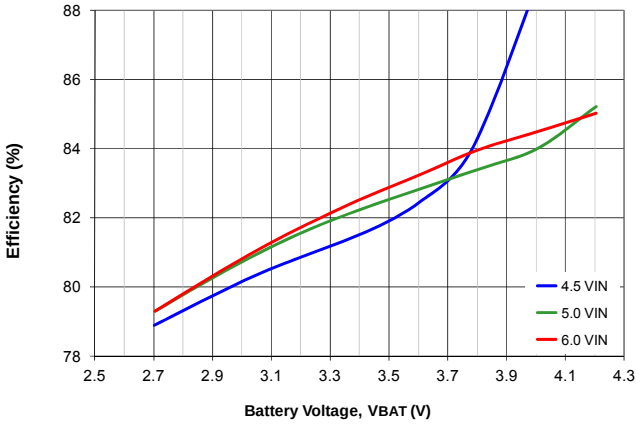


Figure 9. Charger Efficiency, $I_{OCHARGE}$=1,550 mA

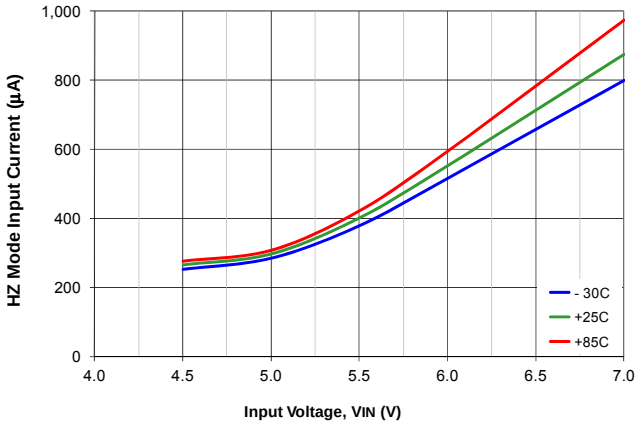


Figure 10. V_{IN} Current in High-Impedance Mode, V_{BAT}=3.6 V

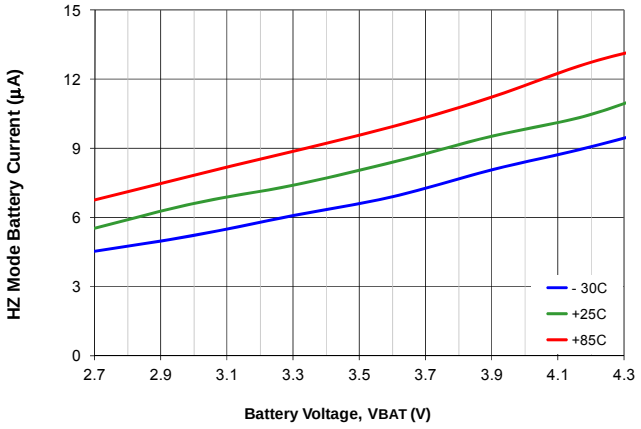


Figure 11. Battery Current in High-Impedance Mode, V_{IN}=Open

Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.2 V, V_{IN} = 5.0 V, and T_A=25°C.

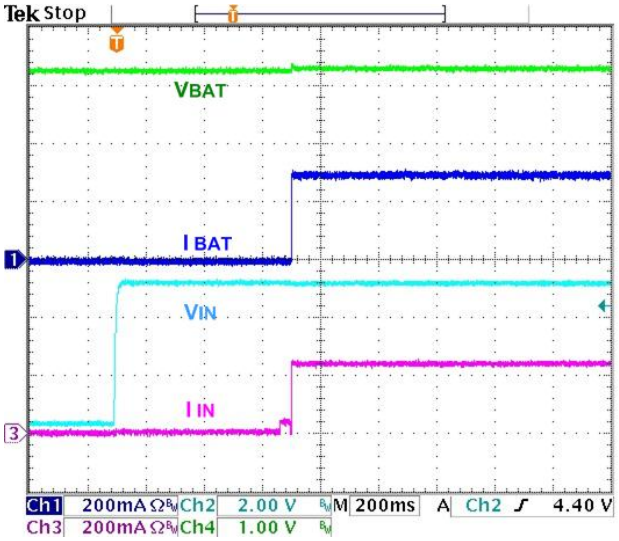


Figure 12. Auto-Charge Startup at V_{BUS} Plug-in, V_{BAT}=3.2 V, $I_{OCHARGE}$=340 mA

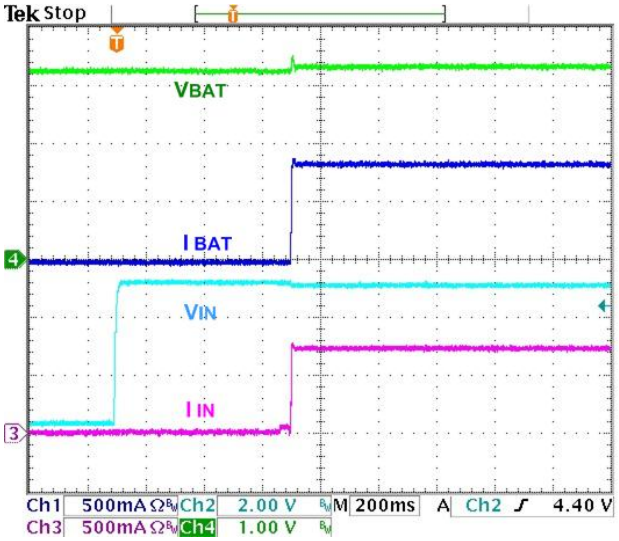


Figure 13. Auto-Charge Startup at V_{BUS} Plug-in, V_{BAT}=3.2 V, $I_{OCHARGE}$=950 mA

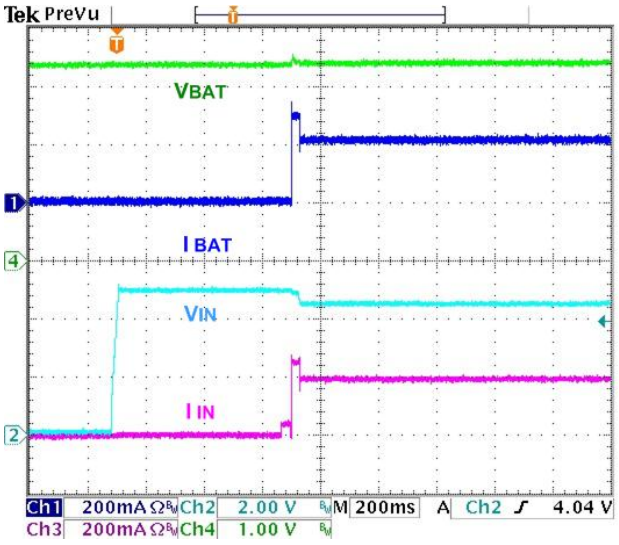


Figure 14. Auto-Charge Startup with 200 mA Limited Charger / Adaptor, V_{BAT}=3.4 V

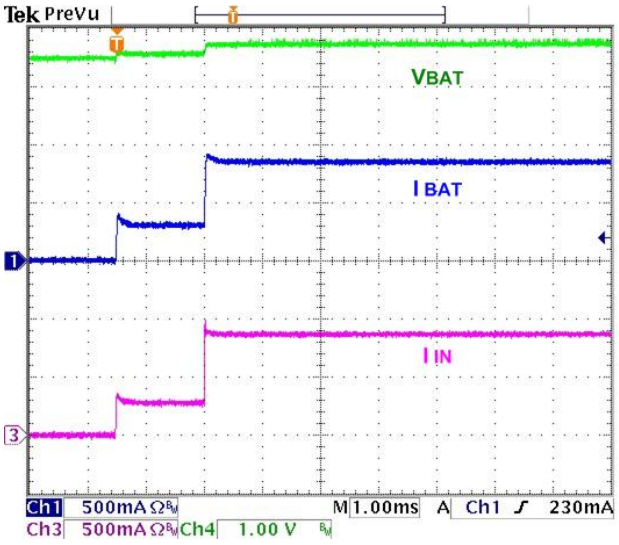


Figure 15. Charger Startup with HZ_MODE Bit Reset, $I_{OCHARGE}$=950 mA, V_{OREG}=4.2 V, V_{BAT}=3.6 V

Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG} = 4.2 V, V_{IN} = 5.0 V, and T_A=25°C.

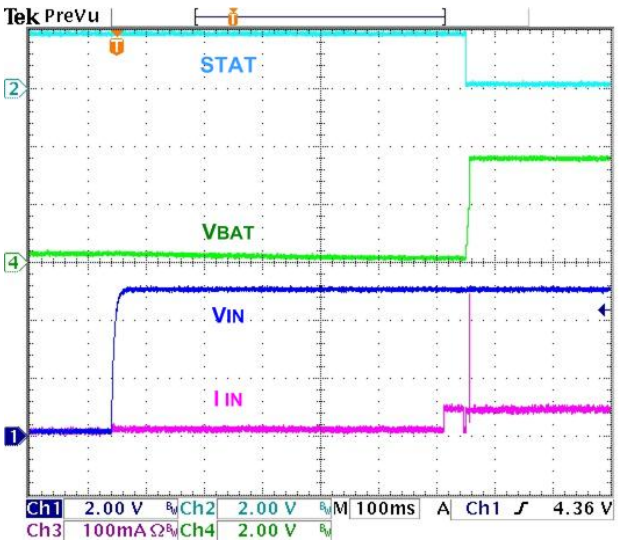


Figure 16. No Battery at V_{IN} Power-up

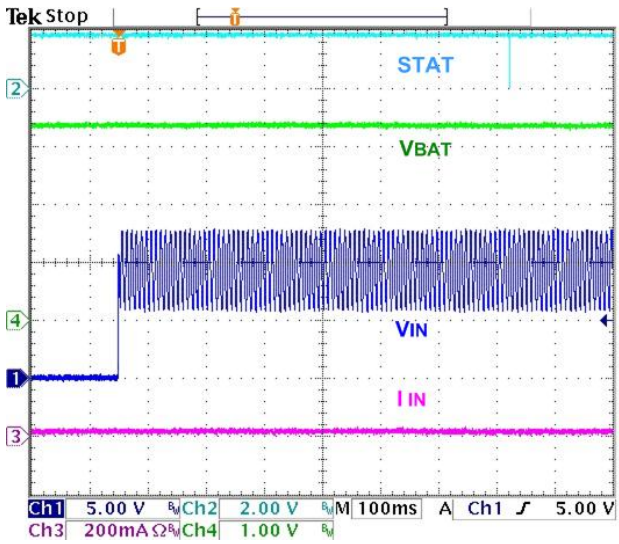


Figure 17. Non-Compliant Charger Rejection, V_{BAT}=3.4 V

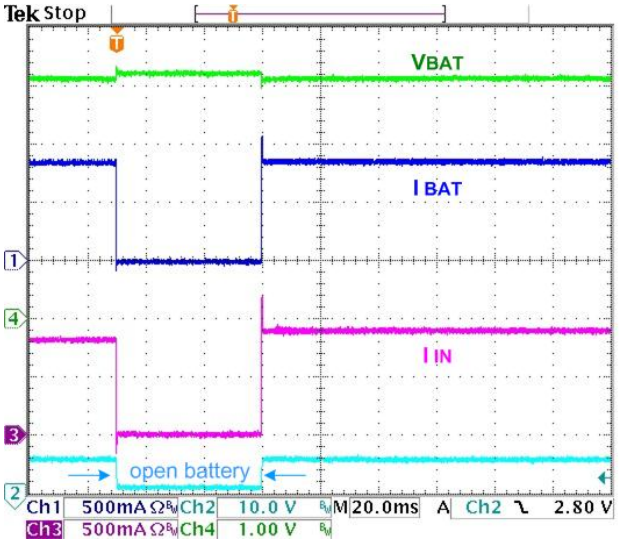


Figure 18. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=950 mA, TE=0

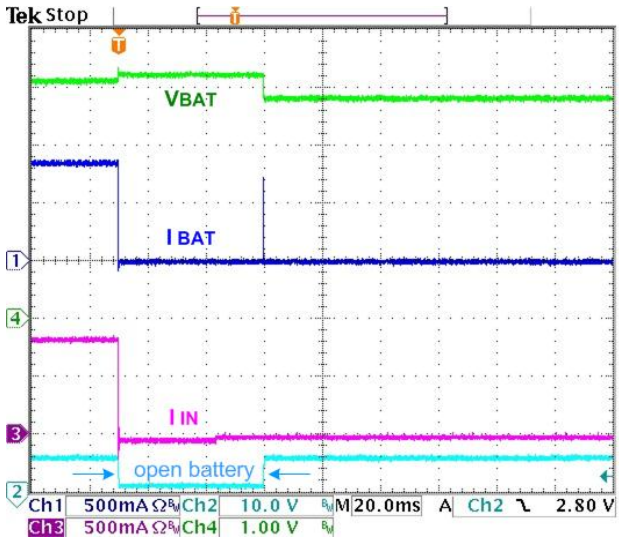


Figure 19. Battery Removal / Insertion During Charging, V_{BAT}=3.9 V, $I_{OCHARGE}$=950 mA, TE=1

Circuit Description / Overview

The FAN5421 is a highly integrated synchronous buck regulator for charging that can accommodate a wide range of input sources, including USB and current-limited “wall wart” power sources. The regulator employs synchronous rectification to maintain high efficiency over a wide range of battery voltages and charge states.

When charging batteries with a current-limited input source, the switching charger’s high efficiency over a wide range of output voltages minimizes charging time.

The FAN5421 has two operating modes:

1. Charge Mode:
   Charges a single-cell Li-Ion or Li-polymer battery.
2. High-Impedance Mode:
   The charging circuits are off in this mode. Current flow from VIN to the battery or from the battery to VIN is blocked in this mode. This mode consumes very little current from VIN or the battery.

Charge Mode

In Charge Mode, FAN5421 employs four regulation loops:

1. Charging Current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
2. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery’s internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
3. Temperature: If the IC’s junction temperature reaches 120°C, charge current is continuously reduced until the IC’s temperature stabilizes at 120°C.
4. VIN: This loop limits the amount of drop on VIN to a programmable voltage (V_{SP}) to accommodate “special chargers” that limit current to a lower current than might be available from a “normal” wall charger.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source “pre-charges” the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. Current slew rate is limited to prevent overshoot.

The FAN5421 is designed to work with a current-limited input source at VIN. During the current regulation phase of charging, the input power source may limit the amount of current available to charge the battery and power the system. The effect of input current limit on I_{CHARGE} can be seen in Figure 21.

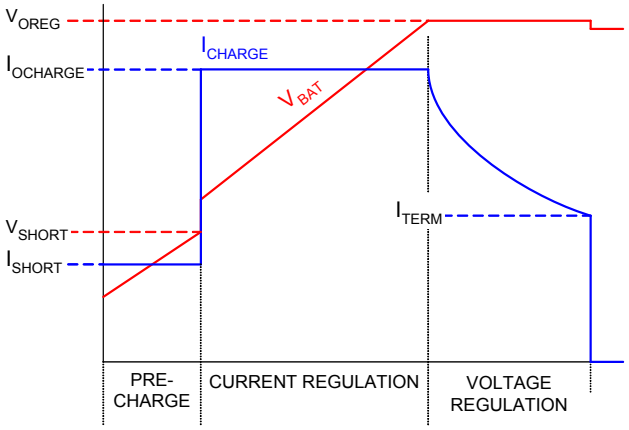


Figure 20. Charge Curve When Source Current Does Not Limit I_{CHARGE}

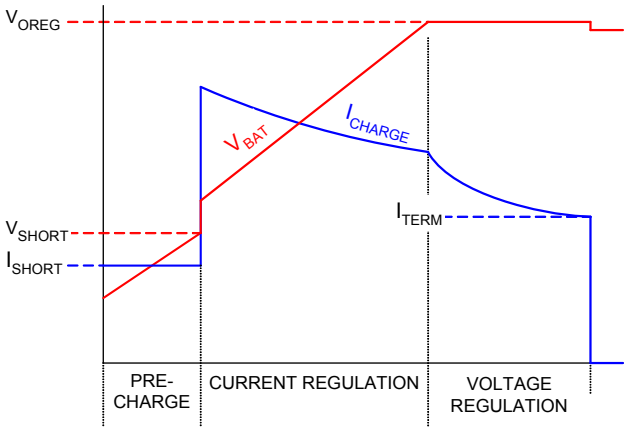


Figure 21. Charge Curve When Input Source Limits I_{CHARGE}

Assuming V_{OREG} is programmed to the cell’s fully charged “float” voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines and the charger enters voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG1[3]).

The charger output or “float” voltage can be programmed by the OREG bits from 3.5 V to 4.44 V in 20 mV increments, as shown in Table 3.

Table 3. OREG Bits (OREG[7:2]) vs. Charger V_{OUT} (V_{OREG}) Float Voltage

Decimal	Hex	V_{OREG}	Decimal	Hex	V_{OREG}
0	00	3.50	32	20	4.14
1	01	3.52	33	21	4.16
2	**02**	**3.54**	34	22	4.18
3	03	3.56	35	23	4.20
4	04	3.58	36	24	4.22
5	05	3.60	37	25	4.24
6	06	3.62	38	26	4.26
7	07	3.64	39	27	4.28
8	08	3.66	40	28	4.30
9	09	3.68	41	29	4.32
10	0A	3.70	42	2A	4.34
11	0B	3.72	43	2B	4.36
12	0C	3.74	44	2C	4.38
13	0D	3.76	45	2D	4.40
14	0E	3.78	46	2E	4.42
15	0F	3.80	47	2F	4.44
16	10	3.82	48	30	4.44
17	11	3.84	49	31	4.44
18	12	3.86	50	32	4.44
19	13	3.88	51	33	4.44
20	14	3.90	52	34	4.44
21	15	3.92	53	35	4.44
22	16	3.94	54	36	4.44
23	17	3.96	55	37	4.44
24	18	3.98	56	38	4.44
25	19	4.00	57	39	4.44
26	1A	4.02	58	3A	4.44
27	1B	4.04	59	3B	4.44
28	1C	4.06	60	3C	4.44
29	1D	4.08	61	3D	4.44
30	1E	4.10	62	3E	4.44

Note:
7. Default register settings are denoted by **bold typeface**.

The charging parameters in Table 4 can be programmed by the host through the I^2C interface.

Table 4. Programmable Charging Parameters

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG2[7:2]
Battery Charging Current Limit	I_{OCHRG}	REG4[6:4]
Charge Termination Limit	I_{TERM}	REG4[2:0]
Weak Battery Voltage	V_{LOWV}	REG1[5:4]

A new charge cycle begins when one of the following occurs:

1. The battery voltage falls below V_{OREG} - V_{RCH}.
2. V_{IN} Power-On-Reset (POR) clears and the battery voltage is below the weak battery threshold (V_{LOWV}).
3. The $\overline{CE}$ or RESET bit is set.

Charge Current Limit

Table 5. $I_{OCHARGE}$ Current as a Function of the IOCHARGE Bits and R_{SENSE} Resistor Value

DEC	BIN	HEX	V_{RSENSE} (mV)	$I_{OCHARGE}$ (mA)	
				68 mΩ	100 mΩ
0	**0000**	**00**	**37.4**	**550**	**374**
1	0001	01	44.2	650	442
2	0010	02	51.0	750	510
3	0011	03	57.8	850	578
4	0100	04	64.6	950	646
5	0101	05	71.4	1,050	714
6	0110	06	78.2	1,150	782
7	0111	07	85.0	1,250	850
8	1000	08	91.8	1,350	918
9	1001	09	98.6	1,450	986
10	1010	0A	105.4	1,550	1,054
11	1011	0B	105.4	1,550	1,054
12	1100	0C	105.4	1,550	1,054
13	1101	0D	105.4	1,550	1,054
14	1110	0E	105.4	1,550	1,054
15	1111	0F	105.4	1,550	1,054

Termination Current Limit

Current charge termination is enabled when TE (REG1[3]) = 1. Typical termination current values are given in Table 6.

Table 6. I_{TERM} Current as a Function of the ITERM Bits (REG4[2:0]) and R_{SENSE} Resistor Value

ITERM	BIN	HEX	V_{RSENSE} (mV)	I_{TERM} (mA)	
				68 mΩ	100 mΩ
0	000	00	3.3	49	33
1	**001**	**01**	**6.6**	**97**	**66**
2	010	02	9.9	146	99
3	011	03	13.2	194	132
4	100	04	16.5	243	165
5	101	05	19.8	291	198
6	110	06	23.1	340	231
7	111	07	26.4	388	264

When the charge current falls below I_{TERM}, PWM charging stops and the STAT bits change to READY (00) for about 500ms while the IC determines whether the battery and charging source are still connected. If they are, STAT then changes to CHARGE DONE (10).

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents. A cycle-by-cycle current limit of nominally 2.3 A, sensed through Q1, is used to terminate t_{ON}. The synchronous rectifier (Q2) also has a current limit that turns off Q2 at 100 mA to prevent current flow from the battery.

Safety Timer *see Figure 26*

At the beginning of charging process, the IC starts a 15-minute timer (t_{15MIN}). When this timer expires, charging is terminated. Writing to any register through I^2C stops the t_{15MIN} timer, which then starts a 32-second timer (t_{32SEC}). Setting the TMR_RST bit (REG0[7]) resets the t_{32SEC} timer. If the t_{32SEC} timer expires; charging is terminated, the registers are set to default values, and charging resumes using the default values with the t_{15MIN} timer running.

Normal charging is controlled by the host with the t_{32SEC} timer running to ensure that the host is alive. Charging with the t_{15MIN} timer running is used for charging that is unattended by the host. If the 15-minute timer expires; the IC turns off the charger, sets the $\overline{CE}$ bit, and indicates a timer fault (110) on the FAULT bits (REG0[2:0]). This sequence prevents overcharge if the host fails to reset the t_{32MIN} timer.

V_{IN} POR / Non-Compliant Charger Rejection

When the IC detects that V_{IN} has risen above $V_{IN(MIN)1}$ (4.4 V), the IC applies a 110 Ω load from VIN to GND. To clear the V_{IN} Power-On-Reset (POR) and begin charging, V_{IN} must remain above $V_{IN(MIN)2}$ (4.1 V) and below VIN_{OVP} for t_{VIN_VALID} (30 ms). The V_{IN} validation sequence always occurs before charging is initiated or re-initiated (for example, after a V_{IN} OVP fault or a V_{RCH} recharge initiation).

t_{VIN_VALID} ensures that unfiltered 50 / 60 Hz chargers and other non-compliant chargers are rejected.

Boot Sequence

At V_{IN} POR, when the battery voltage is above the weak battery threshold (V_{LOWV}), the IC operates in accordance with its I^2C register settings. If $V_{BAT} < V_{LOWV}$, the IC sets all registers to their default values and enables the charger. This feature can revive a cell whose voltage is too low to ensure reliable host operation. Charging continues in the absence of host communication even after the battery has reached V_{OREG}, whose default value is 3.54 V, and the charger remains active until t_{15MIN} expires. Once the host processor begins writing to the IC, charging parameters are set by the host, which must continually reset the t_{32SEC} timer by writing to the TMR_RST bit to continue charging using the programmed charging parameters. If t_{32SEC}.expires, the register defaults are loaded, the FAULT bits are set to 110, STAT is pulsed HIGH, and charging continues with default charging parameters.

Flow Charts

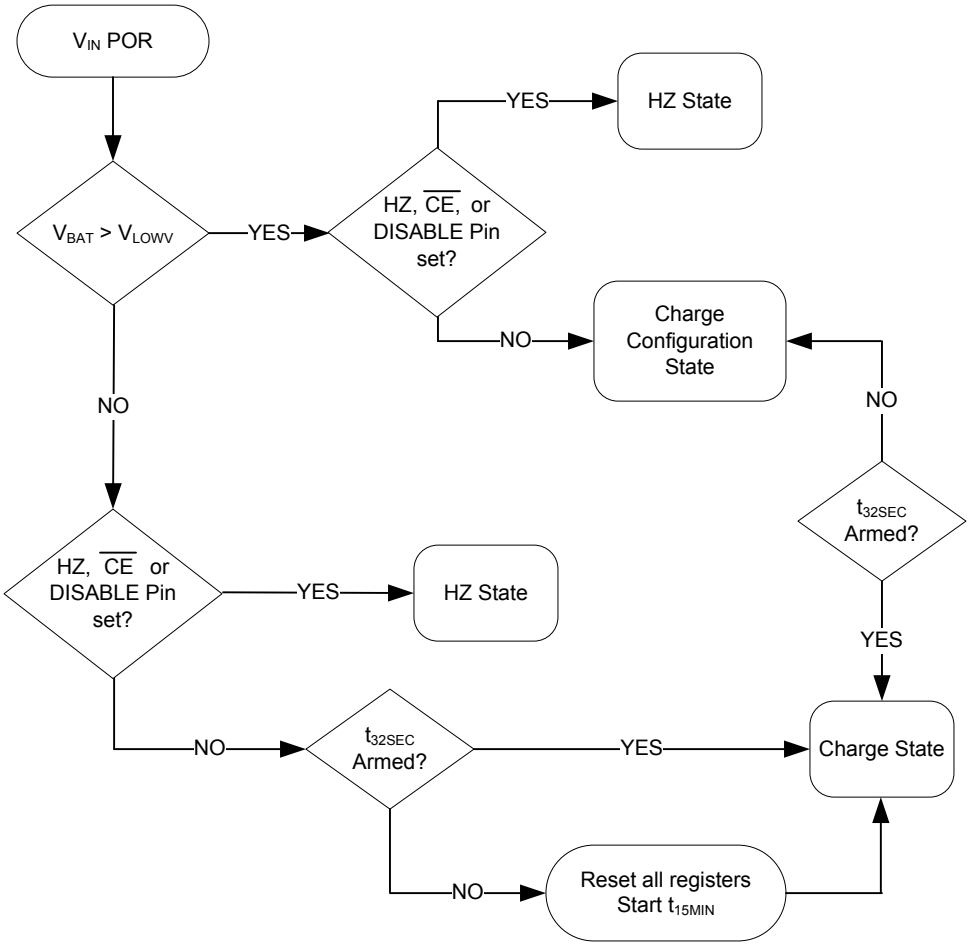


Figure 22. Charger V_{IN} POR

Flow Charts

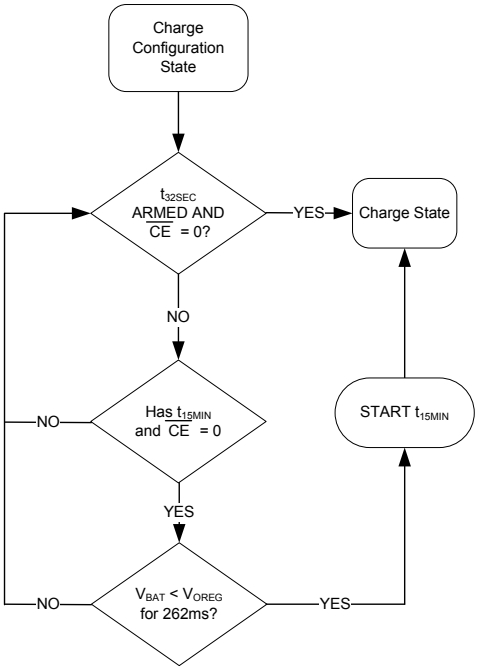


Figure 23. Charge Configuration State

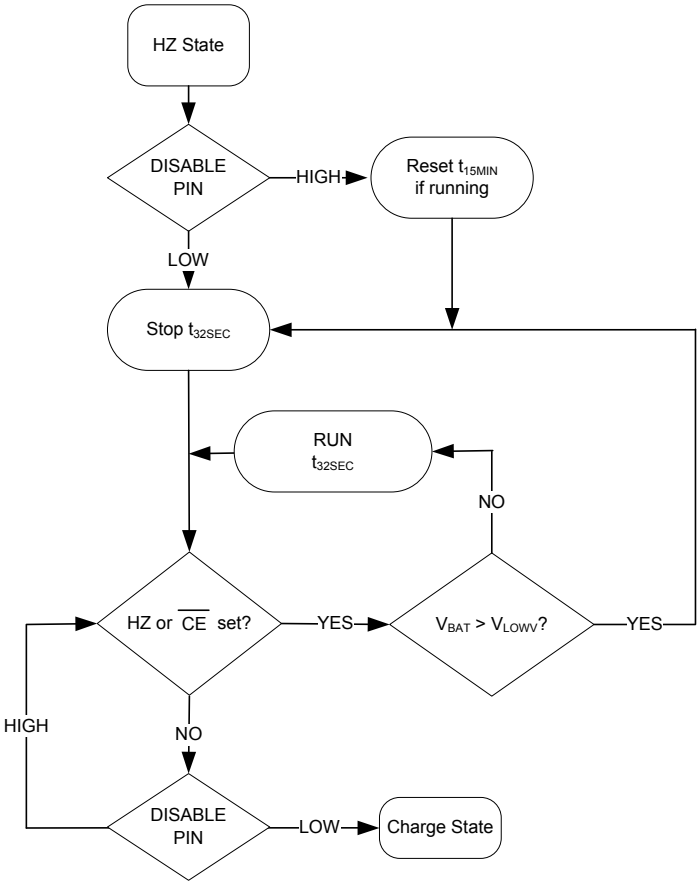


Figure 24. HZ State

Flow Charts

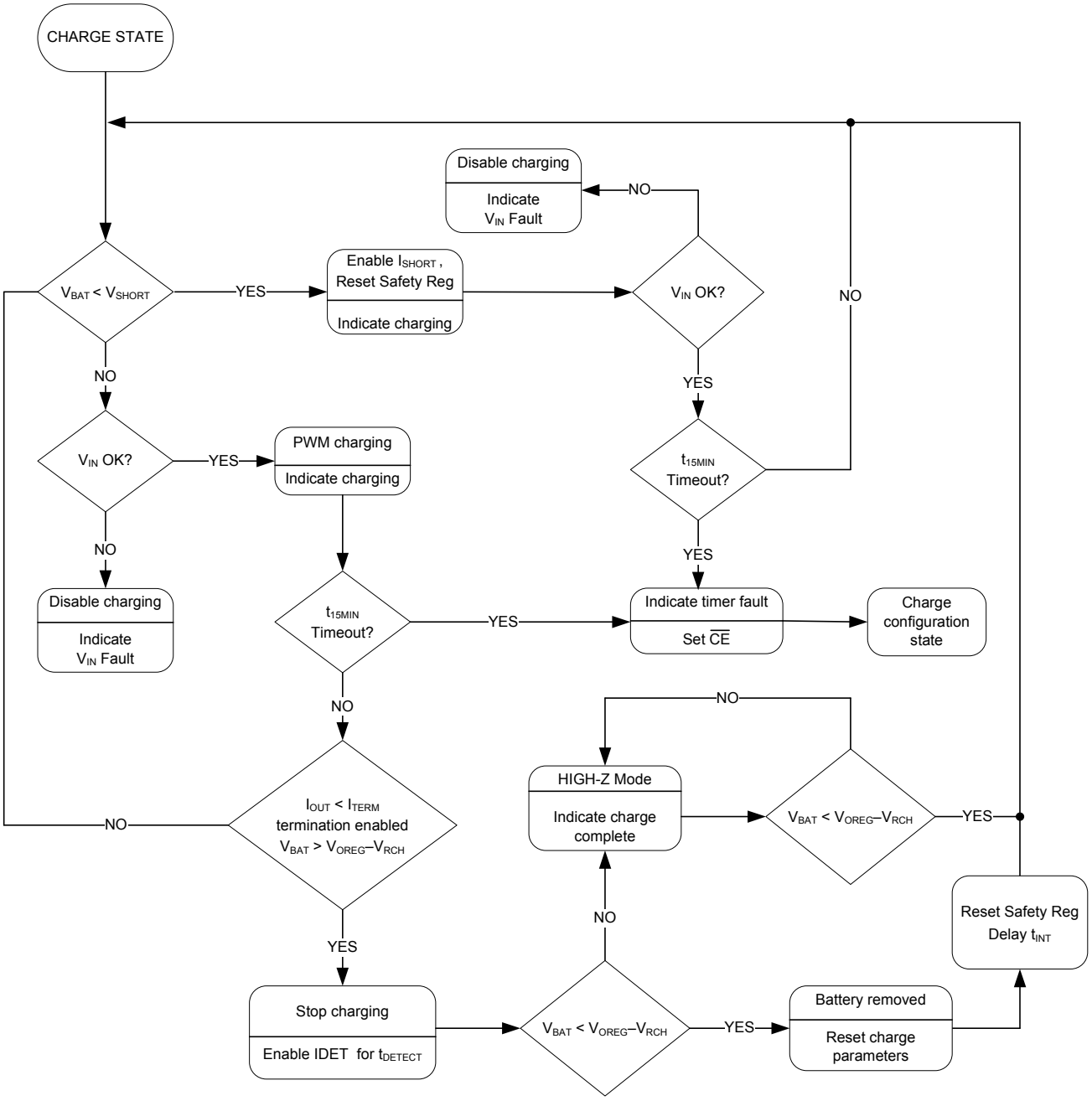


Figure 25. Charge Mode Operational Flow Chart

Flow Charts

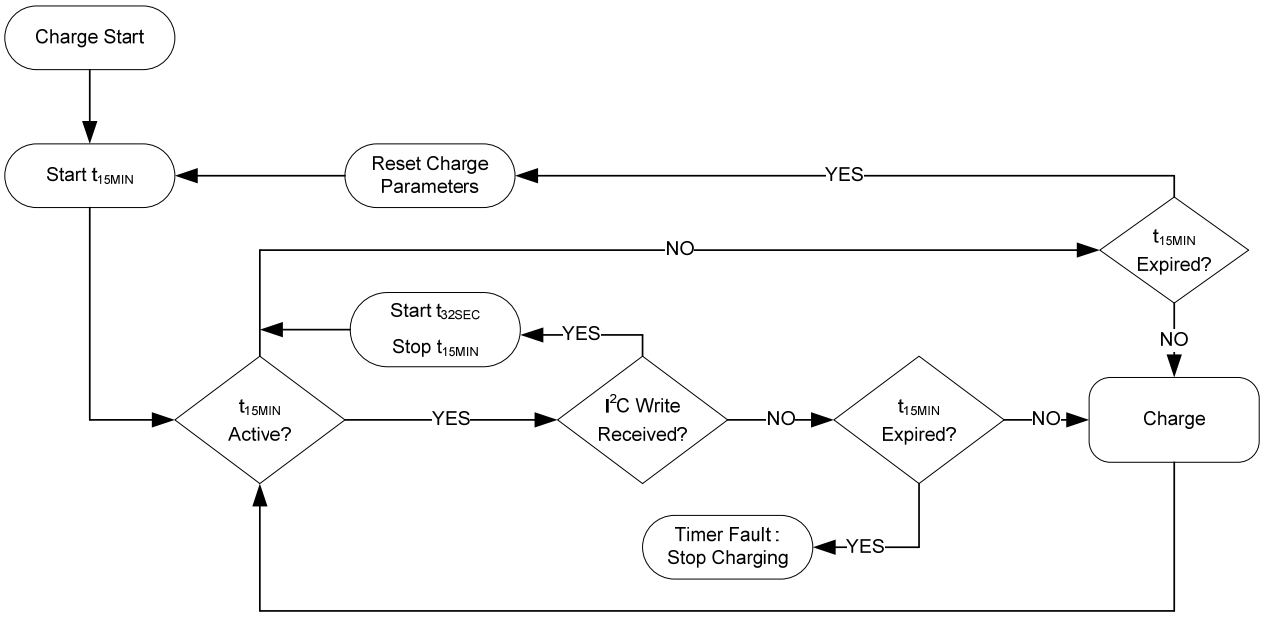


Figure 26. Timer Flow Chart

Current Limited Charger: V_{SP} Loop

The FAN5421 can accommodate current-limited input supplies by reducing the charging current to prevent V_{BUS} from falling below a specified limit. When a current-limited charger is supplying V_{IN}, the IC slowly increases the charging current until either:

- $I_{OCHARGE}$ is reached, or
- $V_{IN} = V_{SP}$.

If V_{IN} collapses to V_{SP} when current is ramping up, the IC charges with an input current that keeps $V_{IN} = V_{SP}$. When the V_{SP} control loop is limiting the charge current, the SP bit (REG5[4]) is set.

Table 7. V_{SP} as a Function of SP Bits (REG5[2:0])

SP (REG5[2:0])			
DEC	**BIN**	**HEX**	**V_{SP}**
0	000	00	4.20
1	001	01	4.28
2	010	02	4.36
3	011	03	4.44
4	**100**	**04**	**4.52**
5	101	05	4.60
6	110	06	4.68
7	111	07	4.76

Safety Settings

The IC contains a SAFETY register (REG6) that prevents the values in OREG (REG2[7:2]) and IOCHARGE (REG4[7:4]) from exceeding the VSAFE and ISAFE values.

After V_{BAT} rises above V_{SHORT}, the SAFETY register is loaded with its default value and may be written only before another register is written. After writing to any other register, the SAFETY register is locked until V_{BAT} falls below V_{SHORT}.

The ISAFE (REG6[6:4]) and VSAFE (REG6[3:0]) establish values that limit the maximum values of $I_{OCHARGE}$ and V_{OREG} used by the control logic. If the host attempts to write a value higher than VSAFE or ISAFE to OREG or IOCHARGE, respectively, the VSAFE or ISAFE value appears as the OREG and IOCHARGE register value, respectively.

Table 8. I_{SAFE} ($I_{OCHARGE}$ Limit) as a Function of ISAFE Bits (REG6[7:4])

ISAFE (REG6[7:4])					
DEC	**BIN**	**HEX**	**V_{RSENSE} (mV)**	**I_{SAFE} (mA)**	
				68 mΩ	**100 mΩ**
0	0000	00	37.4	550	374
1	0001	01	44.2	650	442
2	0010	02	51.0	750	510
3	0011	03	57.8	850	578
4	**0100**	**04**	**64.6**	**950**	**646**
5	0101	05	71.4	1,050	714
6	0110	06	78.2	1,150	782
7	0111	07	85.0	1,250	850

Table 8. I_{SAFE} ($I_{OCHARGE}$ Limit) as a Function of ISAFE Bits (REG6[7:4])

ISAFE (REG6[7:4])					
DEC	BIN	HEX	V_{RSENSE} (mV)	I_{SAFE} (mA)	
				68 mΩ	100 mΩ
8	1000	17	91.8	1,350	918
9	1001	18	98.6	1,450	986
10	1010	19	105.4	1,550	1,054
11	1011	1A	112.2	1,650	1,122
12	1100	1B	119.0	1,750	1,190
13	1101	1C	125.8	1,850	1,258
14	1110	1D	132.6	1,950	1,326
15	1111	1E	139.4	2,050	1,394

Table 9. V_{SAFE} (V_{OREG} Limit) as a Function of VSAFE Bits (REG6[3:0])

VSAFE (REG6[3:0])				
DEC	BIN	HEX	Max. OREG (REG2[7:2])	V_{OREG} Max.
0	**0000**	**00**	**100011**	**4.20**
1	0001	01	100100	4.22
2	0010	02	100101	4.24
3	0011	03	100110	4.26
4	0100	04	100111	4.28
5	0101	05	101000	4.30
6	0110	06	101001	4.32
7	0111	07	101010	4.34
8	1000	08	101011	4.36
9	1001	09	101100	4.38
10	1010	0A	101101	4.40
11	1011	0B	101110	4.42
12	1100	0C	101111	4.44
13	1101	0D	110000	4.44
14	1110	0E	110001	4.44
15	1111	0F	110010	4.44

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{CF} (about 120°C), the charger reduces its output current to prevent overheating. If the temperature continues to increase, the current is reduced to 0 when the junction is 10°C above T_{CF}. If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101, and STAT is pulsed HIGH. In Suspend Mode, all timers stop and the state of the IC's logic is preserved. Charging resumes after the die cools to about 10°C below $T_{SHUTDOWN}$.

Charge Mode Input Supply Protection

Sleep Mode

When V_{IN} falls below V_{BAT} + V_{SLP} and V_{IN} is above $V_{IN(MIN)}$, the IC enters Sleep Mode to prevent the battery from draining into VIN. During Sleep Mode, reverse current is disabled by turning off Q3.

Input Supply Low-Voltage Detection

The IC continuously monitors V_{IN} during charging. If V_{IN} falls below $V_{IN(MIN)}$; the IC terminates charging and pulses the STAT pin HIGH, sets STAT bits to 11, and sets the FAULT bits to 011.

If V_{IN} recovers above the $V_{IN(MIN)}$ rising threshold after timer t_{INT} (about two seconds), the charging process is repeated. This function prevents the input power bus from collapsing or oscillating when the IC is connected to a suspended USB port or a low-current-capable OTG device.

Input Over-Voltage Detection

When V_{IN} exceeds VIN_{OVP}, the IC:

1. Turns off Q3,
2. Suspends charging, and
3. Sets the FAULT bits to 001, STAT bits to 11, and pulses the STAT pin.

When V_{IN} falls about 130mV below VIN_{OVP}, the fault is cleared and charging resumes after VIN is revalidated *(seeVIN POR / Non-Compliant Charger Rejection above)*.

Charge Mode Battery Detection and Protection

V_{BAT} Over-Voltage Protection (OVP)

The OREG voltage regulation loop prevents V_{BAT} from overshooting the OREG voltage by more than 50 mV when the battery is removed. When the PWM charger is running with no battery, the TE bit is not set, and a battery is inserted that's charged to a voltage higher than V_{OREG}; PWM pulses stop. If no further pulses occur for 30ms, the IC sets the FAULT bits to 100, STAT bits to 11, and pulses the STAT pin.

Battery Detection During Charging

The IC can detect presence, absence, or removal of a battery if the termination bit is set (TE=1). During normal charging; once V_{BAT} is close to V_{OREG} and the termination charge current is detected, the IC terminates charging and sets the STAT bits to 10. It then turns on a discharge current, I_{DETECT}, for t_{DETECT}. If V_{BAT} is still above V_{OREG} – V_{RCH}, the battery is present and the IC sets the FAULT bits to 000. If V_{BAT} is below V_{OREG} – V_{RCH}, the battery is absent and the IC:

1. Sets the registers to their default values,
2. Sets the FAULT bits to 111, and
3. Resumes charging with default values after delay t_{INT}.

If the battery is removed while charging with TE = 0, charging continues and V_{BAT} is regulated to V_{OREG}.

System Operation with No Battery

The IC continues charging after VIN POR with the default parameters, regulating the V_{BAT} line to 3.54 V until the host processor issues commands or the 15-minute timer expires. In this way, the IC can start the system without a battery.

By default, the system current is limited to 325 mA. To increase the current limit, use the following sequence.

1. Program the Safety Register.
2. Set OREG to the desired value (typically 4.18).
3. Set IOCHARGE, then reset the IOLEVEL bit.

Battery Short-Circuit Protection

If the battery voltage is below the short-circuit threshold (V_{SHORT}); a linear current source, I_{SHORT}, supplies V_{BAT} until $V_{BAT} > V_{SHORT}$.

Charger Status / Fault Status

The STAT pin indicates the operating condition of the IC and provides a fault indicator for interrupt driven systems.

Table 10. STAT Pin Function

EN_STAT	Charge State	STAT Pin
0	X	OPEN
X	Normal Conditions	OPEN
1	Charging	LOW
X	Fault	128 μs Pulse, then OPEN

The FAULT bits (R0[2:0]) indicate the type of fault in Charge Mode, as shown in Table 11.

Table 11. Fault Status Bits

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (No Fault)
0	0	1	V_{BUS} OVP
0	1	0	Sleep Mode
0	1	1	Poor Input Source
1	0	0	Battery OVP
1	0	1	Thermal Shutdown
1	1	0	Timer Fault
1	1	1	No Battery

Charge Control Bits

The following table defines the $\overline{CE}$ and RESET bit functions.

Table 12. Charge Control Bits

Bit	Reg	State	Function
$\overline{CE}$	REG0[2]	0	Charging Enabled
		1	Charging Disabled
RESET	REG4[7]	1	Writing 1 resets all registers to their default values

$\overline{CE}$ is set by the FAN5421 when t_{15MIN} timer overflows.

Table 13. DISABLE Pin and $\overline{CE}$ Bit Functionality

Charging	DISABLE PIN	$\overline{CE}$ BIT: REG 01[2]
ENABLE	0	0
DISABLE	X	1
DISABLE	1	X

VREF PIN

The VREF pin is powered from PMID and is on only when PMID > V_{BAT} and does not drain current from the battery. The IC uses this pin for its bias supply. Its output is about 350 mV below PMID as long as PMID < 5.6 V. If V_{BUS} / PMID rise above 5.6 V, the VREF pin remains below 5.35 V.

I²C Interface

The FAN5421 serial interface is compatible with Standard, Fast, Fast-Plus, and High-Speed (HS) Mode I²C-Bus® specifications. The SCL line is an input. The SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Table 14. I²C Slave Address

7	6	5	4	3	2	1	0
1	1	0	1	0	1	0	R/$\overline{W}$

In Hex notation, the slave address assumes a 0 LSB. The hex slave address is D4H.

Bus Timing

As shown in Figure 27, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

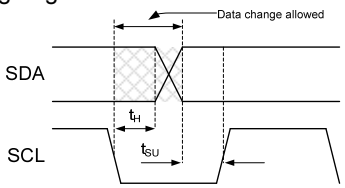


Figure 27. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a "START" condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 28.

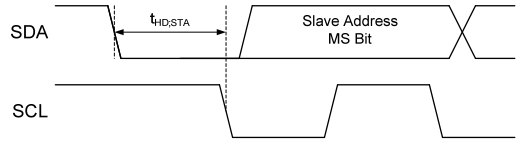


Figure 28. Start Bit

A transaction ends with a "STOP" condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 29.

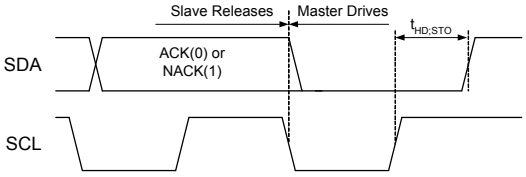


Figure 29. Stop Bit

During a read from the FAN5421 (Figure 32), the master issues a "REPEATED START" after sending the register address and before resending the slave address. The "REPEATED START" is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 30.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical; except the bus speed for HS mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition. The master code is sent in Fast or Fast-Plus Mode (less than 1 MHz clock) and slaves do not ACK this transmission.

The master then generates a REPEATED START condition (Figure 30) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 29) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 30).

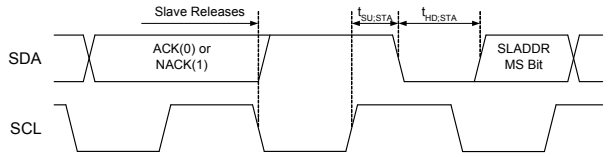


Figure 30. REPEATED START Timing

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Table 15. Bit Definitions for Figure 31, Figure 32

Symbol	Definition
S	START, *see Figure 28*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	REPEATED START, *see Figure 30*
P	STOP, *see Figure 29*

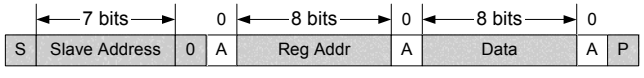


Figure 31. Write Transaction

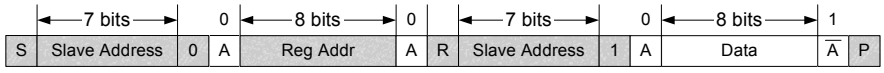


Figure 32. Read Transaction

Register Descriptions

FAN5421 has seven user-accessible registers, described in Table 16.

Table 16. I²C Register Address

Register		Address Bits							
Name	**REG#**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONTROL0	0	0	0	0	0	0	0	0	0
CONTROL1	1	0	0	0	0	0	0	0	1
OREG	2	0	0	0	0	0	0	1	0
IC_INFO	3	0	0	0	0	0	0	1	1
IBAT	4	0	0	0	0	0	1	0	0
SP_CHARGER	5	0	0	0	0	0	1	0	1
SAFETY	6	0	0	0	0	0	1	1	0

Register Bit Definitions

The following table defines the operation of each register bit for all IC versions. Default values are in **bold** text.

Bit	Name	Value	Type	Description
CONTROL0			**Register Address: 00**	**Default Value =X1XX 0XXX**
7	TMR_RST SRST	1	W R	Writing a 1 resets the t_{32SEC} timer. Writing a 0 has no effect. Returns the SRST pin level (1 = HIGH).
6	EN_STAT	0	R/W	Disable STAT pin function. STAT = OPEN
		1		**Enables STAT pin function**
5:4	STAT	00	R	Ready
		01		Charge in progress
		10		Charge done
		11		Fault
3	Reserved	**0**	R	This bit is disabled and always returns 0 when read back.
2:0	FAULT		R	Fault status bits: *see Table 11*
CONTROL1			**Register Address: 01**	**Default Value = 0011 0000 (30H)**
7:6	Reserved	00	R/W	These bits have no effect on the IC operation.
5:4	V_{LOWV}	00	R/W	3.4 V — Weak battery voltage threshold
		01		3.5 V
		10		3.6 V
		11		**3.7 V**
3	TE	**0**	R/W	**Disable charge current termination**
		1		Enable charge current termination
2	$\overline{CE}$	**0**	R/W	**Charger enabled**
		1		Charger disabled
1	HZ_MODE	**0**	R/W	**Not High-Impedance Mode**
		1		High-Impedance Mode
0	Reserved	**0**	R	This bit is disabled and always returns 0 when read back.
OREG			**Register Address: 02**	**Default Value = 0000 1010 (0AH)**
7:2	OREG		R/W	Charger output “float” voltage. Programmable from 3.5 to 4.44 V in 20 mV increments. **Defaults to 000010 (3.54 V)**: *see Table 3*.
1:0	Reserved	**10**	R	These bits are disabled and always returns 10 when read back.

Continued on the following page…

Register Bit Definitions (Continued)

The following table defines the operation of each register bit for all IC versions. Default values are in **bold** text.

Bit	Name	Value	Type	Description
IC_INFO				**Register Address: 03 Default Value = 1001 0XXX**
7:5	Vendor Code	**100**	R	Identifies Fairchild Semiconductor as the IC supplier.
4:3	PN	**00**	R	Part number bits
2:0	REV		R	IC Revision. Revision is 1.X, where X is the decimal of these 3 bits.
IBAT				**Register Address: 04 Default Value = 1000 0001 (81H)**
7	RESET	1	W	Writing a 1 resets all registers parameters, except the Safety register (Reg6), to their defaults. Writing a 0 has no effect. Read returns 1.
6:3	IOCHARGE	Table 5	R/W	Programs the maximum charge current, *see Table 5*.
2:0	ITERM	Table 6	R/W	Sets the current used for charging termination, *see Table 6.*
SP_CHARGER				**Register Address: 05 Default Value = 0010 XX00**
7:6	Reserved	**0**	R	This bit is disabled and always returns 0 when read back.
5	IO_LEVEL	0	R/W	Output current is controlled by IOCHARGE bits.
		1		Voltage across R_{SENSE} for output current control is set to 22.1 mV (325 mA for R_{SENSE}=68 mΩ, 221 mA for 100 mΩ).
4	SP	0	R	Special charger is not active (V_{BUS} is able to stay above V_{SP}).
		1		Special charger has been detected and V_{BUS} is being regulated to V_{SP}.
3	EN_LEVEL	0	R	DISABLE pin is LOW.
		1		DISABLE pin is HIGH.
2:0	VSP	Table 7	R/W	Special charger input regulation voltage, *see Table 7.*
SAFETY				**Register Address: 06 Default Value = 0100 0000 (40H)**
7:4	ISAFE	Table 8	R/W	Sets the maximum $I_{OCHARGE}$ value used by the control circuit, *see Table 8.*
3:0	VSAFE	Table 9	R/W	Sets the maximum V_{OREG} used by the control circuit, *see Table 9*.

PCB Layout Recommendations

Bypass capacitors should be placed as close to the IC as possible.

In particular, the total loop length for CMID should be minimized to reduce overshoot and ringing on the SW, PMID, and VBUS pins.

All power and ground pins must be routed to their bypass capacitors using top copper if possible. Copper area connecting to the IC should be maximized to improve thermal performance.

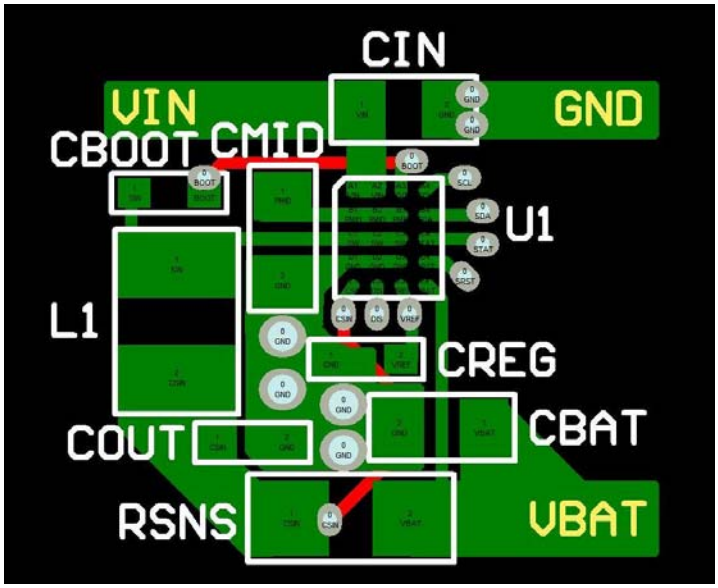
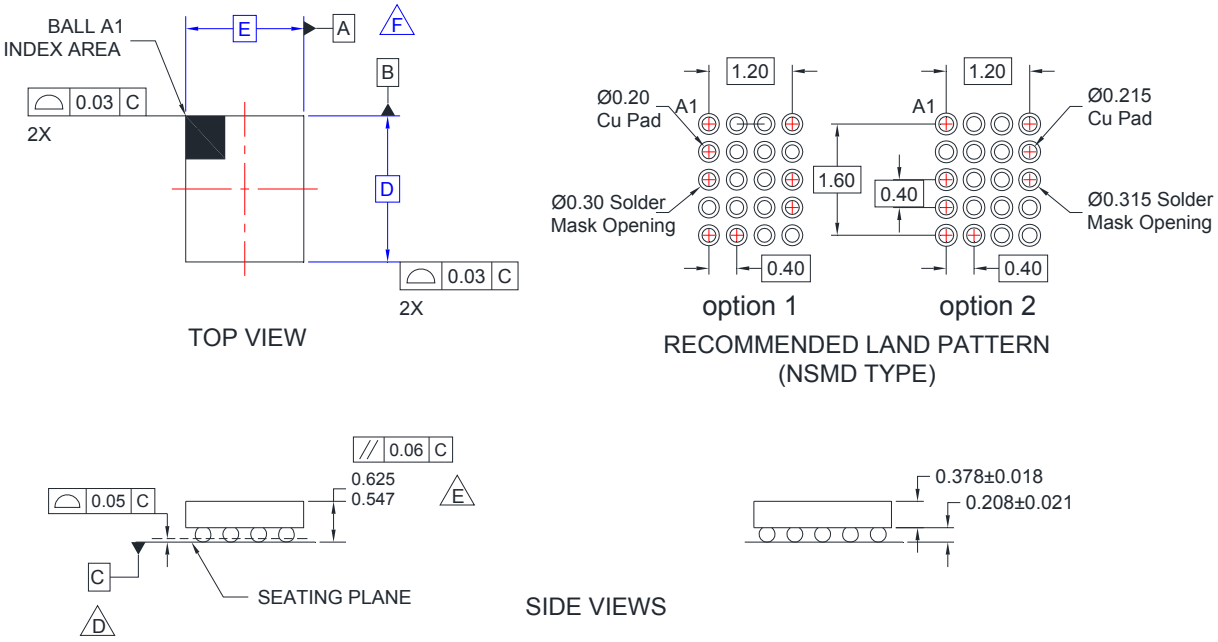


Figure 33. PCB Layout Recommendations

Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC020AArev3.

Figure 34. 2 x 1.82 mm, 20-Bump, 0.4 mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)

Product-Specific Dimensions

Product	D	E	X	Y
FAN5421BUCX	1.960 ±0.030	1.870 ±0.030	0.335	0.180

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