FAN54511

3.2 A Dual Input, Switch Mode Charger with Power Path

ON Semiconductor®

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Description

The FAN5451x family of chargers includes an I^{2}C controlled 3.2 A USB−compliant switch−mode charger.

To facilitate fast system startup, the IC includes an optimized Power Path circuit which also accurately measures battery currents during charging and provides low impedance during discharge.

The charging parameters and operating modes are programmable through an I^{2}C Interface. Charge status is reported back to the host through the I^{2}C port and the / STAT pin.

The FAN5451x provides battery charging in three modes: Pre−Charge (IPP), Constant Current (CC) and Constant Voltage (CV). The charger can automatically restart the charge cycle when the battery falls below a restart voltage threshold. If the input source is removed, the IC enters a high−impedance mode, blocking battery current from leaking to either input.

The FAN5451x is available in a 63−bump, 0.4 mm pitch WLCSP package.

Features

- Fully Integrated, High−Efficiency Charger for Single−Cell Li−Ion and Li−Polymer Battery Packs
- Power Path Circuit ensures Fast System Startup with a Dead Battery
- 95% Charge Efficiency
- Charge Current Programmable up to 3.2 A
- 10 mV Float Voltage Accuracy
- ±5% Charge Current Regulation Accuracy
- 5 V, 1.5 A Boost Mode for USB OTG
- 22 V DC Withstand Voltage on VBUS
- 13.25 V Maximum Input Operating Voltage
- −2 V Input Reverse Polarity Protection

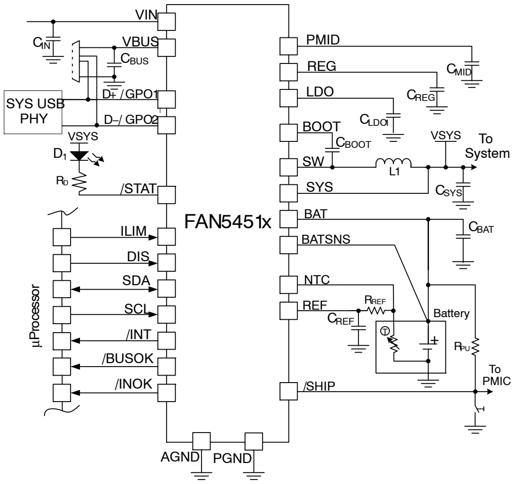


Figure 1. Typical Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Benefits

- Secondary Input for Wireless Charging
- Dynamic Input Voltage Control (DIVC) for Operation with Weak Adapters
- USB BC1.2 Compatible
- Programmable 10 mA LDO
- Programmable Safety Timer with Reset Control
- Pin Configurable Ship Mode prevents Battery Discharge to System Load
- Pin or Software Configurable Hardware Reset for Quick System Restart
- Battery Temperature Sensing Ensures Safe−To−Charge Operation (JEITA)
- Thermal Shutdown and Programmable Thermal Regulation
- High−Speed I^{2}C Interface (3.4 Mb/s) with Fast Mode Plus Compatibility

Applications

- Smart Phones
- Tablets
- e−Books
- Li Ion Powered Devices

April, 2018 − Rev. 4

Table 1. ORDERING INFORMATION

Part Number	Package	Packing Method
FAN54510AUCX	63 − Bump, Wafer−Level Chip_Scale Package (WLCSP) 0.4 mm Pitch	Tape and Reel
FAN54511AUCX		
FAN54511APUCX		
FAN54512AUCX		
FAN54513AUCX		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 2. DEVICE ORDERING INFORMATION

Part Number	Slave Address	PN Bits: IC_INFO[5:3]	BC1.2 Detection	BC1.2 SDP I_{BUS} Current Limit	BC1.2 CDP/DCP I_{BUS} Current Limit	ILIM Pin Control	I_{BUS} Current Limit (ILIM Pin = HIGH)	I_{BUS} Current Limit (ILIM Pin = LOW)
FAN54510A (Note 1)	1101011_	000	ON (D+, D−)	2 min. @500 mA	Safety Timer @1500 mA	OFF	N/A	N/A
FAN54511A	1101011_	001	OFF (GPO1,GPO2)	N/A	N/A	ON	500 mA	1500 mA
FAN54511AP	1101010_	001	OFF (GPO1,GPO2)	N/A	N/A	ON	500 mA	1500 mA
FAN54512A (Note 1)	1101011_	010	ON (D+, D−)	45 min. @100 mA	Safety Timer @1500 mA	OFF	N/A	N/A
FAN54513A	1101011_	011	OFF (GPO1,GPO2)	N/A	N/A	ON	100 mA	1500 mA

1. Contact ON for these options.

STATE DIAGRAMS

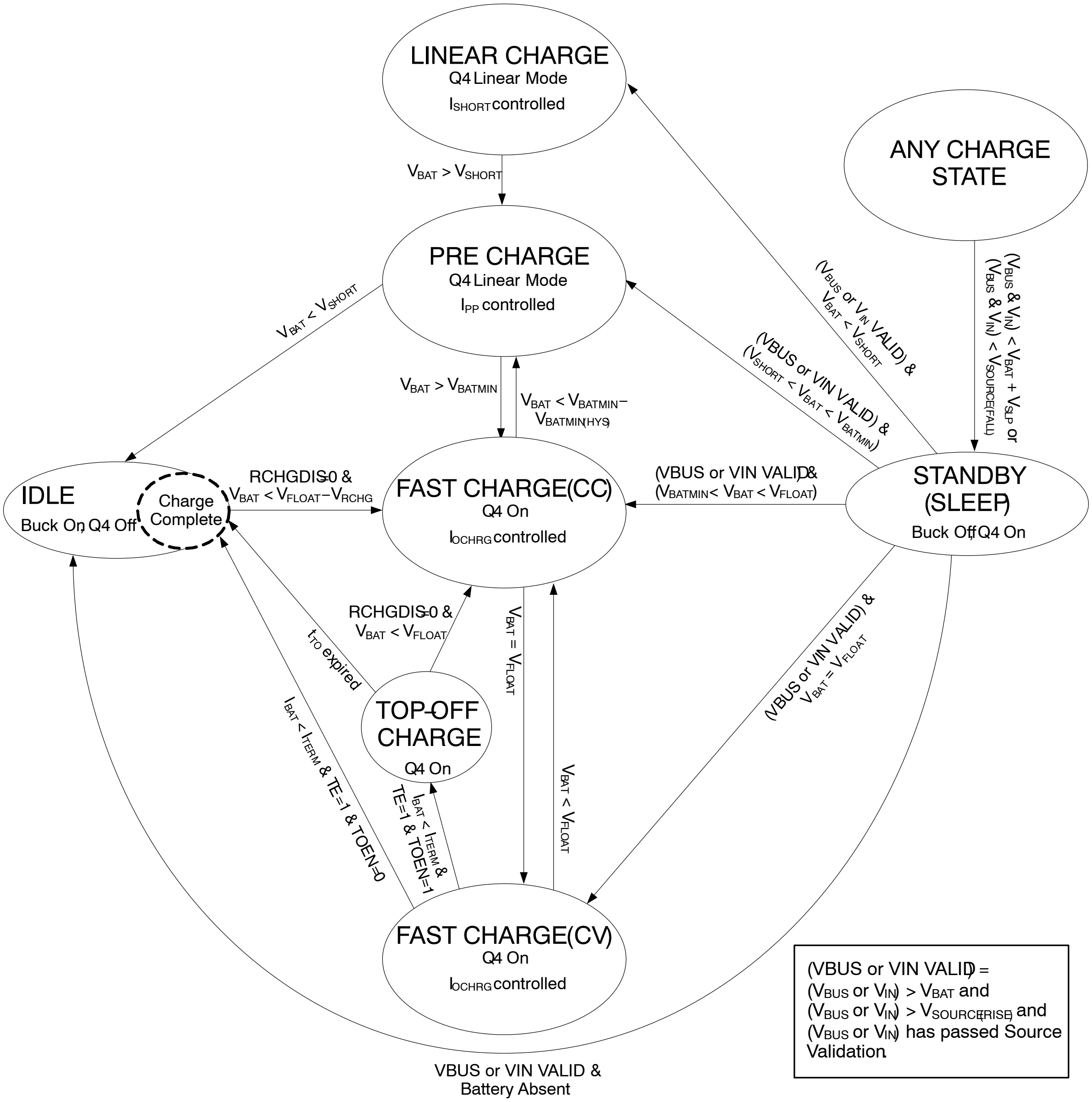


Figure 2. Charger State Diagram: State and Mode Transitions

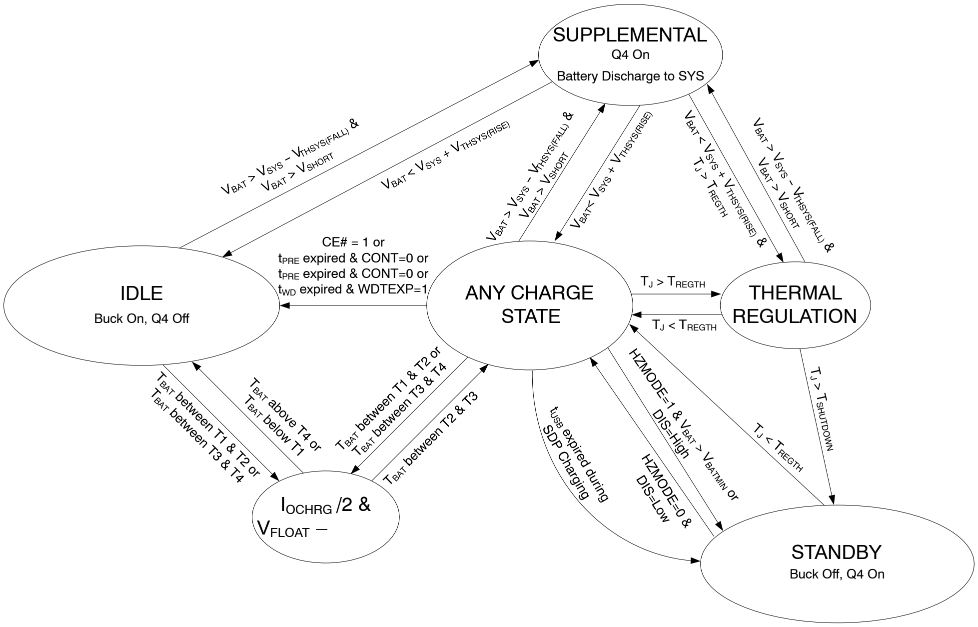


Figure 3. Charger State Diagram: Charger/Battery/System Protection

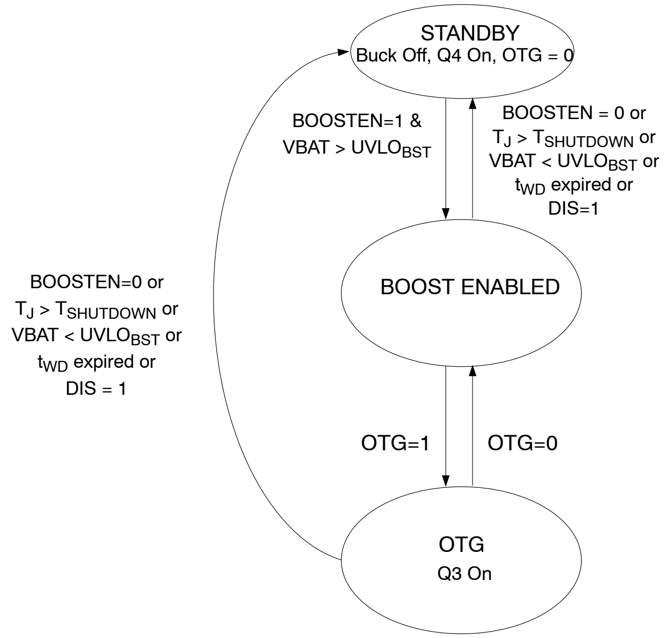


Figure 4. Boost State Diagram

BLOCK DIAGRAM AND SYSTEM DIAGRAMS

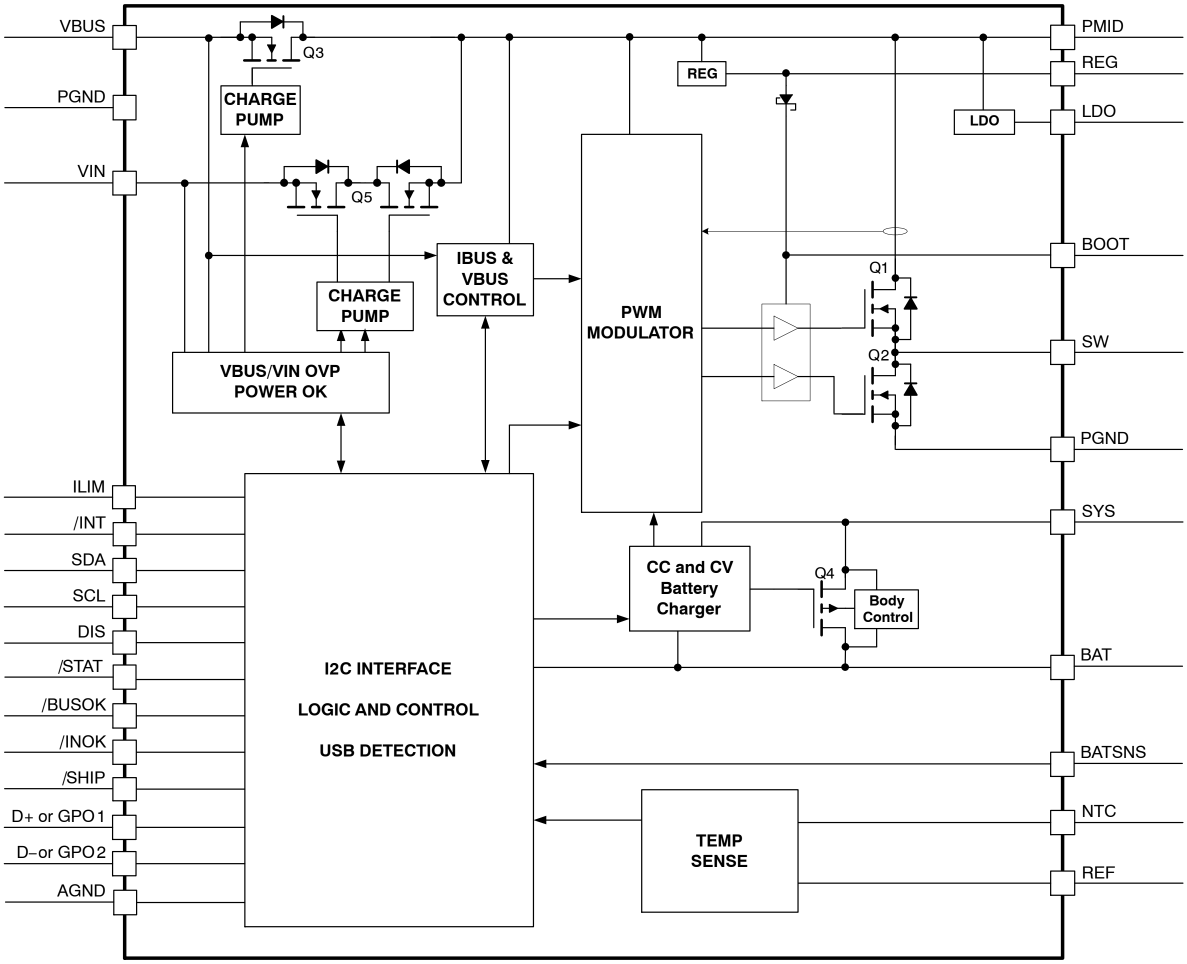


Figure 5. Block Diagram

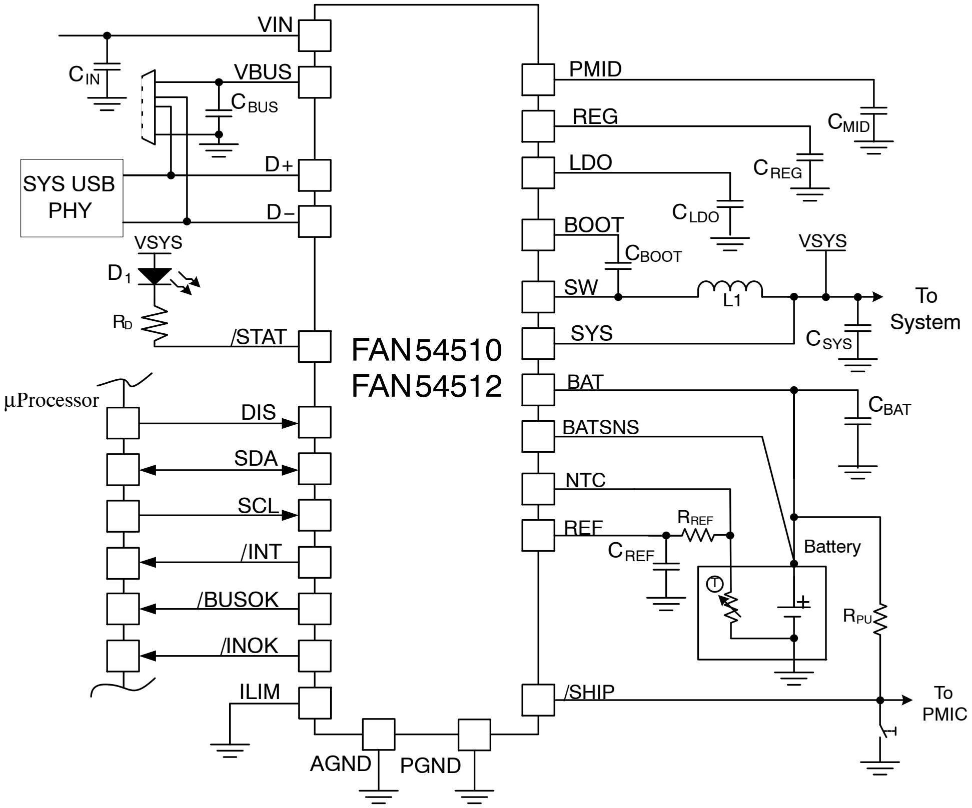


Figure 6. FAN54510A, FAN54512A System Diagram

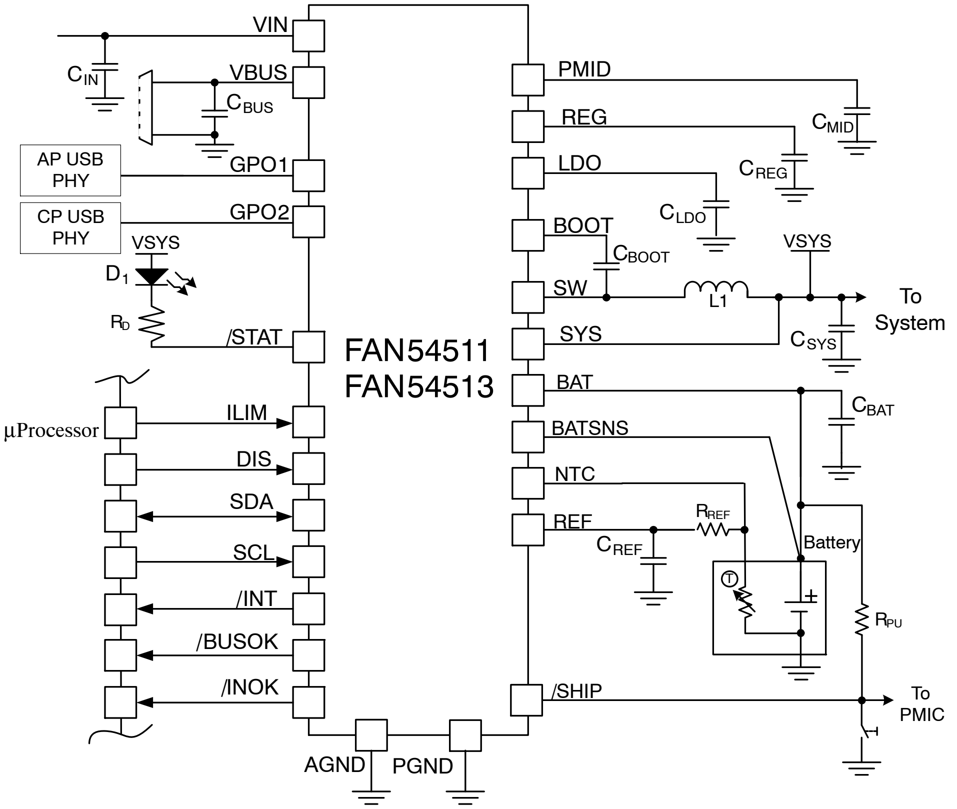


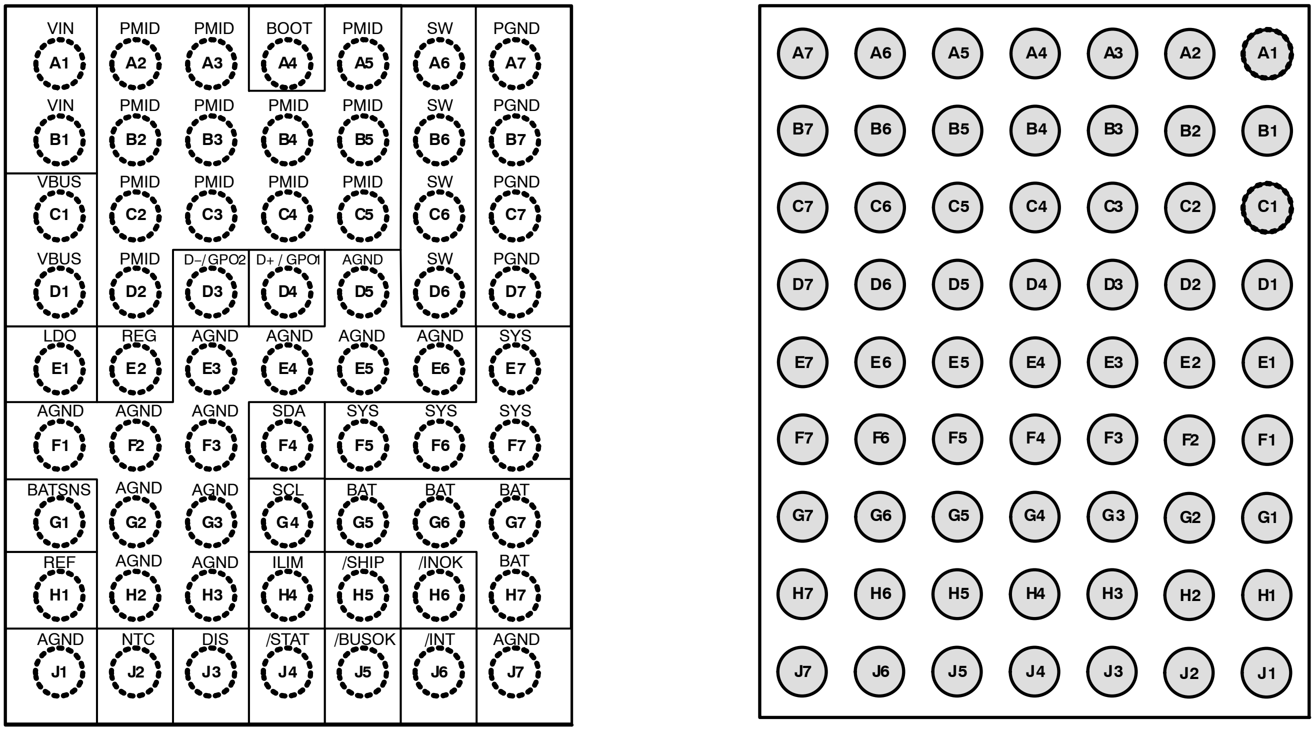
Figure 7. FAN54511A, FAN54511AP, FAN54513A System Diagram

RECOMMENDED EXTERNAL COMPONENTS

Table 3. RECOMMENDED EXTERNAL COMPONENTS

Component	Description	Vendor	Parameter	Typ.	Unit
L1	1.0 μH, +20/−10%, 4.1 A, 2520 x 1.0 mm	SEMCO CIGT252010EH1R0MNE	L	1.0	μH
			DCR	26	mΩ
C_{BAT} (Note 2)	22 μF, 6.3 V, 20%, X5R, 0603	TDK C1608X5R0J226M	C	22	μF
C_{MID} x 2 (Note 3)	10 μF, 25 V, 10%, X5R, 0805	Murata GRM219R61E106M	C	10	
C_{BUS}, C_{IN}	1.0 μF, 25 V, 10% X5R, 0603	Murata GRM188R61E105K TDK: C1608X5R1E105M	C	1.0	nF
C_{SYS} (Note 4)	10 μF, 6.3 V, 20%, X5R, 0603	Murata GRM188R60J106M	C	10	μF
C_{REF}, C_{REG}, C_{LDO}	1.0 μF, 10 V, 20%, X5R, 0402	Murata GRM155R61A105M	C	1.0	
C_{BOOT}	10 nF, 10 V, 10%, X7R, 0201	Murata GRM033R71A103K	C	10	
R_{REF}	10 kΩ		R	10	kΩ
R_{PU}	1 MΩ		R	1	MΩ

2. A minimum effective capacitance of 3.6 μF is required after accounting for tolerance, temperature, and aging.
3. A minimum effective capacitance of 8 μF is required after accounting for tolerance, temperature, and aging.
4. Including CSYS, a minimum effective system capacitance (distributed) of 20 μF after accounting for tolerance, temperature, and aging is required.



Top View **Bottom View**

Figure 8. WLCSP−63 Pin Assignments

Table 4. PIN DEFINITIONS

Pin #	Name	Type	Description
POWER GROUND (LOCAL PGND) REFERENCED PINS			
A1, B1	VIN	P	Wireless Charger Input Voltage. From wireless receiver or second input power source. Bypass VIN to PGND with 1 μF.
C1, D1	VBUS	P	Charger Input Voltage. USB adapter input source also used for the USB−OTG output voltage. Bypass VBUS to PGND with 1 μF.
A2, A3, A5, B2−B5, C2−C5, D2	PMID	PFP	Power Input Voltage. Power input to the charger regulator, bypass point for the input current sense. Bypass PMID to PGND locally with a minimum of 2x C_{MID}.
A6, B6, C6, D6	SW	P	Switching Node. Connect to inductor L1 and CBOOT.
A4	BOOT	P	Bootstrap. High side NMOS Driver Bias. Connect a 10 nF capacitor between BOOT and SW.
E7, F5−F7	SYS	P	System Supply. Connect system load here. Bypass SYS to PGND locally with C_{SYS}.
G5−G7, H7	BAT	P	Battery Voltage. Connect to the positive (+) terminal of the battery pack. Bypass BAT to PGND with C_{BAT}.
E1	LDO	AO	Linear Regulator. LDO is for powering external circuitry. Default output is 4.95 V when VBUS or VIN is valid.
A7, B7, C7, D7	PGND	PG	Power Ground. Power return for gate drive and power transistors. The connection from these pins to the ground pads of C_{MID} and C_{SYS} should be as short as possible. Refer to Recommended Component Placement.
ANALOG GROUND (AGND) REFERENCED PINS			
E2	REG	AFP	Internal Regulator. Bypass with a 1 μF capacitor to AGND
G1	BATSNS	AI	Battery Voltage Sense. Connect this pin as close to battery terminal as possible using a single trace. Do not use as a power pin.
H1	REF	AO	Reference Voltage. REF is a 1.8 V regulated output used in conjunction with the NTC pin to determine the battery temperature. Connect to a 1 μF capacitor to AGND.
J2	NTC	AI	Negative Temperature Coefficient Resistor. Pin is connected to the NTC terminal of the battery pack with a 10 kΩ external pull−up resistor to the REF pin. Note: Other values of the pull/up resistor and NTC may be used. See applications section for more detail.
D5, E3−E6, F1−F3, G2, G3, H2, H3, J1, J7	AGND	AGND	Analog Ground. All IC signals are referenced to this node. Connect to PGND at a single point. Refer to Recommended Component Placement.
SYSTEM GROUND (PGND) REFERENCED PINS			
D4	D+	AI/O	Positive USB data line (FAN54510A, FAN54512A only). Used for BC1.2 adapter detection of SDP, DCP, or CDP device connection.
	GPO1	DO	General Purpose Output 1 (FAN54511A, FAN54511AP, FAN54513A only). CMOS output driver that is sourced from the LDO output.
D3	D−	AI/O	Negative USB data line (FAN54510A, FAN54512A only). Used for BC1.2 detection of SDP or DCP/CDP device connection.
	GPO2	DO	General Purpose Output 2 (FAN54511A, FAN54511AP, FAN54513A only). CMOS output driver that is sourced from the LDO output
F4	SDA	DI/O	I^2C Interface Serial Data. Open−drain, Bi−directional I^2C serial data line. This pin should not be left floating.
G4	SCL	DI	I^2C Interface Serial Clock. I^2C communication clock input. This pin should not be left floating.
H4	ILIM	DI	Input Current Limit for VBUS (FAN54511A, FAN54511AP, FAN54513A only). Input LOW sets the input current limit to 1.5 A and HIGH sets to 500 mA (FAN54511A, FAN54511AP only) or 100 mA (FAN54513A only). This pin is internally pulled down through a 1 MΩ resistor. ILIM pin functionality is disabled for FAN54510A and FAN54512A versions where it is recommended to tie ILIM to AGND or PGND.

H5	/SHIP	DI	Ship Mode Enable (Active−Low). If this pin is held LOW for more than $t_{SHIPENTER}$ during any other state, Ship Mode is entered and the battery is fully isolated from the system load. If /SHIP is held LOW again for more than $t_{SHIPEXIT}$, Ship mode is disabled and Q4 is configured to allow the battery to discharge to the system load. Ship mode can also be exited, automatically, by applying a valid input source. Tie this pin to BAT using a 1 MΩ pull−up resistor for devices with embedded batteries.
H6	/INOK	DO	VIN Power Okay (Active−Low). Active low, open−drain output indicates that the input source voltage at VIN has risen above $V_{SOURCE(RISE)}$ and passed validation, and a valid VBUS is not present. /INOK remains low while $V_{IN\ (FALL)} < V_{IN} < V_{INOVP}$ and $V_{IN} > V_{BAT.}$ /INOK will be HIGH if /BUSOK is LOW.
J4	/STAT	DO	Status (Active−Low). Open−drain output indicating charge status. The IC pulls this pin LOW when charging is in progress, and can be used to signal the host processor or drive an LED.
J5	/BUSOK	DO	VBUS Power Okay (Active−Low). Active low, open−drain output indicates that the input source voltage at VBUS has risen above $V_{SOURCE(RISE)}$ and passed validation. /BUSOK remains low while $V_{BUS\ (FALL)} < V_{BUS} < V_{BUSOVP}$ and $V_{BUS} > V_{BAT.}$
J6	/INT	DO	Interrupt (Active−Low). Active low, open−drain output indicates that an interrupt bit or bits have been set. This pin is reset to HIGH after all set interrupt register bit(s) are read. This pin is not pulled LOW when an interrupt occurs that is masked by the associated mask bit.
J3	DIS	DI	Disable. If this pin is held HIGH, the PWM converter is disabled, creating a high impedance path between VBUS/VIN and SYS. This pin has an internal 1 MΩ pull−down.

5. Pin Types−A = Analog, D = Digital, P = Power, I = Input, O = Output, G = Ground, FP = Filter Point

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Table 5. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DC}	VBUS, PMID Voltage, Maximum Slew Rate of 2 V/μs (Note 6)		−2.0	22.0	V
	VIN Voltage, Maximum Slew Rate of 2 V/μs (Note 6)		−2.0	16.0	
	BOOT Voltage		−0.3	19.0	
	SW Voltage	DC	−0.3	14.0	
		Transient: < 5 ns	−1.0	17.0	
	SYS, BAT Voltage		−0.3	6.5 (Note 7)	
V_{DCO}	Voltage on Other Pins		−0.3	6.5 (Note 7)	
ESD	Electrostatic Discharge Protection Level, HBM per JESD22−A114	VBUS, PMID, VIN, BOOT, SW	1250		V
		All Other Pins	2000		
	Electrostatic Discharge Protection Level, CDM per JESD22−C101	All Pins	1500		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

6. Positive slew rate applies only to voltages above the VIN_OVP or VBUS_OVP threshold.
7. Lesser of 6.5 V or V_{BAT} + 0.3 V.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. On Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Table 6. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min.	Max.	Unit
V_{BUS}, V_{IN}	Supply Voltage		4.50	13.25	V
T_A	Ambient Temperature		−30	+85	°C
T_J	Junction Temperature		−30	+100	°C
C_{BAT}	Minimum Effective Capacitance on VBAT		3.6		μF
C_{MID}	Minimum Effective Capacitance on PMID	V_{BST} = 5 V	8		μF
$C_{SYS\_DISTRIBUTED}$	Minimum Effective Capacitance on SYS (includes C_{SYS} and distributed system capacitance)		20		μF
C_{LDO}	Minimum Effective Capacitance on LDO		0.4		μF
C_{REG}	Minimum Effective Capacitance on REG		0.4		μF

THERMAL PROPERTIES

Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four−layer 2s2p boards without vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Table 7. THERMAL PROPERTIES

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	40	°C/W
Ψ_{JB}	Junction−to−Board Thermal Characterization Parameter (Evaluation Board)	4.3	°C/W

Table 8. ELECTRICAL SPECIFICATIONS

Unless otherwise specified: V_{BUS} = 5.0 V; V_{BAT} = 3.7 V; HZMODE = “0”; BOOSTEN = “0” (Charge Mode); TREGTH = 120°C; I_{REG} = I_{LDO} = 0 A; SCL, SDA = 0 or 1.8 V; and typical values are for T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
I_{SOURCE}	V_{BUS} or V_{IN} Current	$V_{BUS} > V_{SOURCE(RISE)}$; V_{IN} Open; PWM Switching; $I_{BAT} = I_{SYS}$ = 0 A		4		mA
		$V_{IN} > V_{SOURCE(RISE)}$; V_{BUS} Open; PWM Switching; $I_{BAT} = I_{SYS}$ = 0 A		4		mA
		HZMODE= “1”; $V_{SOURCE} > V_{SOURCE(RISE)}$, NTC = GND		200	400	µA
I_{BAT_HZ}	Battery Discharge Current	Sleep State; $V_{BUS} = V_{IN}$ = Open or 0V; V_{BAT} = 4.2 V		3	10	µA
		Ship Mode State; $V_{BUS} = V_{IN}$ = Open or 0 V; V_{BAT} = 4.2 V		0.8	10	µA
		DIS = HIGH or HZMODE=“1”; V_{BUS}=5 V; V_{IN} = Open; V_{BAT} = 4.2V ; I_{SYS} = 0 A		1	10	µA
		DIS = HIGH or HZMODE =“1”; V_{BUS} = Open; V_{IN} = 5V; V_{BAT} = 4.2V; I_{SYS} = 0 A		1	10	µA
I_{SOURCE_HZ}	Battery Leakage Current to V_{BUS} in High−Impedance Mode	V_{BUS} = 0 V; V_{IN} = Open; V_{BAT} = 4.2 V; I_{SYS} = 0 A		0.2	5.0	µA
	Battery Leakage Current to V_{IN} in High−Impedance Mode	V_{IN} = 0 V; V_{BUS} = Open; V_{BAT} = 4.2 V; I_{SYS} = 0 A		0.2	5.0	µA
CHARGER VOLTAGE REGULATION						
V_{FLOAT}	Charge Voltage Range		3.30		4.72	V
	Charge Voltage Accuracy	T_J = 25°C; V_{FLOAT} = 4.20 V to 4.50 V	−6		+6	mV
		T_J = 0 to 70°C; V_{FLOAT} = 4.20 V to 4.50 V	−10		+10	
		T_J = −25 to 85°C; V_{FLOAT} = All Settings	−25		+25	
FAST CHARGE CURRENT REGULATION						
I_{OCHRG}	Output Charge Current Range	$V_{BATMIN} < V_{BAT} < V_{FLOAT}$	200		3200	mA
	Charge Current Accuracy	$I_{OCHRG} \geq$ 500 mA, −30°C $< T_A <$ 85°C	−5		+5	%
		$I_{OCHRG} <$ 500 mA, −30°C $< T_A <$ 85°C	−10		+10	
PRE−CHARGE CURRENT CONTROL						
I_{pp}	Pre−Charge Current Range		200		800	mA
	Pre−Charge Current Accuracy		−15		+15	%
I_{SHORT}	Linear Charging Current	$V_{BAT} < V_{SHORT}$	45	55	65	mA

Table 8. ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: V_{BUS} = 5.0 V; V_{BAT} = 3.7 V; HZMODE = "0"; BOOSTEN = "0" (Charge Mode); TREGTH = 120°C; I_{REG} = I_{LDO} = 0 A; SCL, SDA = 0 or 1.8 V; and typical values are for T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CHARGE TERMINATION DETECTION						
I_{TERM}	Termination Current Threshold Range	$V_{BAT} > V_{FLOAT} - V_{RCHG}$; $V_{BUS} > V_{BAT}$	25		600	mA
	Termination Current Threshold Accuracy	ITERM Setting > 200 mA	−10		+10	%
		ITERM Setting = 100 mA to 200 mA	−20		+20	
	Termination Current Deglitch Time			30		ms
WEAK BATTERY DETECTION						
V_{LOWV}	Weak Battery Threshold Range		3.0		3.7	V
	Hysteresis	FAN54512A Only		100		mV
		All Other Part Numbers		3		
	Termination Current Threshold Accuracy		−5		+5	%
	Weak Battery Deglitch Time	Rising Voltage; 2 mV Overdrive		30		ms
MINIMUM BATTERY VOLTAGE DETECTION						
V_{BATMIN}	Pre−charge to Fast Charge Transition Threshold Range		2.7		3.4	V
	Hysteresis		180	265	350	mV
	Threshold Accuracy		−5		+5	%
	Deglitch Time			30		ms
BATTERY RECHARGE THRESHOLD						
V_{RCHG}	Recharge Threshold	Below V_{FLOAT}; T_J = 25°C		170		mV
	Deglitch Time	V_{BAT} falling below V_{RCHG} threshold		130		ms
SHORTED BATTERY THRESHOLD						
V_{SHORT}	Battery Short−Circuit Threshold	V_{BAT} Rising	1.94	2.00	2.06	V
BATTERY FET SUPPLEMENTAL CONTROL						
V_{THSYS}	BAT to SYS Threshold for BATFET Gate transition while charging	$V_{SYS} - V_{BAT}$, Falling V_{SYS}	−6	−5	−4	mV
		$V_{SYS} - V_{BAT}$, Rising V_{SYS}	0	1	2	
BATTERY TEMPERATURE DETECTION						
T1	T1 (0°C) Temperature Threshold		71.9	73.9	75.9	% of VREF
T2	T2 (10°C) Temperature Threshold		62.6	64.6	66.6	
T3	T3 (45°C) Temperature Threshold		30.9	32.9	34.9	
T4	T4 (60°C) Temperature Threshold		21.3	23.3	25.3	
V_{JEITA} (Note 9)	FLOAT Voltage Reduction During JEITA Region	V_{FLOAT} = 4.35 V	160	200	240	mV

Table 8. ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: V_{BUS} = 5.0 V; V_{BAT} = 3.7 V; HZMODE = “0”; BOOSTEN = “0” (Charge Mode); TREGTH = 120°C; I_{REG} = I_{LDO} = 0 A; SCL, SDA = 0 or 1.8 V; and typical values are for T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
INPUT POWER SOURCE DETECTION						
$V_{SOURCE(RISE)}$	V_{BUS} or V_{IN} Input Voltage Rising	To Initiate Source Validation	4.30	4.40	4.52	V
$V_{SOURCE(FALL)}$	Minimum V_{BUS} or V_{IN}	During Charging, V_{BAT} < 3.6 V	3.55	3.70	3.80	V
V_{SLP}	Sleep−Mode Entry Threshold, $V_{SOURCE} - V_{BAT}$	$V_{SOURCE(FALL)} \leq V_{BAT}$	0	40	100	mV
$t_{SRCQUAL}$	V_{BUS} or V_{IN} Input Qualification Time			32		ms
t_{VSC_VALID}	V_{BUS} or V_{IN} Input Validation Time			32		ms
$I_{VSOURCE}$	V_{BUS} or V_{IN} Input Validation Current			50		mA
DIVC CONTROL LOOP						
$V_{SOURCE(LIM)}$	Input Voltage Loop Setpoint Accuracy		−3		+3	%
INPUT CURRENT LIMIT						
I_{BUSLIM}	V_{BUS} Input Current Limit Range		100		3000	mA
	V_{BUS} Input Current Limit Threshold	ILIM = HIGH (100 mA) FAN54513A Only	86	93	100	
		ILIM = HIGH (500 mA) FAN54511A, FAN54511AP Only	460	480	500	
		ILIM = LOW (1.5 A); FAN54511A, FAN54511AP, FAN54513A Only	1380	1440	1500	
		IBUSLIM (REG 14h[6:0]) = “00h”	86	93	100	
		IBUSLIM (REG 14h[6:0]) = “10h”	460	480	500	
		IBUSLIM (REG 14h[6:0]) = “74h”	2760	2880	3000	
I_{INLIM}	V_{IN} Input Current Limit Range		325		2000	mA
	V_{IN} Input Current Limit Threshold	INLIM (REG 16h[6:0]) = “1Bh”	920	960	1000	
		INLIM (REG 16h[6:0]) = “43h”	1840	1920	2000	
LOW DROP OUT REGULATOR						
V_{LDOACC}	LDO Voltage Accuracy	$V_{PMID} \geq V_{LDO}$ + 500 mV; I_{LDO} = 1 mA	−5		+5	%
I_{LDO}	Current Rating	$V_{PMID} = V_{LDO}$ + 500 mV	10			mA
$VLDO_{DROP}$ (Note 10)	Drop Out Voltage	I_{OUT} = 10 mA		170		mV
$RLDO_{PD}$	LDO Pull Down Resistance when Disabled	LDO Off		1.2		kΩ
IQ_{LDO}	LDO Quiescent Current	LDO On, $V_{PMID} = V_{LDO}$ + 500 mV		20	40	μA
REG_{LDO}	LDO Load Regulation	$V_{PMID} = V_{LDO}$ + 500 mV; 10 μA < $I_{OUT} \leq$ 10 mA		50		mV

Table 8. ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: V_{BUS} = 5.0 V; V_{BAT} = 3.7 V; HZMODE = “0”; BOOSTEN = “0” (Charge Mode); TREGTH = 120°C; I_{REG} = I_{LDO} = 0 A; SCL, SDA = 0 or 1.8 V; and typical values are for T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
GPO1, GPO2 (FAN54511A, FAN54511AP, FAN54513A ONLY)						
$V_{(OL)}$	Output Low	I_{SINK} = 5 mA			0.3	V
$V_{(OH)}$	Output High	I_{SOURCE} = 5 mA	V_{LDO} – 200 mV			V
V_{REF} BIAS GENERATOR						
V_{REF}	Bias Regulator Voltage	V_{SOURCE} > $V_{SOURCE(MIN)}$		1.8		V
	Short−Circuit Current Limit			2.5		µA
/STAT, /BUSOK, /INOK, /INT, SDA						
$V_{(OL)}$	Output Low	I_{SINK} = 5 mA			0.4	V
$I_{(OH)}$	Output High Leakage Current	VDD = 5 V			1	µA
LOGIC LEVELS: SDA, SCL, /SHIP, ILIM, DIS						
V_{IH}	High−Level Input Voltage		1.05			V
V_{IL}	Low−Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input Tied to GND or V_{BUS}		0.01	1.00	µA
DIS, ILIM						
R_{PD} (Note 11)	Pull Down Resistance			1		MΩ
D+/D− DETECTION (FAN54510A, FAN54512A ONLY)						
V_{DP_SRC}	D+ Source Voltage	0 to 300 µA	0.5	0.6	0.7	V
V_{DM_SRC}	D− Source Voltage	0 to 300 µA	0.5	0.6	0.7	V
V_{DAT_REF}	Data Detect Voltage		0.25		0.40	V
I_{DP_SRC}	Data Contact Detect Current Source		7		13	µA
I_{DP_SNK}	D+ Sink Current		25		175	µA
I_{DM_SNK}	D− Sink Current		25		175	µA
V_{LGC_HI}	Logic High Threshold		2			V
V_{LGC_LO}	Logic Low Threshold				0.8	V
R_{DM_DWN}	D− Pulldown Resistor		14.25		24.80	kΩ
C_{OFF} (Note 9)	D+, D− Off Capacitance	D+, D− = Hi−Z; f = 1 MHz, V_{BIAS} = 0.2 V		4		pF
BATTERY ABSENCE DETECTION						
I_{DETECT} (Note 12)	Battery Detection Current before Charge Done (Sink Current)	Begins after Termination Detected and before $V_{BAT} \leq V_{FLOAT} - V_{RCHG}$		−8		mA
t_{DETECT}	Battery Detection Time			262		ms

Table 8. ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: V_{BUS} = 5.0 V; V_{BAT} = 3.7 V; HZMODE = “0”; BOOSTEN = “0” (Charge Mode); TREGTH = 120°C; I_{REG} = I_{LDO} = 0 A; SCL, SDA = 0 or 1.8 V; and typical values are for T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POWER SWITCHES						
$R_{DS(ON)}$	Resistance of VBUS Blocking FET (Q3)	VBUS to PMID; I_{BUS} = 300 mA		360		mΩ
		VBUS to PMID; I_{BUS} = 900 mA		82		
		VBUS to PMID; I_{BUS} = 3000 mA		28		
	Resistance of VIN Blocking FET (Q5)	VIN to PMID		135		
	Resistance of Buck High Side FET (Q1)	PMID to SW		24		
	Resistance of Buck Low Side FET (Q2)	SW to GND		19		
	Resistance of BATFET (Q4)	SYS to BAT; VBAT = 4.2 V; I_{OCHG} = 500 mA		55		
		SYS to BAT; VBAT = 4.2 V; I_{OCHG} = 1.5 A		15		
CHARGER PWM MODULATOR						
f_{SW}	Oscillator Frequency			1.5		MHz
D_{UTY} (Note 9)	Duty Cycle		0		99.6	%
BOOST MODE OPERATION (BOOSTEN (REG 1Ch[5]) = OTG (REG 1Ch[6]) = “1”)						
V_{BOOST}	Programmable Boost Output Voltage Range	2.5 V < V_{BAT} < 4.5 V	4.940		5.347	V
	Boost Output Voltage at VBUS	2.5 V < V_{BAT} < 4.5 V; V_{BST} = 5 V; I_{LOAD} from 0 to 900 mA	4.85	5.00	5.25	
		3.0 V < V_{BAT} < 4.5 V; V_{BST} = 5 V; I_{LOAD} from 0 to 1500 mA	4.75	5.00	5.25	
$I_{BAT(BOOST)}$	Boost Mode Quiescent Current	V_{BAT} = 3.6 V; I_{LOAD} = 0 A		300	575	μA
$I_{LIMPK(BST)}$ (Note 9)	Q2 Peak Current Limit		3.3	4.1	5.7	A
$UVLO_{BST}$	Minimum Battery Voltage for Boost Operation	While Boost Active		2.32		V
		To Start Boost Regulator		2.48	2.70	
PROTECTION AND TIMERS						
V_{BUSOVP}	VBUS Over−Voltage Threshold	V_{BUS} Rising; VBUSOVP (REG 15h[5:4]) = “00”	6.35	6.50	6.65	V
		V_{BUS} Rising; VBUSOVP (REG 15h[5:4] = “01”	10.25	10.50	10.75	
		V_{BUS} Rising; VBUSOVP (REG 15h[5:4] = “10”	13.4	13.7	14.0	
$V_{BUSOVP(HYS)}$	V_{BUSOVP} Hysteresis	V_{BUS} Falling		100		mV

Table 8. ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified: V_{BUS} = 5.0 V; V_{BAT} = 3.7 V; HZMODE = “0”; BOOSTEN = “0” (Charge Mode); TREGTH = 120°C; I_{REG} = I_{LDO} = 0 A; SCL, SDA = 0 or 1.8 V; and typical values are for T_A = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PROTECTION AND TIMERS						
V_{INOVP}	V_{IN} Over–Voltage Threshold	V_{IN} Rising; VINOVP (REG 17h[5:4]) = “00”	6.35	6.50	6.65	V
		V_{IN} Rising; VINOVP (REG 17h[5:4]) = “01”	10.25	10.50	10.75	
		V_{IN} Rising; VINOVP (REG 17h[5:4]) = “10”	13.4	13.7	14.0	
$V_{BUSOVP(HYS)}$	V_{INOVP} Hysteresis	V_{IN} Falling		100		mV
V_{BOOST_OVP}	Boost Over–Voltage Threshold	BOOSTEN (REG 1Ch[5] = “1”; V_{BUS} Rising	5.8	5.9	6.1	V
	Hysteresis	V_{BUS} Falling		100		mV
V_{BAT_OVP}	Battery Over–Voltage Threshold	Rising	1.025* V_{FLOAT}	1.050* V_{FLOAT}	1.075* V_{FLOAT}	V
	Hysteresis	V_{BAT} Falling relative to Rising Threshold		1		%
$I_{LIMPK(CHG)}$ (Note 9)	High–Side Cycle–by–Cycle Peak Current Limit (Q1)	Charge Mode	4.6	4.9	5.4	A
$I_{LIMQ4SC}$	Q4 Short Circuit Current Limit		6.6	9.0		A
t_{SCQUAL}	Q4 Short Circuit Qualification Time			1		ms
$t_{SCRECOV}$	Q4 Short Circuit Recovery Time			2		sec
$t_{SHIPENTER}$	Hardware Ship Mode Entry Time	Not in Ship Mode		8		sec
$t_{SHIPEXIT}$	Hardware Ship Mode Exit Time	In Ship Mode		4		sec
$T_{SHUTDOWN}$ (Note 9)	Thermal Shutdown Threshold during Charging	T_J Rising		150		°C
	Hysteresis	T_J Falling		T_{REGTH}		
T_{REGTH} (Note 9)	Thermal Regulation Threshold during Charging or Thermal Shutdown Threshold during Boost Operation	REG 0Fh[6:5]) = ”10”		100		°C
t_{INT}	Battery Detection Interval while the Battery is Removed			2.1		sec
t_{FAST}	Safety Timer – Fast Range		240		960	min
t_{PRE}	Safety Timer – Pre Range		1.667		36.000	min
t_{TO}	Top Off Timer		10		70	min
t_{USB}	USB Timer	FAN54510A SDP Attached		100	120	sec
		FAN54512A SDP Attached		36	45	min
t_{SAFE_ACC}	Safety Timer Accuracy		–20		20	%
t_{WD}	Watch Dog Timer	Charger Enabled	80	100	120	sec
		Charger Disabled	73	100	127	%
Δt_{L_F} (Note 13)	Low–Frequency Timer Accuracy	Charger Inactive	–27		27	%

8. Limits over the recommended temperature operating range (–30 to 85 °C) are correlated by statistical quality control methods.
9. Guaranteed by design and/or Characterization; not tested in production.
10. Dropout voltage is determined by reducing the LDO input voltage until the LDO output voltage falls to 98% of its regulated voltage. Under this condition, PMID – VLDO (MEASURED) = VLDODROP.
11. In LOW state, the pull–down is present. In HIGH state, the pull–down is released.
12. Negative current is current flowing from the battery to GND (discharging the battery).
13. This tolerance (%) applies to all timers on the IC, including soft–start and deglitch timers.

Table 9. I^{2}C TIMING SPECIFICATIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	
		Fast Mode Plus			1000	
		High−Speed Mode, $C_B \leq$ 100 pF			3400	
		High−Speed Mode, $C_B \leq$ 400 pF			1700	
t_{BUF}	Bus−free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		
		Fast Mode Plus		0.5		
$t_{HD;STA}$	START or Repeated START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		Fast Mode Plus		0.5		µs
		High−Speed Mode, $C_B \leq$ 100 pF		160		ns
		High−Speed Mode, $C_B \leq$ 400 pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode, $C_B \leq$ 100 pF		60		ns
		High−Speed Mode, $C_B \leq$ 400 pF		120		ns
$t_{SU;STA}$	Repeated START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		Fast Mode Plus		260		ns
		High−Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		
		Fast Mode Plus		50		
		High−Speed Mode		10		
$t_{HD;DAT}$	Data Hold Time	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		Fast Mode Plus	0		450	ns
		High−Speed Mode, $C_B \leq$ 100 pF	0		70	ns
		High−Speed Mode, $C_B \leq$ 400 pF	0		150	ns

Table 9. I^2C TIMING SPECIFICATIONS (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, $C_B \leq 100$ pF		10	80	
		High−Speed Mode, $C_B \leq 400$ pF		20	160	
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, $C_B \leq 100$ pF		10	40	
		High−Speed Mode, $C_B \leq 400$ pF		20	80	
t_{RCL1}	Rise Time of SCL after a Repeated START Condition and after ACK Bit	High−Speed Mode, $C_B \leq 100$ pF		10	80	ns
		High−Speed Mode, $C_B \leq 400$ pF		20	160	
t_{RDA}	SDA Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, $C_B \leq 100$ pF		10	80	
		High−Speed Mode, $C_B \leq 400$ pF		20	160	
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		Fast Mode Plus	$20+0.1C_B$		120	
		High−Speed Mode, $C_B \leq 100$ pF		10	80	
		High−Speed Mode, $C_B \leq 400$ pF		20	160	
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		μs
		Fast Mode		600		ns
		Fast Mode Plus		120		ns
		High−Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

CIRCUIT OVERVIEW

The FAN5451x combines a highly integrated synchronous buck regulator for battery charging and providing system power. The converter can also operate as a boost regulator, which can supply 5 V to USB On−The−Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost operations to maintain high efficiency over a wide range of adapter input voltage and battery voltages.

With dual inputs, the charger can quickly switch between multiple power sources. For example, the charger can be powered from a wireless power receiver until plugged into a traditional USB or wall adapter.

An integrated Power Path FET facilitates fast system startup. This FET also accurately senses charging current, thus eliminating the need for an external sense resistor. Additionally, the FET provides a low impedance path from the battery to the system.

OPERATING MODES

The FAN5451x has seven operating modes:

Linear Mode:

When $V_{BAT} < V_{SHORT}$ (2.0 V), the buck converter regulates voltage at SYS and provides the system current enabling instant turn on of the system. The BATFET (Q4) charges the battery at the I_{SHORT} current to safely recover the battery.

Pre−Charge Mode:

Above V_{SHORT}, the buck converter regulates voltage at SYS and provides the system current. The BATFET (Q4) is operated as a linear current source to pre−charge the battery under I_{PP} control.

Fast Charge Mode:

The BATFET (Q4) is fully enhanced, charging the battery under I_{OCHRG} control either in the Constant Current Mode or Constant Voltage Mode from the output of the buck regulator.

System Mode (Idle State):

The buck converter regulates voltage at SYS and provides the system current, while the battery is not being charged. This mode can occur if the battery charging has terminated or charging is disabled.

Supplemental Mode

The buck converter cannot produce enough current to maintain V_{SYS} above $V_{BAT.}$ The BATFET (Q4) is fully enhanced to provide supplemental current from the battery to the system load.

Boost Mode

Q1 and Q2 operate as a synchronous boost regulator to provide power to the VBUS pin for USB−On−the−Go (OTG) applications using the battery as its input. The boost converter output voltage is programmable.

High−Impedance Mode (Standby State)

Both the boost and charging circuits are OFF and the battery is providing current to the system. Current flow from VBUS or VIN to the battery or from the battery to VBUS or VIN is blocked.

CONFIGURABLE CHARGE PARAMETERS

The following charging parameters can be programmed by the host through I^2C:

Pre−Charge Current Regulation (I_{PP})

Limits the maximum battery charging current when $V_{SHORT} < V_{BAT} < V_{BATMIN}$. The default setting is 450 mA.

See *PRECHG* (REG 13h[3:0])

Minimum Battery Threshold (V_{BATMIN})

Sets the battery voltage threshold for transitioning between Pre−Charge and Fast Charge. V_{BATMIN} should not be set lower than the minimum required system voltage. The default setting is 3.4 V.

See *VBATMIN* (REG 0Ch[2:0])

Regulated System Voltage (V_{SYS})

Regulates the system voltage when $V_{BAT} < V_{BATMIN}$. VSYS should be programmed 200 mV, or more, above the minimum required system voltage. The default setting is 3.6 V.

See *VSYS* (REG 0Dh[1:0])

Fast Charge Current Regulation (I_{OCHRG})

Limits the maximum battery charging current when $V_{BAT} > V_{BATMIN}$. The default setting is 1000 mA.

See *IOCHRG* (REG 12h[5:0])

Thermal Regulation (T_{REG})

Limits charge current to prevent the IC from overheating. The default setting is 100°C.

See *TREGTH* (REG 0Fh[6:5])

Output Voltage Regulation (V_{FLOAT})

Maximum battery charging voltage. The default setting is 4.35 V.

See *FLOAT* (REG 11h[7:0])

Charge Termination Threshold (I_{TERM})

Terminates charging at the desired current when TE (termination enable)=“1”. The default setting is 300 mA.

See *ITERM* (REG 13h[7:4])

CONFIGURABLE INPUT POWER PARAMETERS

The following input power parameters can be programmed by the host through I^2C:

VBUS Input Current Limit (I_{BUSLIM})

Limits the amount of current drawn from the VBUS source. The default setting is 500 mA.

See *IBUSLIM* (REG 14h[6:0])

VIN Input Current Limit (I_{INLIM})

Limits the amount of current drawn from the VIN source. The default setting is 1 A.

See *IINLIM* (REG 16h[6:0])

Dynamic Input Voltage Control (V_{SOURCE})

Limits the input current when a current−limited weak adapter is connected to either of VBUS or VIN. The settings are configurable from 4.2 V to 8.6 V. The default settings are 4.56 V.

See *VBUSLIM* (REG 15h[3:0]) and *VINLIM* (REG 17h[3:0])

CONFIGURABLE BOOST PARAMETERS

The following boost parameters can be programmed by the host through I^2C:

Boost Output Voltage (V_{BOOST})

Regulates the boost converter output voltage on PMID when BOOSTEN = “1”. When OTG = “1” VBUS is connected to PMID. The default setting is 5.0 V.

See *VBOOST* (REG 1Ch[3:0]).

CHARGE MODE TYPICAL CHARACTERISTICS

Unless otherwise specified, circuit of Typical Application, using FAN54511A, default register values/settings, V_{BUS} = 5.0 V, and T_A = 25°C.

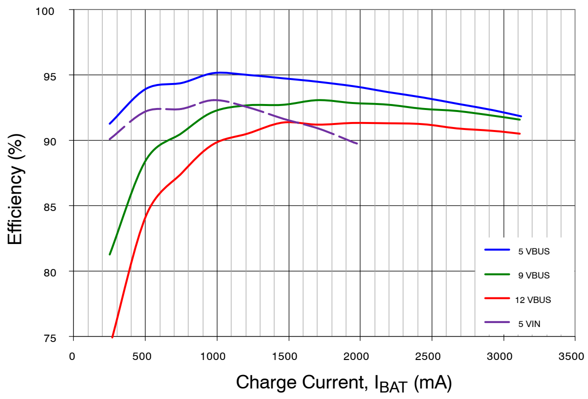


Figure 9. Efficiency vs. IOCHRG, V_{BAT} = 4.3 V, I_{BUSLIM} = 3.0 A, I_{INLIM} = 2.0 A

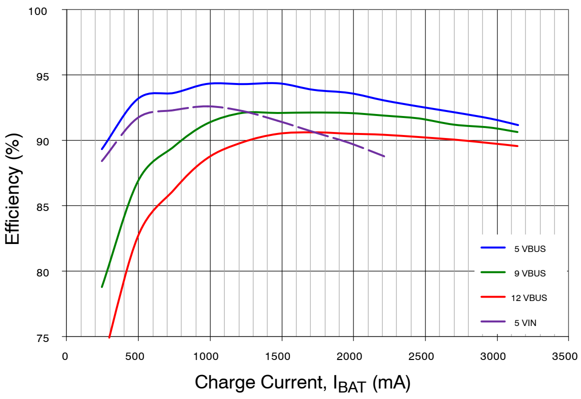


Figure 10. Efficiency vs. IOCHRG, V_{BAT} = 3.8 V, I_{BUSLIM} = 3.0 A, I_{INLIM} = 2.0 A

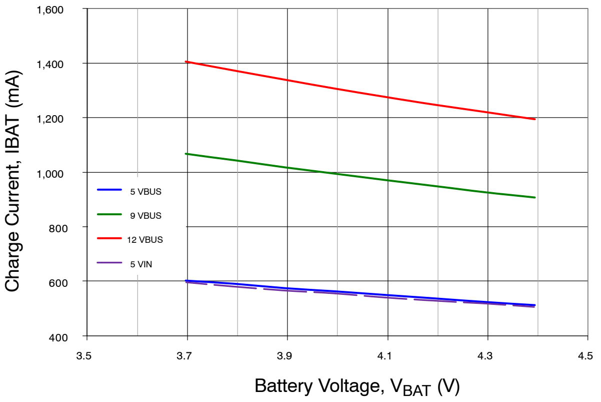


Figure 11. Fast Charge Current vs. $V_{BAT,}$ I_{OCHRG} = 3.2 A, I_{BUSLIM} = I_{INLIM} = 500 mA, V_{FLOAT} = 4.5 V

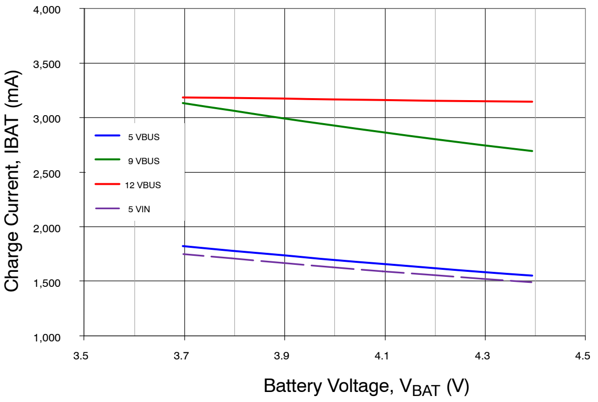


Figure 12. Fast Charge Current vs. $V_{BAT,}$ I_{OCHRG} = 3.2 A, I_{BUSLIM} = I_{INLIM} = 1,500 mA, V_{FLOAT} = 4.5 V

CHARGE MODE TYPICAL CHARACTERISTICS

(Unless otherwise specified, circuit of *Typical Application*, using FAN54511A, default register values/settings, V_{BUS} = 5.0 V, T_A = 25°C

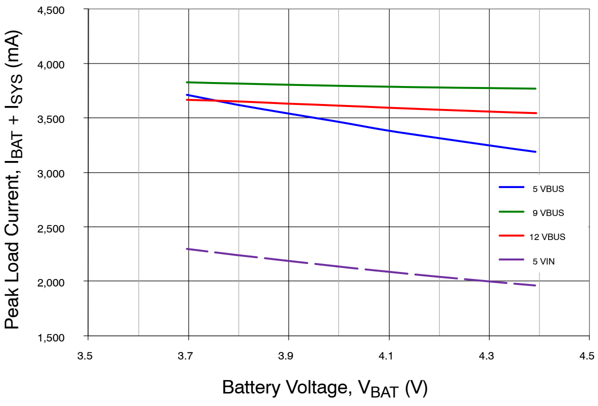


Figure 13. Peak Available Load Current (I_{BAT} + I_{SYS}) vs. V_{BAT}, I_{BUSLIM} = 3.0 A, I_{INLIM} = 2.0 A, V_{FLOAT} = 4.5 V

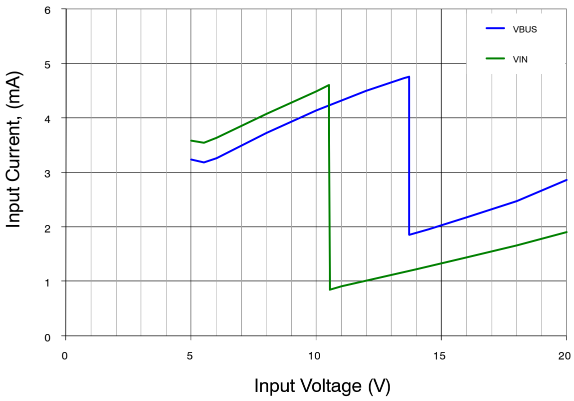


Figure 14. Quiescent Current vs. Input Voltage, I_{SYS} = 0 A, No Battery, LDO Off, NTC = GND, V_{BUSOVP} = 13.7 V, V_{INOVP} = 10.5 V

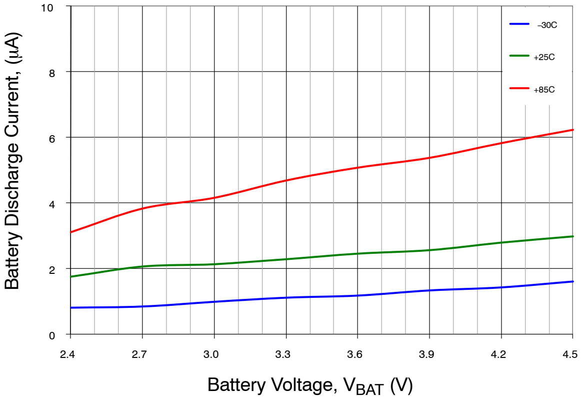


Figure 15. Battery Discharge Current vs. V_{BAT}, Sleep Mode

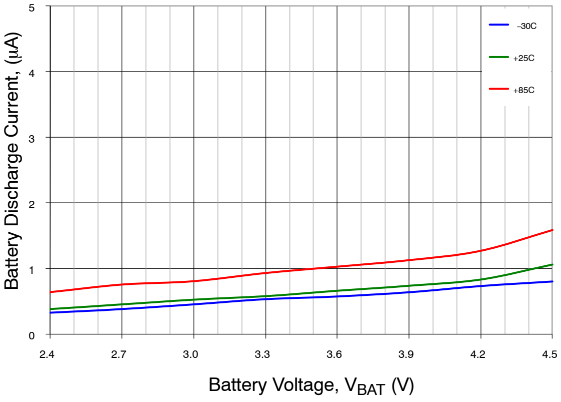


Figure 16. Battery Discharge Current vs. V_{BAT}, Ship Mode

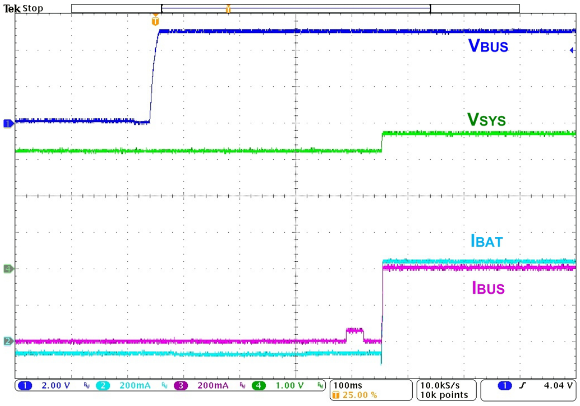


Figure 17. Startup at V_{BUS} Plug−In, V_{BAT} = 3.2 V, 50 Ω SYS Load, ILIM = “0”

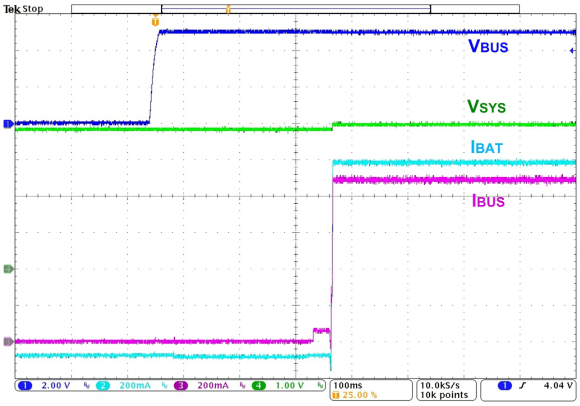


Figure 18. Startup at V_{BUS} Plug−In, V_{BAT} = 3.8 V, 50 Ω SYS Load, ILIM = “0”

CHARGE MODE TYPICAL CHARACTERISTICS (continued)

(Unless otherwise specified, circuit of Typical Application, using FAN54511A, default register values/settings, V_{BUS} = 5.0 V, and T_A = 25°C)

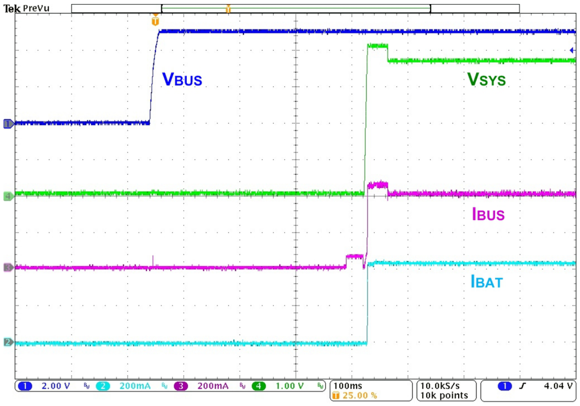


Figure 19. Startup at V_{BUS} Plug−In, Dead Battery, 50 Ω SYS Load, ILIM = “0”

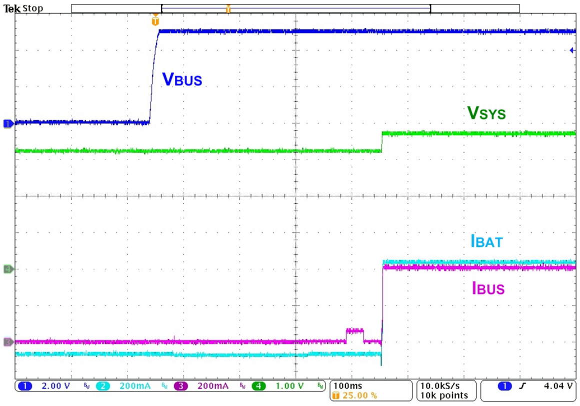


Figure 20. FAN54510 Startup at V_{BUS} Plug−In, V_{BAT} = 3.2 V, 50 Ω SYS Load, SDP, No Host Control

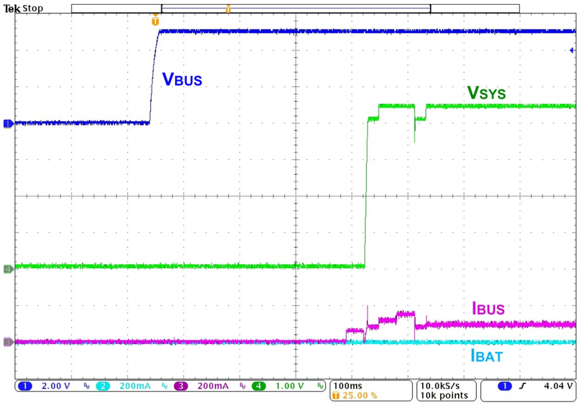


Figure 21. Startup at V_{BUS} Plug−In, No Battery, 50 Ω SYS Load, ILIM = “0”

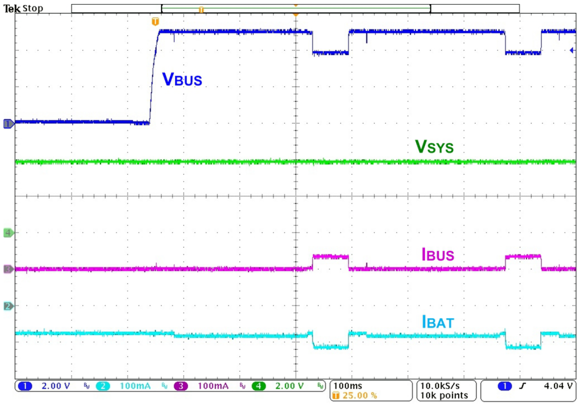


Figure 22. V_{BUS} Plug−In with V_{SOURCE} Validation Fail, V_{BAT} = 3.8 V, 50 Ω SYS Load

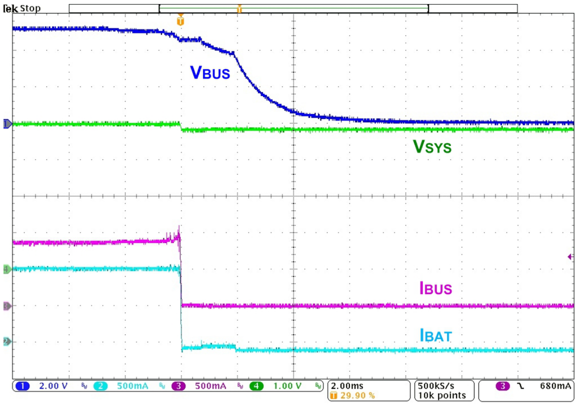


Figure 23. V_{BUS} Un−Plug, 3.8 V_{BAT}, 50 Ω SYS Load, ILIM = “0”

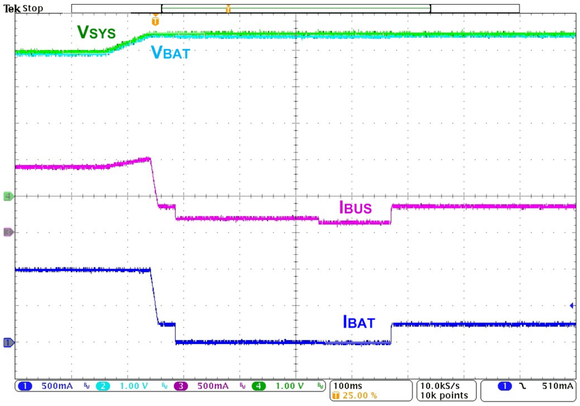


Figure 24. Charge Termination, TE = TOEN = “1”, I_{TERM} = 300 mA, 100 mA SYS Load

CHARGE MODE TYPICAL CHARACTERISTICS (continued)

(Unless otherwise specified, circuit of Typical Application, using FAN54511A, default register values/settings, V_{BUS} = 5.0 V, and T_A = 25°C)

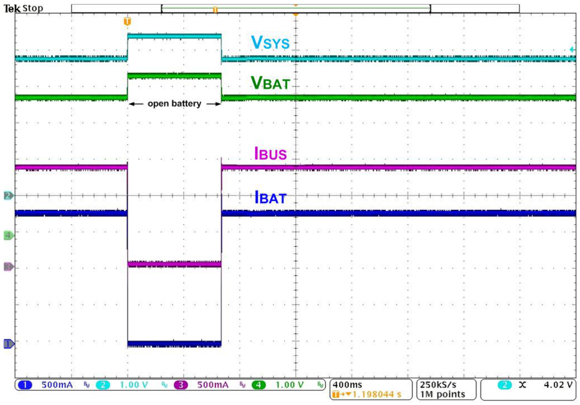


Figure 25. Battery Removal/Insertion while Charging, TE = “0”, V_{BAT} = 3.8 V, 50 mA SYS Load, I_{BUSLIM} = 1.5 A, I_{OCHRG} = 2.0 A

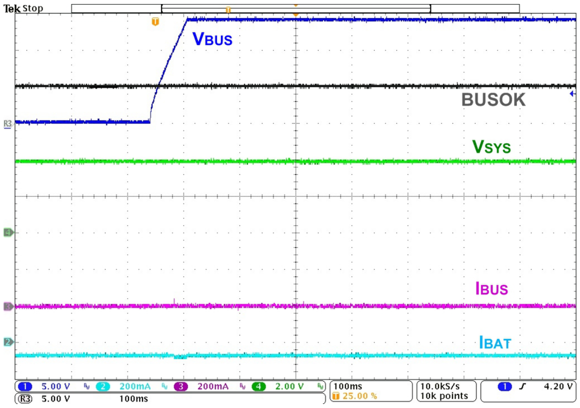


Figure 26. V_{BUS} Plug−In OVP Condition, V_{BAT} = 3.8 V, 50 Ω SYS Load, ILIM = “0”

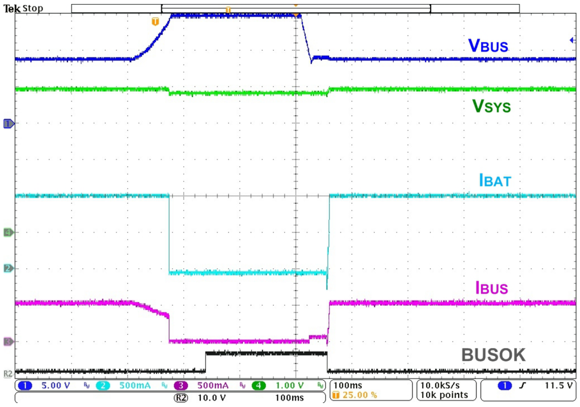


Figure 27. V_{BUS} OVP Response While Charging, V_{BAT} = 3.8 V, 50 Ω SYS Load, ILIM = “0”

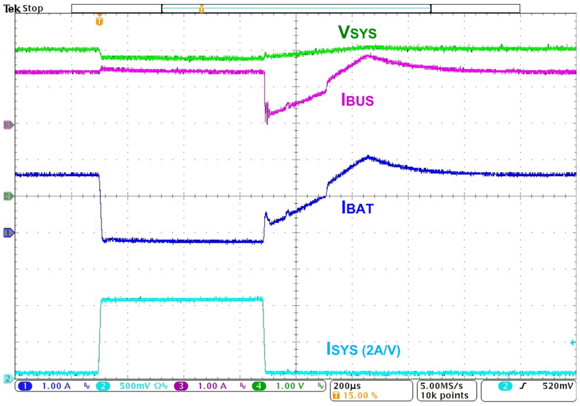


Figure 28. Load Pulse Response, 150 mA–2150 mA– 150 mA SYS Load with $t_R = t_F$ = 10 μsec, 3.8 V_{BAT}, I_{BUSLIM} = 1.5 A, I_{OCHRG} = 3.0 A

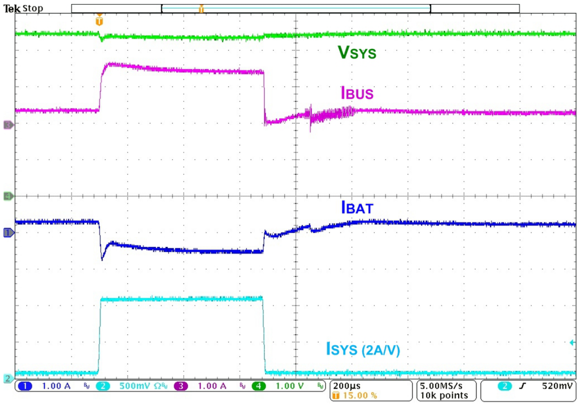


Figure 29. Load Pulse Response, 150 mA–2150 mA– 150 mA SYS Load with $t_R = t_F$ = 10 μsec, 4.35 V_{BAT}, I_{BUSLIM} = 1.5 A, I_{ORCHG} = 3.0 A, TE = “0”

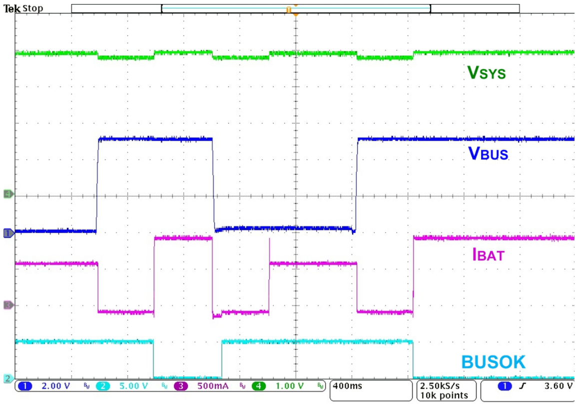


Figure 30. Input Source Selection, 5.0 V_{IN} Present, Insert/Remove 5.0 V_{BUS}, 3.8 V_{BAT}, 50 Ω SYS Load

CHARGE MODE TYPICAL CHARACTERISTICS (continued)

(Unless otherwise specified, circuit of Typical Application, using FAN54511A, default register values/settings, V_{BUS} = 5.0 V, and T_A = 25°C)

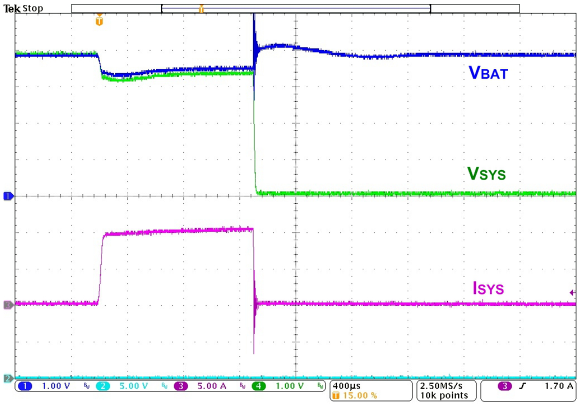


Figure 31. Battery Discharge Current Limit Response to SYS Fault, Sleep Mode, 3.8 V_{BAT}

CHARGE MODE TYPICAL CHARACTERISTICS

(Unless otherwise specified, using circuit of Typical Application, V_{BAT} = 3.8 V, V_{BOOST} = 5.00 V, T_A = 25°C. Boost enabled by writing BOOSTEN = OTG = “1”, simultaneously.)

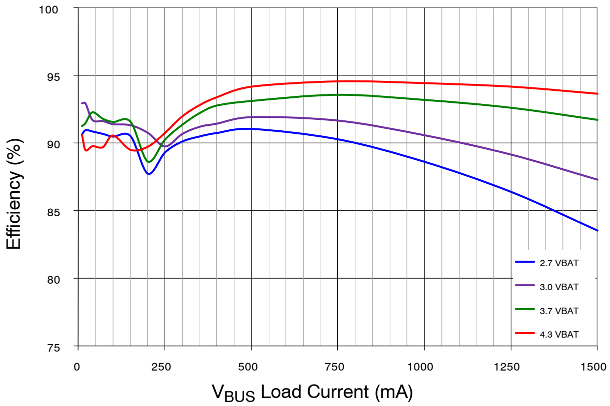


Figure 32. Efficiency vs. Load Current

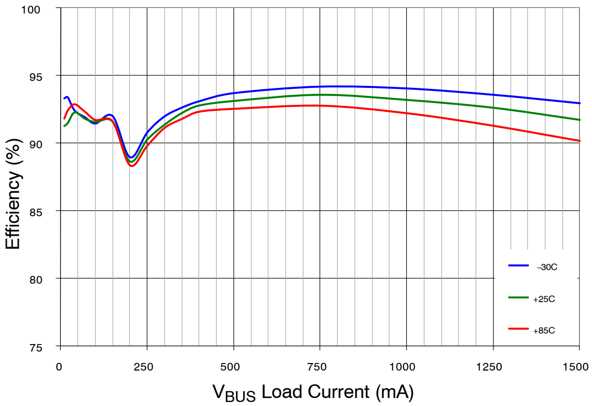


Figure 33. Efficiency vs. Load Current, 3.7 V_{BAT}

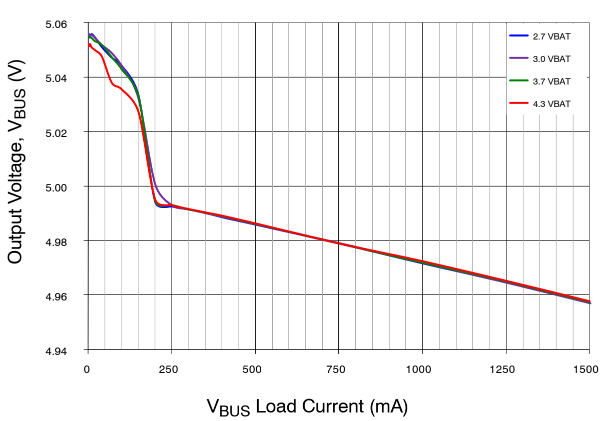


Figure 34. Output Regulation

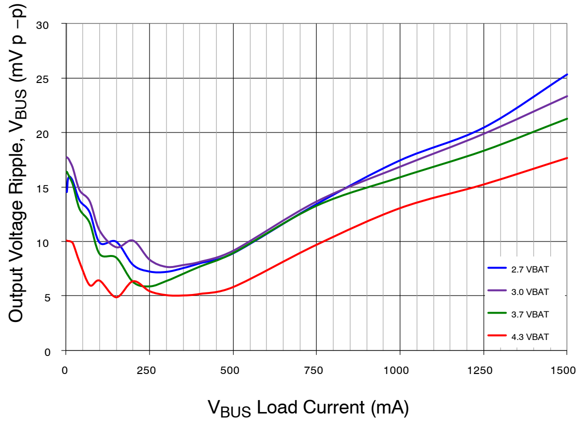


Figure 35. Output Ripple vs. Load Current

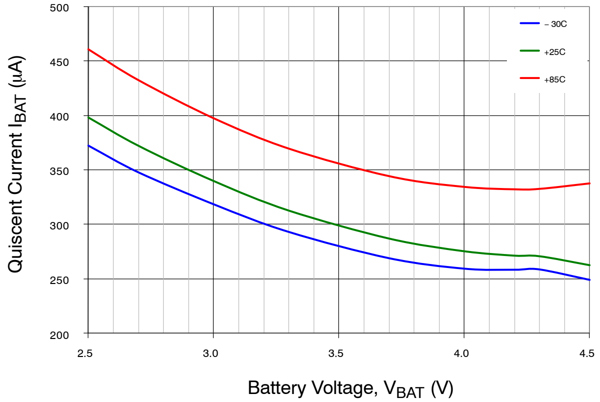


Figure 36. Quiescent Current

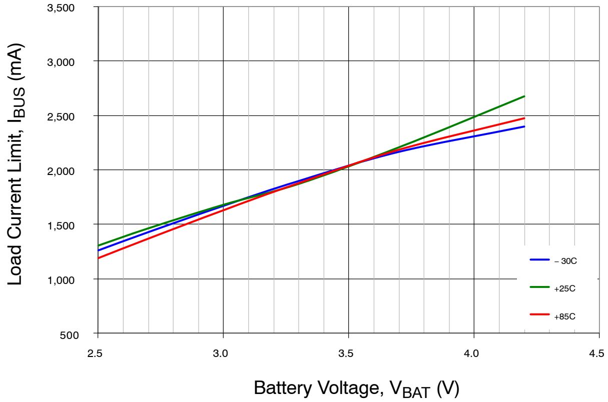


Figure 37. Load Current Limit, 5.00 V_{BOOST}

CHARGE MODE TYPICAL CHARACTERISTICS

(Unless otherwise specified, using circuit of Typical Application, V_{BAT} = 3.8 V, V_{BOOST} = 5.00 V, T_A = 25°C. Boost enabled by writing BOOSTEN = OTG = “1”, simultaneously.)

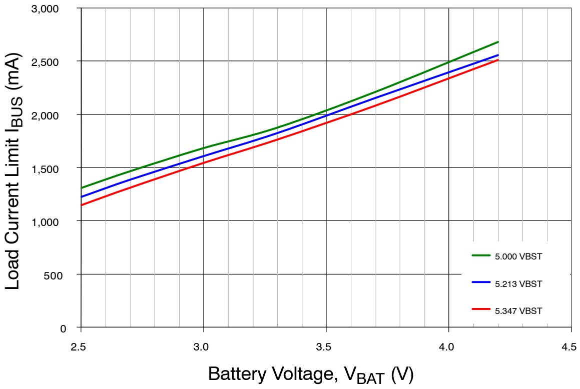


Figure 38. Load Current Limit vs. V_{BOOST}

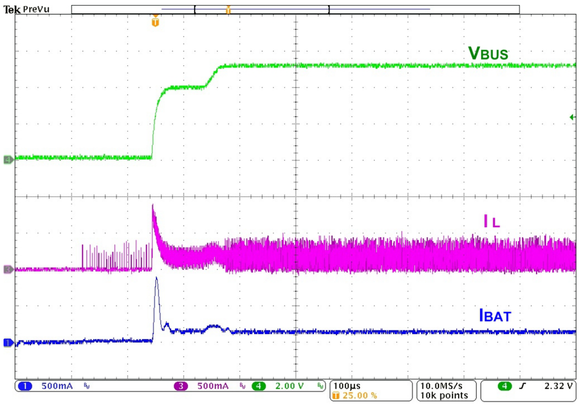


Figure 39. Boost Startup, 50 Ω Load

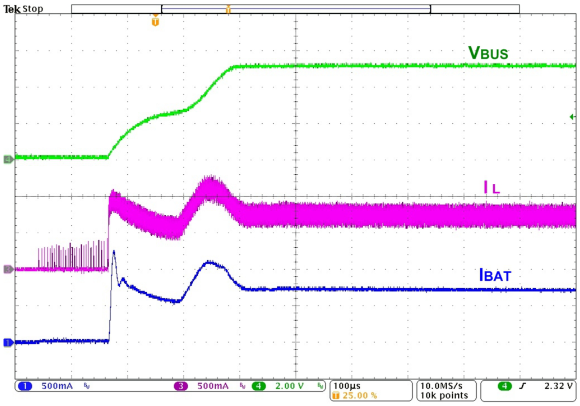


Figure 40. Boost Startup, 5 Ω || 10 µF Load

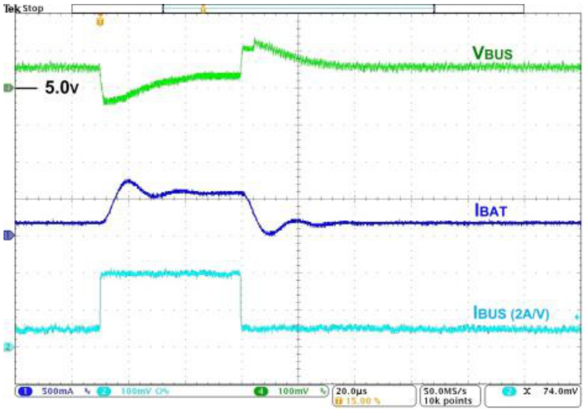


Figure 41. Load Transient Response, 100 mA–400 mA–100 mA Load with t_R = t_F = 100 nsec

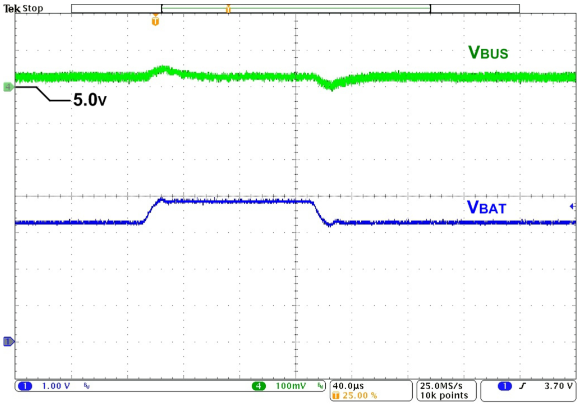


Figure 42. Line Transient Response, 500mA Load, 3.8 V_{BAT} –3.2 V_{BAT} –3.8 V_{BAT} with t_R = t_F = 10 µsec

CHARGE MODE TYPICAL CHARACTERISTICS

(Unless otherwise specified, using circuit of Typical Application, V_{BAT} = 3.8 V, V_{BOOST} = 5.00 V, T_A = 25°C. Boost enabled by writing BOOSTEN = OTG = "1", simultaneously.)

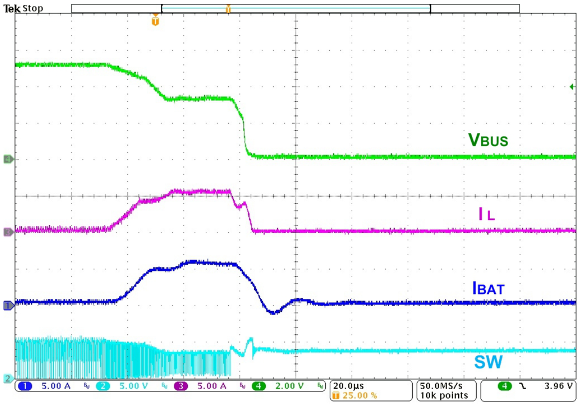


Figure 43. V_{BUS} Output Fault Response

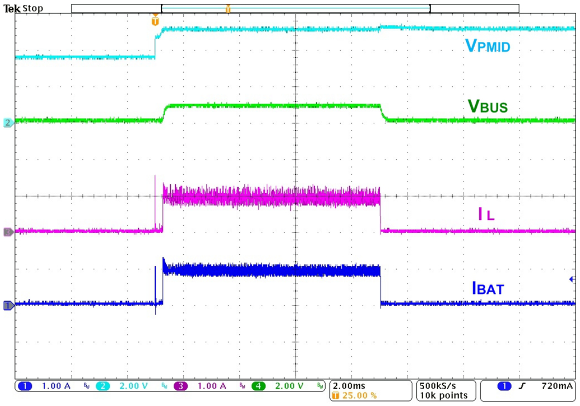


Figure 44. Boost Startup into V_{BUS} Fault

NON–CHARGING STATES

Idle State

During Idle State the PWM Buck continues to regulate system voltage to V_{FLOAT} providing power to the system. The battery is not being charged and the BATFET (Q4) is off.

In the Idle State, the V_{BAT}/V_{SYS} comparator is monitored and if V_{SYS} falls below V_{BAT} by V_{THSYS}, the BATFET (Q4) is fully enhanced for Supplemental Mode operation.

If Idle State is entered for any of the following conditions, a return to Charge State occurs when the related condition is removed:

1. Charge Complete (CHGCMP = "1") occurs with TE = "1". If RCHGDIS (REG 0Eh[5]) = "0", the IC will return to Charge State when $V_{BAT} < V_{FLOAT} - V_{RCHG}$.
2. The Top−Off Timer (t_{TO}) expires. If RCHGDIS (REG 0Eh[5]) = "0", the IC will return to Charge State when $V_{BAT} < V_{FLOAT} - V_{RCHG}$.
3. The battery is below T1 or above T4. See JEITA Charging section for details.
4. The battery is removed and TE = "1".
5. The BATFET is disabled by the Charge Enable bit, CE# = "1".

If Idle State is entered for any of the following conditions, the only way to restart charging is to first remove V_{SOURCE}, and then reconnect a valid VIN or VBUS power source:

1. The Safety Timer (t_{PRE} or t_{FAST}) expires when CONT (REG 0Eh[7]) = "0".
2. The battery voltage drops below V_{SHORT} during charging.
3. The Watch Dog Timer (t_{WD}) expires and WDTEXP (REG 30h[7]) = "1".

Standby State

The Standby State is an intermediate state where the PWM Buck is off and the BATFET (Q4) is fully enhanced. During Standby State, reverse current out of the VBUS or VIN pin is prevented by turning off the Q3 and Q5 blocking FETs.

If Standby State is entered for any of the following conditions, a return to Charge State occurs when the related condition is removed:

1. Sleep State where $V_{SOURCE} < V_{BAT} + V_{SLP}$ or $V_{SOURCE} < V_{SOURCE(FALL)}$.
2. The device has been put in Hi−Z state by HZMODE (REG 0Eh[1]) = "1" or DIS = HIGH.
3. The die temperature is in thermal shutdown ($T_{SHUTDOWN}$).

If Standby State is entered for any of the following conditions, the only way to restart charging is to first remove V_{SOURCE}, and then reconnect a valid VIN or VBUS power source:

1. The USB Timer (t_{USB}) expires (FAN54510A and FAN54512A only).

Sleep State

Sleep State is part of the suite of conditions which make up the Standby State. The BATFET (Q4) is fully enhanced while the IC is in the Sleep State. This ensures that the FAN5451x powers the system from the battery when operating without a valid input source on either VBUS or VIN.

APPLICABLE STATUS AND INTERRUPT

Status Bits: SLEEP (REG 00h[1])

CHARGER CIRCUIT DETAILS

Refer to:

Charger State Diagram" State and Mode Transitions

and

Charger State Diagram: Charger/Battery/System Protection

Plug In: Source Selection and Validation

Source Selection

Only one input source (VBUS or VIN) can be routed to the buck converter at any given time. If valid power sources are connected to both VIN and VBUS, the input selector automatically opens Q5 and closes Q3, thereby selecting VBUS as the input source to the buck converter.

The active source is identified by a Status bit.

APPLICABLE STATUS AND INTERRUPT

Status Bits:	INPUTSEL (REG 02h[7])

Battery Capacitor Discharge

When either V_{BUS} or V_{IN} rises and remains above $V_{SOURCE(RISE)}$ for the $t_{SRCQUAL}$ (32 mS) duration, the IC applies a I_{DETECT} (−8 mA) load to V_{BAT} for T_{DETECT} (262 ms) to ensure that if the battery is not present, or its discharge protection switch is open, the capacitors on V_{BAT} will be discharged below the V_{SHORT} threshold.

D+/D− Adapter Detection (VBUS only)

See Table 11 and Table 12 for the FAN5451x versions that have this feature.

When V_{BUS} rises and remains above $V_{SOURCE(RISE)}$ for the $t_{SRCQUAL}$ (32 mS) duration, the FAN5451x versions that have this feature perform adapter detection.

SDP, CDP, and DCP adapter types can be uniquely identified by the Charger IC, which will automatically select the appropriate I_{BUS} current limit per the USB Battery Charging Specification (BC1.2), and report the adapter type in a Status register.

APPLICABLE STATUS AND INTERRUPT

Status Bits:	CHGDET (REG 01h[6:5])

Source Voltage Validation

After battery capacitor discharge, Source Voltage Validation occurs with a $I_{VSOURCE}$ (50 mA) load on PMID. To pass validation, either V_{BUS} or V_{IN} must remain above $V_{SOURCE(RISE)}$ and below $V_{SOURCEOVP}$ for t_{VSR_VALID} (32 ms) before the IC initiates charging. T_{VSR_VALID} ensures that unfiltered 50/60 Hz chargers and other non−compliant chargers are rejected.

APPLICABLE STATUS AND INTERRUPT

Pins:	/BUSOK /INOK /INT
Interrupt Bits:	VBUSINT (REG 04h[5]) VININT (REG 04h[6])
Status Bits:	VBUSPWR (REG 00h[5]) VINPWR (REG 00h[6]) INPUTSEL (REG 02h[7])

If the input source fails validation, the validation period is extended an additional 32 ms and source validation is re−tried. A failure will result in an interrupt and the part returning to Sleep State, where the entire validation routine will restart when $V_{SOURCE} > V_{SOURCE(RISE)}$.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	VALFAIL (REG 04h[7])

Battery Voltage Measurement

The battery voltage is measured if the adapter passes Source Validation. The IC can identify an absent, shorted, low, or dead battery, configure the charging parameters accordingly, and then enter Charge Mode.

Figure 45, Figure 46, and Figure 47 illustrate Plug In timing under various conditions. The t_{DELAY} timing specification is affected by V_{BAT} and is described in Table 10.

Table 10. T_{DELAY} TIMING vs. V_{BAT}

V_{BAT} (V)	T_{DELAY} (ms)
$< V_{BATMIN}$	69
$V_{BATMIN} < V_{BAT} < V_{LOWV}$	37
$> V_{LOWV}$	10

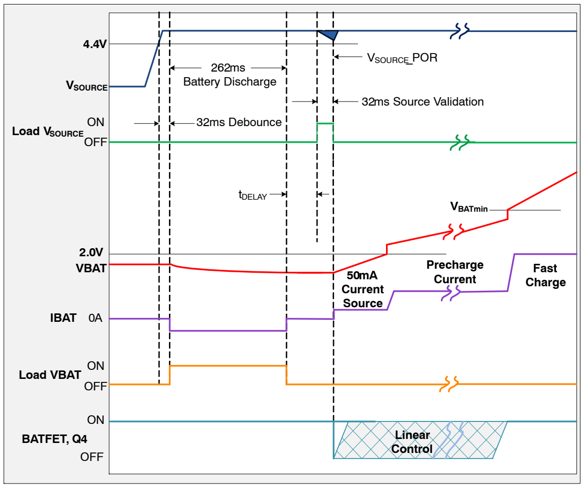


Figure 45. VBUS or VIN Plug In, $V_{BAT} < V_{SHORT}$

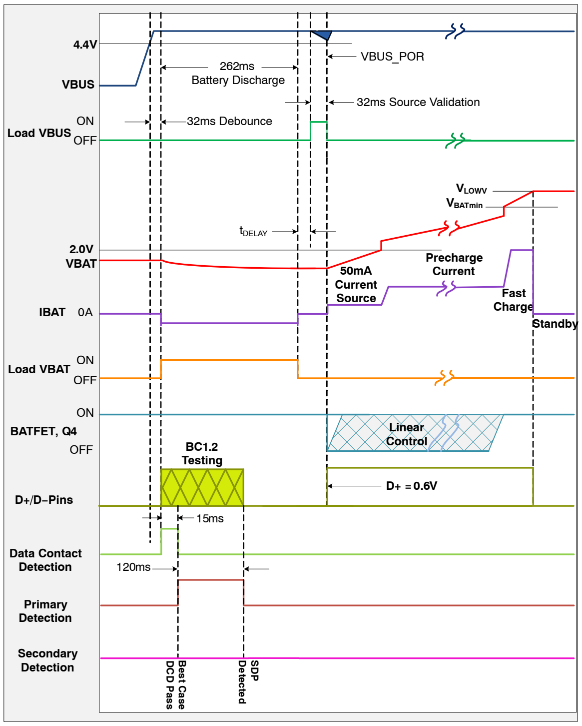


Figure 46. VBUS Plug In, SDP, $V_{BAT} < V_{SHORT}$

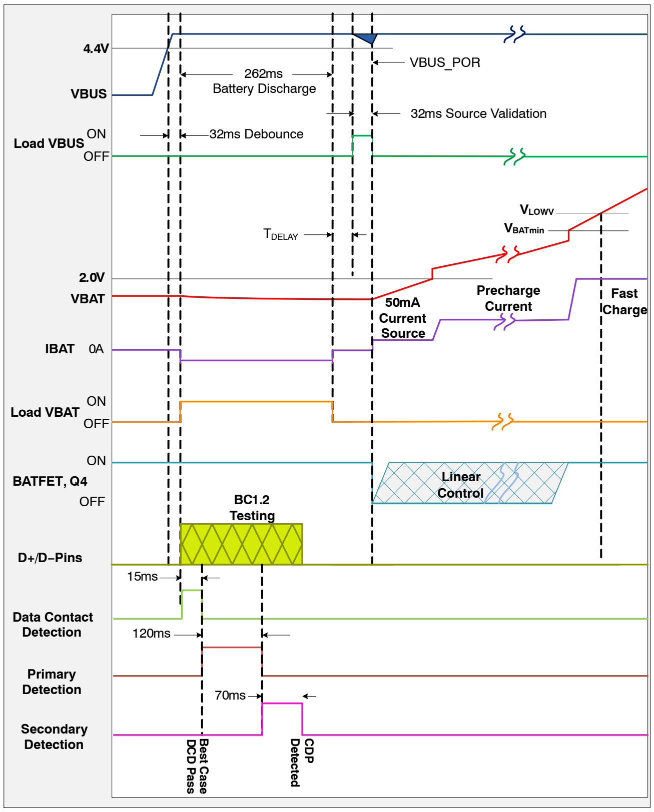


Figure 47. VBUS Plug In, CDP, $V_{BAT} < V_{SHORT}$

CHARGE MODES

Auto−Charge and Establishing Host Control

The FAN5451x features Auto−Charge, which supports battery charging prior to Host Control.

After the source voltage has been validated at Plug In, if $V_{BAT} < V_{BATMIN}$, the IC resets all registers to their default values. Regardless of battery voltage, the IC then operates in accordance with its I^2C register settings except that the IBUSLIM (REG 14h[6:0]) settings are ignored until the first I^2C write after charging begins.

Only after the first I^2C write after charging begins is Host Control established.

Prior to Host Control, the I_{BUS} current limit and the charge timer length are as described in Table 11 and Table 12.

Once Host Control has been established, the charge parameter settings are as described in Table 13.

For FAN5451x versions where the BC1.2 adapter detection circuit is enabled, the I_{BUS} current limit prior to establishing Host Control is determined by D+/D− Adapter Detection at Plug In. If the adapter type cannot be identified as either CDP or DCP, the charger will be configured to SDP Auto−Charge.

SDP Auto−Charge uses a dedicated SDP timer (t_{USB}) with the I_{BUS} current limit configured as per Table 11. If the t_{USB} timer is allowed to expire, the charger enters Standby State, where the only way to restart charging is to first remove V_{SOURCE}, then reconnect a valid VIN or VBUS power source.

If a SDP adapter is detected and $V_{BAT} > V_{LOWV}$, the charger will disable the LDO and enter Standby State, where any I^2C write to the IC will return it to Charge Mode under Host Control.

If a SDP adapter is detected and the DIS pin is HIGH, the LDO will be disabled after validation and remain disabled until SDP charging occurs when DIS is driven LOW or Host Control is established.

If a CDP or DCP adapter is detected, Auto−Charge uses the Safety Timer with the I_{BUS} current limit set to 1500 mA.

ILIM Pin Control Auto−Charge Mode

See Table 11 and Table 12 for the FAN5451x versions that have this feature.

For FAN5451x versions where the BC1.2 adapter detection circuit is disabled, the ILIM pin is used to set the I_{BUS} current limit prior to Host Control.

ILIM Pin Auto−Charge uses the Safety Timer with the I_{BUS} current limit configured as per Table 11.

Table 11. I_{BUS} CURRENT LIMIT (AUTO−CHARGE ONLY)

Part Number	Configuration	BC1.2 SDP	BC1.2 CDP/DCP	ILIM Pin Control (ILIM Pin = HIGH)	ILIM Pin Control (ILIM Pin = LOW)
FAN54510A	BC1.2 Detection	500 mA	1500 mA	N/A	N/A
FAN54511A	ILIM Pin Control	N/A	N/A	500 mA	1500 mA
FAN54511AP	ILIM Pin Control	N/A	N/A	500 mA	1500 mA
FAN54512A	BC1.2 Detection	100 mA	1500 mA	N/A	N/A
FAN54513A	ILIM Pin Control	N/A	N/A	100 mA	1500 mA

Table 12. CHARGE TIMER (AUTO−CHARGE ONLY)

Part Number	Configuration	BC1.2 SDP	BC1.2 CDP/DCP	ILIM Pin Control
FAN54510A	BC1.2 Detection	t_{USB} = 2 min.	Safety Timer	N/A
FAN54511A	ILIM Pin Control	N/A	N/A	Safety Timer
FAN54511AP	ILIM Pin Control	N/A	N/A	Safety Timer
FAN54512A	BC1.2 Detection	t_{USB} = 45 min.	Safety Timer	N/A
FAN54513A	ILIM Pin Control	N/A	N/A	Safety Timer

Table 13. CHARGE PARAMETER SETTING VS. OPERATING MODE (HOST CONTROL ONLY)

Operating Mode	V_{SOURCE}	V_{BAT}	Charger Bit Settings					
			IINLIM	IBUSLIM	PRECHG	IOCHRG	STAT	PWROK
Linear	Valid	$< V_{SHORT}$	1000 mA	500 mA	50 mA	X	1	0
Pre−Charge	Valid	$< V_{BATMIN}$	1000 mA	500 mA	450 mA	X	1	0
FAST Charge	Valid	$> V_{BATMIN}$	1000 mA	500 mA	X	1000 mA	1	0
FAST Charge	Valid	$> V_{LOWV}$	1000 mA	500 mA	X	1000 mA	1	1
Top−Off	Valid	$> V_{LOWV}$	1000 mA	500 mA	X	1000 mA	0	1
Recharge	Valid	$> V_{LOWV}$	1000 mA	500 mA	X	1000 mA	1	1

Linear Pre−Charge Mode

At the beginning of charging, if $V_{BAT} < V_{SHORT}$, the BATFET (Q4) operates as a linear current source with its current limited to 50 mA (I_{SHORT}) in order to safely recover a battery pack with an open protection switch. Additionally, the IC delivers power to SYS by regulating V_{SYS} to the default VSYS (REG 0Dh[1:0]) setting.

Pre−Charge (I_{PP}) Mode

At the beginning of charging, if $V_{SHORT} < V_{BAT} < V_{BATMIN}$, or if V_{BAT} has transitioned above V_{SHORT} from Linear Pre−Charge Mode, the IC enters Pre−Charge Mode while delivering power to SYS.

During Pre−Charge Mode, the BATFET (Q4) will operate as a linear current source with its current limited to the PRECHG (REG 13h[3:0]) setting. The IC will regulate V_{SYS} to the VSYS (REG 0Dh[1:0]) setting and attempt to charge the battery at less than or equal to the PRECHG setting without allowing V_{SYS} to drop below V_{BATMIN}.

All registers are programmable in Pre−Charge Mode.

APPLICABLE STATUS AND INTERRUPT

Pins:	/STAT /INT
Interrupt Bits:	WKBAT (REG 04h[1])
Status Bits:	PRE (REG 00h[2]) STAT (REG 00h[3])

Fats Charge (I_{OCHRG}) Mode

At the beginning of charging, if $V_{BAT} > V_{BATMIN}$, or if V_{BAT} has transitioned above V_{BATMIN} from Pre−Charge Mode, the IC enters Fast Charge.

During Fast Charge Mode, the BATFET (Q4) is fully enhanced and acts as a current sense element to limit charge current per the IOCHRG (REG 12h[5:0]) setting. Battery charging under constant current (CC) I_{OCHG} control continues until the battery voltage reaches V_{FLOAT}.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT /STAT
Interrupt Bits:	CHGMOD (REG 04h[2])

Good Battery Threshold (VLOWV)

The VLOWV (REG 0Ch[5:3]) bits define a battery voltage threshold between 3.0 V and 3.7 V where an interrupt is generated. The system designer can use this interrupt to indicate that full system power is available or for any other purpose. Charge parameters are not affected by VLOWV.

APPLICABLE STATUS AND INTERRUPTS

Pins:	/INT
Interrupt Bits:	VLOWVTH (REG 04h[4])
Status Bits:	PWROK (REG 00h[4])

Constant Voltage (CV) Mode

When V_{BAT} reaches V_{FLOAT}, as set by VFLOAT (REG 11h [7:0]), the charger enters the voltage regulation (CV Mode) phase of charging. The PWM regulator goes from regulating current across the BATFET (Q4) to regulating voltage on the BATSNS pin. This results in charge current declining.

The CV (REG 20h[0]) Monitor bit will be set to a “1” while the IC is in CV Mode.

Termination

Charge current termination is enabled when TE (REG 0Eh[3]) = “1”. When charge current falls below I_{TERM}, as set by ITERM (REG 13h[7:6]), for longer than the deglitch time of 30 ms, charging stops, Q4 turns off, an interrupt is issued, and the IC enters Idle State (Charge Complete) if TOEN (REG 0Eh[2]) = “0”. The buck converter will regulate SYS to VFLOAT (REG 11h[7:0]) and the battery will support Supplemental Mode if required.

Recharge occurs after Termination (TE = “1”), if RCHGDIS (REG 0Eh[5]) = “0”, when $V_{BAT} < V_{FLOAT} - V_{RCHG}$.

Charge termination is blocked unless the I_{TERM} threshold is crossed while in CV Mode. If another control loop (IBUSLIM, IOCHRG, DIVC) or Supplemental Mode operation exist, termination will be prevented until the CV condition is met.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT /STAT
Interrupt Bits:	CHGEND (REG 04h[3])
Status Bits:	CHGCMP (REG 01h[4])

If TE = “0”, when the charge current falls below I_{TERM}, charging continues, an interrupt is issued, but the CHGCMP bit is not set.

APPLICABLE STATUS, INTERRUPT AND MONITOR

Pins:	/INT
Interrupt Bits:	IBATLO (REG 05h[7])
Status Bits:	LOIBAT (REG 01h[7])
Monitor Bits:	ITERMCMP (REG 20h[7])

Top−Off Charging Mode

Top−Off Charging occurs after Termination (TE = “1”) if TOEN (REG 0Eh[2]) = “1”. The CHGEND interrupt will be issued and Top−Off Charging begins 400 ms later with the /STAT pin HIGH. During Top−Off Charging, the Battery Absence Detection is retried every 5s unless TO_BDETDIS (REG 1Bh[3]) is set to “1”.

The Top−Off Charging duration is set by the Top−Off Timer, TOTMR (REG 1Bh[2:0]). See Top−Off Timer for details.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT STAT
Interrupt Bits:	CHGEND (REG 04h[3]) TOCMP (REG 06h[7])
Status Bits:	STAT (REG 00h[3]) LOIBAT (REG 01h[7]) TOCHG (REG 01h[3])

System Current Prioritization

During Charge Mode, if the current available to charge is less than the programmed charge setting due to an input current limit setting, source limitations, or system load requirements, the current to the battery will be reduced to support the system load.

Supplemental Mode

During Charge Mode or Idle State, if the system load exceeds what the buck converter can provide, V_{SYS} will drop. If a falling V_{SYS} drops more than V_{THSYS} below V_{BAT}, the BATFET (Q4) will be fully enhanced to hold the system up to V_{BAT}.

Then, once a rising V_{SYS} becomes higher than V_{BAT} by V_{THSYS}, the BATFET (Q4) again serves as the current sense element to limit the charge current.

Table 14. SUMMARY OF BATFET (Q4) OPERATION VS. OPERATING MODE

PWM	Operating Mode	CE#	V_{SOURCE}	V_{BAT}	BATFET (Q4)
OFF	SLEEP	X	Both < (VSYS + VSLP)	X	ON
ON	Linear and Pre−Charge	0	Valid	> VSHORT & < VBATMIN	Linear
ON	FAST Charge	0	Valid	> VBATMIN & < VSYS	ON
OFF	HZMODE (REG 0Eh[1]) = ”1”	X	X	X	ON
ON	Supplemental	X	Valid	> VSYS	ON
ON	CE# = “1” (disable Q4 with Supplemental Mode remaining functional)	1	Valid	< VSYS	OFF
ON	PPOFF = ”1” (disable Q4 with Supplemental Mode disabled)	X	Valid	X	OFF

Source Plug Out

The IC continuously monitors V_{BUS} (or V_{IN}) during charging. If V_{SOURCE} falls below the higher of $V_{SOURCE(FALL)}$ or V_{BAT}+V_{SLP}, the IC terminates charging and enters Sleep State (Standby).

APPLICABLE STATUS AND INTERRUPT

Pins:	/BUSOK /INOK /INT /STAT
Interrupt Bits:	VLOWTH (REG 04h[4]) VBUSINT (REG 04h[5]) VININT (REG 04h[6])
Status Bits:	SLEEP (REG 00h[1]) VBUSPWR (REG 00h[5]) VINPWR (REG 00h[6]) INPUTSEL (REG 02h[7])

CHARGING STATUS AND INTERRUPT REPORTING

Charging Status

The /STAT pin is used to report the charge status to the host processor. During charge, the /STAT pin is LOW. After Termination, the /STAT pin goes HIGH and will remain HIGH even during Top−Off Charging Mode.

The STAT (REG 00h[3]) bit indicates a “1” when charging except during Top−Off.

APPLICABLE STATUS AND INTERRUPT

Pins:	/STAT
Status Bits:	STAT (REG 00h[3])

Interrupts

The /INT pin is used to indicate that one or more unmasked interrupt bits have been set.

The pin will remain LOW until all set interrupt bits (Registers 04h to 06h) are read and cleared. In the event that another interrupt occurs while the register containing the bit is read, the interrupt will be stored in a buffer and transferred to the register after the read. Thus, the /INT pin may remain LOW until the register is read and cleared again.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	INT 0 (REG 04h) INT 1 (REG 05h) INT 2 (REG 06h)

Interrupt Masking

Masking an interrupt bit using its corresponding mask bit, found in registers 08h to 0Ah, prevents a masked interrupt event from setting the /INT pin to LOW. The associated interrupt bit will be set to “1”.

CHARGER/BATTERY/SYSTEM PROTECTIONS

Dynamic Input Voltage Control

The IC includes a Dynamic Input Voltage Control (DIVC) loop which automatically limits input current in case a current−limited source is supplying V_{BUS} or V_{IN}. The control loop increases the charging current until either:

I_{BUSLIM} / I_{INLIM} or I_{OCHRG}

is reached or

$V_{BUS} = V_{BUSLIM}$ or $V_{IN} = V_{INLIM}$

If an increase in load occurs on VSYS during charging that causes VBUS or VIN to reduce below VBUSLIM or VINLIM, the charge current is reduced until VBUS or VIN rise to the VBUSLIM or VINLIM threshold. At V_{SOURCE} plug in, the VBUSLIM (REG 15h[3:0]) and VINLIM (REG 17h[3:0]) bits are always set to their default values.

High−Impedance Mode and Disable

Setting the HZMODE (REG 0Eh[1]) bit to “1” or setting the DIS pin to HIGH disables the charger and puts the IC into High−Impedance Mode (HZ). The Safety Timer and Watch Dog Timer are reset.

If V_{BAT} falls below V_{BATMIN}, with HZMODE set to “1”, the HZMODE bit will automatically reset to “0”, and charging will commence. Setting HZMODE = “1” when $V_{BAT} < V_{BATMIN}$ is ignored. The DIS pin is functional when $V_{BAT} < V_{BATMIN}$.

Safety Timer

At the beginning of charging, the IC starts the Safety Timer. The Safety Timer consists of two segments, Pre−Charge (PRETMR) and Fast Charge (FCTMR). The Safety Timer can be programmed using the bits in the TIMER (REG 19h) register.

The Pre−Charge timer begins at the start of charging of a battery whose voltage is less than V_{BATMIN}. Once the battery voltage has risen above V_{BATMIN}, the Pre−Charge Timer is cleared and the Fast Charge Timer begins. If the battery voltage were to fall below V_{BATMIN} during Fast Charge, the Fast Charge Timer will continue to run until the battery is fully charged or the timer expires.

Charging with the Safety Timer running is used for charging that is unattended by the host. If the Safety Timer expires charging ceases, all registers reset to their default values, the device enters Idle State, and an interrupt is issued.

If the CONT (REG 0Eh[7]) = “1”, charging will continue if the Safety Timer is allowed to expire.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT /STAT
Interrupt Bits:	TIMER (REG 06h[0])
Status Bits:	TMRTO Status bit (REG 02h[0])

Watch Dog Timer (WDT)

Setting WDEN (REG 19h[6]) to "1" enables the WDT and disables, but does not clear the Safety Timer.

Setting TMRRST (REG19h[7]) to "1" resets the WDT. This bit should be written at a rate more frequent than t_{WD}.

If the WDT expires, charging continues on the remainder of the time left on the Safety Timer. Additionally, all registers except SAFETY (REG 1Ah[7:0]), are reset to their default values, and an interrupt is issued. If WDTEXP (REG 30h[7]) = "1" and the WDT expires, the device will instead immediately enter Idle State.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT /STAT
Interrupt Bits:	TIMER (REG 06h[0])
Status Bits:	WDTTO (REG 02h[1])

Top−Off Timer

The Top−Off timer duration is programmable using the TOTMR (REG 1Bh [2:0]) bits. When the timer expires charging stops, the BATFET (Q4) is disabled, an interrupt is issued, and the device enters Idle State. If RCHGDIS (REG 0Eh[5]) = "0", the IC will return to Charge State when $V_{BAT} < V_{FLOAT} − V_{RCHG}$.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	TOCMP (REG 06h[7])
Status Bits:	CHGCMP (REG 01h[4])

Table 15. SUMMARY OF TIMERS

Name	Control Register	Range (Minutes)	Default
Pre−Charge	19h[4:3]	100 sec to 36 min.	On, 36 min.
Fast Charge	19h[2:0]	4 hr to 16 hr	On, 8 hr
Watch Dog	19h[6]	100 sec	Off
Top – Off	1Bh[2:0]	10 min. to 70 min.	On, 30 min.

Thermal Regulation

When the IC's junction temperature reaches the programmable Thermal Regulation threshold, T_{REGTH}, set by TREGTH (REG (0Fh[6:5]), the thermal regulation loop reduces charge current to the lowest IOCHRG (REG 12h[5:0]) setting (200 mA) to prevent overheating.

The device will attempt to charge the battery at a maximum average current while maintaining the die temperature at or below T_{REGTH}. This is accomplished by stepping I_{OCHRG} from the lowest IOCHRG setting back up to the programmed IOCHRG setting. If T_{REGTH} is again reached the process is repeated.

During Thermal Regulation, the IBUSLIM and IINLIM input current limit settings are retained in order to support the system load from a valid power source.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	ICTEMP (REG (06h[4])
Status Bits:	TEMPFB (REG 02h[4])

Thermal Shutdown

If the junction temperature increases beyond the Thermal Shutdown threshold, $T_{SHUTDOWN}$, charging is suspended and the buck converter is disabled. While suspended, all timers stop and registers do not reset. Charging resumes only after the die temperature falls below T_{REGTH} where I_{OCHRG} will be stepped back up to the programmed IOCHRG setting.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT /STAT
Interrupt Bits:	ICTEMP (REG (06h[4])
Status Bits:	TEMPSD (REG (02h[5])

Register Reset Conditions

As an added layer of safety, the I^2C control bits automatically reset to their default values under certain situations. Refer to Table 16 for details.

Table 16. REGISTER RESET SUMMARY

Reset Condition Description	Registers that are Reset	Behavior After Reset Event
VBUS/VIN plug in (from no input connected) and any V_{BAT} voltage	VBUSLIM and VINLIM only	VBUSLIM = 4.56 V VINLIM = 4.56 V
VBUS/VIN plug in (from no input connected) and $V_{BAT} < V_{SHORT}$	All registers except STATUS, and IN TERRUPT	Pre−Charge with default settings; Q4 in Linear Region
VBUS/VIN plug in (from no input connected) and $V_{SHORT} < V_{BAT} < V_{BATMIN}$	All registers except SAFETY, STATUS, and INTERRUPT	Pre−Charge with default settings; Q4 in Linear Region
V_{BAT} falls below V_{BATMIN} with an input connected	HZMODE bit only	Pre−Charge at programmed settings; Q4 in Linear Region
Battery Removal Detected (input connected)	VFLOAT, IOCHRG, PRECHG, ITERM, SAFETY	Buck regulates at V_{FLOAT}; Q4 Off
Pre−Charge / Fast Charge Safety Timer Expiration	All registers except SAFETY, STATUS, and INTERRUPT	Buck regulates at 4.35 V; Charging stops; Q4 Off
Charge Mode Watchdog Timer Expiration (WDTEXP=”0”)		Charging continues with default settings; Q4 On
Charge Mode Watchdog Timer Expiration (WDTEXP= “1”)		Buck regulates at 4.35 V; Charging stops; Q4 Off
OTG Boost Mode Watchdog Timer Expiration		Boost Off; Q3 Off; Q4 On
Set RESET (REG 0Fh[7]) = “1” (Charge Mode)		Charging continues with default settings; Q4 On
Set RESET (REG 0Fh[7]) = “1” (OTG Boost Mode)		Boost Off; Q3 Off; Q4 On

JEITA Charging

The IC reduces I_{OCHRG} and V_{FLOAT} if the measured battery temperature is outside of the fast charging limits (Between T2 to T3) as described in the JEITA specification. There are four battery temperature thresholds that change battery charger operation: T1, T2, T3, and T4.

The IC first measures the NTC immediately prior to entering any PWM charging state, and then measures the NTC once per second, updating the result in the NTC4−NTC1 bits (REG 18h[3:0]).

The Host processor can disable JEITA charging reduction by setting the TEMPDIS (REG 18h[5]) bit to “1”.

To disable the thermistor circuit, tie the NTC pin to GND. This also disables the REF output. Before enabling the charger, the IC tests to see if NTC is shorted to GND. If NTC is shorted to GND, the NTCGND monitor bit (REG 21h[2]) will be set, no thermistor readings will take place, the NTCOK bit (REG 18h[4]) and NTC4−NTC1 (REG 18h[3:0]) bits will be reset.

APPLICABLE STATUS AND INTERRUPTS

Pins:	/INT
Interrupt Bits:	BATTEMP (REG 06h[3])
Status Bits:	JEITA (REG 02h[3]) TBAT (REG 02h[2])

Table 17. BATTERY TEMPERATURE THRESHOLDS, FOR USE WITH 10 K NTC, B = 3380, and R_{REF} = 10 K

Threshold	T_{BAT} (°C)	% of VREF
T1	0°C	73.9
T2	10°C	64.6
T3	45°C	32.9
T4	60°C	23.3

Table 18. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

T_{BAT} (°C)	I_{OCHRG}	V_{FLOAT}	NTC4−1	JEITA	TBAT	Notes
Below T1	Charging disabled (Q4 open)		0000	1	1	
Between T1 and T2	I_{OCHRG} / 2	V_{FLOAT} – 200 mV	0001	1	0	If IOCHRG is programmed to less than 400 mA, the charge current will be limited to 200 mA.
Between T2 and T3	I_{OCHRG}	V_{FLOAT}	0011	0	0	
Between T3 and T4	I_{OCHRG} / 2	V_{FLOAT} – 200 mV	0111	1	0	If IOCHRG is programmed to less than 400 mA, the charge current will be limited to 200 mA.
Above T4	Charging disabled (Q4 open)		1111	1	1	

Table 19. TEMPERATURE THRESHOLD WITH VARIOUS THERMISTORS, R_{REF} = R_{THRM} AT 25 °C

Parameter	Various Thermistors			
$R_{THRM(25°C)}$	10K	10K	47K	100K
β	3380	3940	4050	4250
T1	0°C	3°C	6°C	8°C
T2	10°C	12°C	13°C	14°C
T3	45°C	42°C	41°C	40°C
T4	60°C	55°C	53°C	51°C

V_{BUS} Over−Voltage Protection

When $V_{BUS} > V_{BUSOVP}$, the IC stops switching, fully enhances Q4 to support SYS load, and issues an interrupt.

When V_{BUS} falls below $V_{BUSOVP} - V_{BUSOVP(HYS)}$, charging resumes after VBUS is revalidated, where another interrupt is issued.

If $V_{BUS} > V_{BUSOVP}$, VIN cannot be used as a charging source.

APPLICABLE STATUS AND INTERRUPT

Pins:	/BUSOK /INT /STAT
Interrupt Bits:	VBUSINT (REG 04h[5]) OVPINPUT (REG 06h[6])
Status Bits:	INPUTOVP (REG 02h[6])

V_{IN} Over−Voltage Protection

When $V_{IN} > V_{INOVP}$, the IC stops switching, opens Q5, fully enhances Q4 to support SYS load, and issues an interrupt.

When V_{IN} falls below $V_{INOVP} - V_{INOVP(HYS)}$, charging resumes after VIN is revalidated, where another interrupt is issued.

If $V_{IN} > V_{INOVP}$, VBUS cannot be used as a charging source.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INOK /INT /STAT
Interrupt Bits:	VININT (REG 04h[6]) OVPINPUT (REG 06h[6])
Status Bits:	INPUTOVP (REG 02h[6])

V_{BAT} Over−Voltage Protection

The FLOAT voltage regulation loop prevents V_{BAT} from overshooting V_{FLOAT} by more than V_{BAT_OVP} if the battery is removed during Charge Mode with TE (REG 0Eh[3]) = “0” or “1”.

Additionally, if the battery is removed during Charge Mode and TE = “0”, the IC will remain in Charge Mode. Then if a battery is inserted that is charged to a voltage higher than 1.05 * V_{FLOAT};

1. PWM pulses stop while $V_{BAT} > V_{FLOAT}$.
2. HIVBAT (REG 20h[3]) monitor bit set to “1”.
3. BATFET (Q4) remains on to support the system, thus removing excess charge from the battery.

Battery Absence Detection while Charging

The IC can detect the presence, absence, or removal of a battery if TE (REG 0Eh[3]) = "1" and CE# = "0". During normal charging, once $V_{BAT} = V_{FLOAT}$ and the charge current falls below I_{TERM}, the PWM charger continues to provide power to SYS, the BATFET (Q4) is turned off except to support Supplemental Mode, and the IC enters Idle State. It then turns on a battery discharge current, I_{DETECT}, for t_{DETECT}. If V_{BAT} is still above $V_{FLOAT} – V_{RCHG}$, the battery is present and the NOBAT bit is maintained at "0". If V_{BAT} is below $V_{FLOAT} – V_{RCHG}$, the battery is absent and the IC resets all charging related registers to their default values (FLOAT, IOCHRG, PRECHG, and ITERM) and issues an interrupt.

By default the IC will retry Battery Absence Detection every t_{INT} (2.1 s) unless NOBATOP (REG 0Eh[4]) = "0".

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	BATINT (REG 04h[0])
Status Bits:	NOBAT (REG. 00h[0])

Battery Under−Voltage Protection

The battery voltage falling below V_{SHORT} during battery charging indicates that a catastrophic event has occurred on the BAT pin. If the battery voltage drops below V_{SHORT} during charging, the IC will automatically disable the BATFET (Q4) to stop current flow to the battery node, and issue an interrupt. The IC enters the Idle State where the buck converter continues to provide power to the system. If the battery voltage recovers above V_{SHORT}, Q4 remains off (Idle State is maintained) and BATSHORT is set to "1". This implementation is intended to lock out battery charging. The only way to restart charging is to first remove V_{SOURCE}, and then reconnect a valid VIN or VBUS power source.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT /STAT
Interrupt Bits:	SHORTBAT (REG 06h[5])
Status Bits:	LOIBAT (REG 01h[7])
Monitor Bits:	BATSHORT (REG 20h[4])

BATFET (Q4) Over−Current Protection

In order to prevent damage to the charger and battery due to a potentially dangerous fault on the SYS pin, the IC prevents its internal BATFET(Q4) from allowing excessive battery discharge current for more than T_{SCQUAL}. The Q4 short circuit current limit ($I_{LIMQ4SC}$) is set for 9 A (typical). If the battery is connected and the discharge current through Q4 exceeds $I_{LIMQ4SC}$ for more than the t_{SCQUAL} deglitch time (1 ms), Q4 will be disabled for the $t_{SCRECOV}$ recovery time of 2 seconds. Once the 2 seconds has passed, Q4 will turn on and check if the over−current condition still exists. If the over−current condition still exists, Q4 will be disabled again for 2 seconds. This cycle will repeat until the over−current condition is removed.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	BATOCP (REG 06h[1])

Safety Register

The IC contains a SAFETY (REG 1Ah) register that prevents the values in FLOAT (REG 11h[7:0]) and IOCHRG (REG 12h[5:0]) from being set to unsafe levels. The VSAFE (REG 1Ah[7:4]) and ISAFE (REG 1Ah[3:0]) register bits within the SAFETY register set a maximum programmable value for FLOAT and IOCHRG.

After V_{BAT} rises above V_{SHORT}, the SAFETY register is loaded with its default value and may be changed on the first write to the SAFETY register and only before writing to any other register. The VSAFE and ISAFE values must be written to the register at the same time. After first writing to the SAFETY register or any other register, the SAFETY register is locked.

The SAFETY register will reset to default values when $V_{BAT} < V_{SHORT}$. The SAFETY register does not reset if the Safety Timer or WDT timer expires.

Ship Mode

Ship Mode is a state where the BATFET (Q4) is configured to isolate the battery from the system load to minimize battery discharge current to the system. This mode of operation is useful for preserving the battery life of a mobile device during extended shipping and storage durations. Ship Mode is also useful for production testing of a mobile device without having to drain the battery.

The /SHIP pin controls entry into and exit out of Ship Mode. To enter Ship Mode, the /SHIP pin must be held LOW for $t_{SHIPENTER}$. To exit Ship Mode, /SHIP must be first released and then held LOW for $t_{SHIPEXIT}$. This configuration prevents accidental entry into and exit out of Ship Mode with a single key press of a mobile device's power button. An alternate method for exiting Ship Mode is to reapply a valid source to VBUS or VIN. Once the source has been validated, the charger IC will exit Ship Mode.

Ship Mode can also be programmed using the PPOFF (REG 0Fh[1]) and PPOFFSLP (REG 0Fh[2]) control bits. Setting PPOFF to "1" will disable Q4 and isolate the battery from the system load. As long as there is input power to maintain the charger's I^2C port, setting PPOFF back to "0" will re−enable Q4.

Setting PPOFFSLP to "1" while there is input power connected will disable Q4 once power is removed from VBUS and VIN. Once power is reapplied, the charger IC will automatically enable Q4.

The PPOFF and PPOFFSLP bits are automatically controlled by the /SHIP pin. When entering Ship Mode using the /SHIP pin, PPOFF and PPOFFSLP are set to "1". When exiting Ship Mode using the /SHIP pin, PPOFF and PPOFFSLP are reset to "0".

Hardware Reset

This is a factory configurable option of the /SHIP pin.

The Ship Mode feature can be disabled and the /SHIP pin can also be reconfigured to perform a Hardware Reset. When the /SHIP pin is held LOW for 8 s it will disable Q4 for 512 ms and discharge SYS using an internal 200 Ω pull−down. After the 512 ms period has passed, Q4 is re−enabled and the 200 Ω pull−down is disconnected from SYS. This feature allows for a quick system restart of a mobile device with an embedded battery by eliminating the time needed for the battery to self−discharge to the point where its protection switch opens.

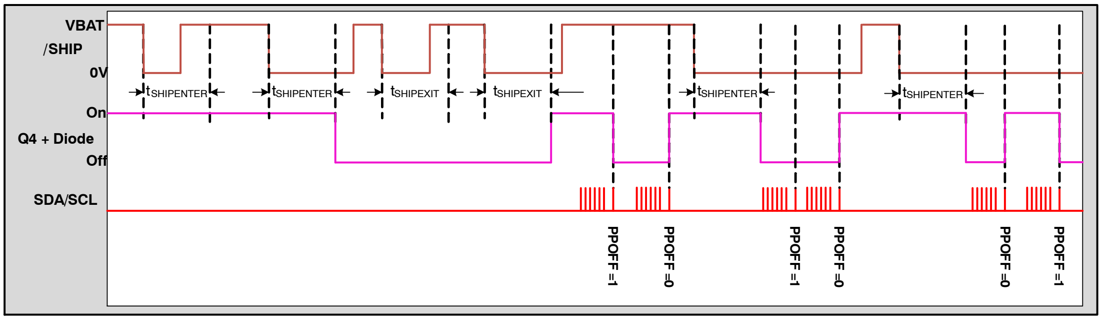


Figure 48. Ship Mode Control

BOOST CIRCUIT DETAILS

Refer to: *Boost State Diagram*

Q1 and Q2 operate as a synchronous boost regulator to provide power to the VBUS pin for USB−On−the−Go (OTG) applications using the battery as its input. The Boost output voltage can be programmed using the VBOOST (REG 1Ch[3:0]) bits.

Boost Enable and Programming

Boost Mode can be enabled by setting the BOOSTEN (REG 1Ch[5]) bit to “1”. BOOSTEN starts the boost operation, regulating VBOOST (REG1Eh[3:0]) at the PMID node. To provide power out to the VBUS pin, the OTG bit (REG 1Ch[6]) must also be set to “1”. Whenever boost mode is disabled, either by a fault or writing BOOSTEN=”0”, the OTG bit will be automatically reset to “0”.

The HZMODE (REG 0Eh[1]) bit will be ignored when the boost is enabled. The device will return to High Impedance Mode when BOOSTEN is set back to “0” or the DIS pin is raised HIGH.

The boost should not be enabled with a valid VIN present.

If a source is plugged into VIN while the boost is already running, VIN will be ignored (Q5 will remain off) until the boost is disabled.

Boost Mode and Timer Operation

It is recommended to enable the watchdog timer (t_{WD}) by setting WDEN (REG 19h[6]) bit to “1” to ensure that the host processor is controlling Boost Mode operation. The TMRRST (REG 19h[7]) bit must be set by the host before the t_{WD} timer times out. If t_{WD} times out in Boost Mode, the BOOSTEN and OTG bits are reset, and an interrupt is issued.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	BSTWDTTO (Reg.05h[1])
Status Bits:	BOOST (REG 01h[1])

Boost PWM Control

The IC uses a computed off−time and a regulated on−time (with an enforced minimum) to regulate V_{PMID}. The regulator achieves excellent transient response by employing current−mode modulation.

Since V_{BOOST} is regulated at the PMID node, V_{BUS} will exhibit a load−line equal to the $R_{DS(ON)}$ of Q3.

Boost PFM Mode

If $V_{PMID} > VREF_{BOOST}$ (nominally 5.00 V) when the minimum off−time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until $V_{PMID} < VREF_{BOOST}$. The minimum on−time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore the regulator behaves like a constant on−time regulator, with the bottom of its output voltage ripple at V_{BOOST} in PFM Mode.

Boost Startup

As the device should be in the Standby State when the boost is enabled, the BATFET (Q4) will already be enabled to support the system.

Soft−Start State

By setting BOOSTEN = “1”, the boost regulator begins switching with a reduced peak current limit of 50% of its normal current limit ($I_{LIMPK(BST)}$). The output slews up until V_{PMID} is within 5% of its setpoint (V_{BST}); at which time, the regulation loop is closed and the current limit is set to 100%.

If the output fails to achieve 95% of its setpoint within 128 μs, the current limit is increased to 100%. If the output fails to achieve 95% of its setpoint after an additional 1 ms period, a boost fault state is initiated and an interrupt is issued.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	BSTFAIL (Reg.05h[3])

Short Check State

The OTG (REG 1Ch[6]) control bit needs to be set in order to pass the boost output voltage (PMID) to V_{BUS} for USB On−the−Go operation. Once OTG is set to “1”, the Short Check state enables a resistor from PMID to V_{BUS} and waits for V_{BUS} to rise to about 1.5 V before proceeding with the VBUS Connect State. This prevents high current drain from the battery, which could occur if Q3 is turned on into a short circuit.

If V_{BUS} fails to rise above 1.5 V within 8 ms, an interrupt is issued, the resistor is disconnected between PMID and VBUS, and V_{PMID} remains regulated to V_{BOOST}.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	OTGOCP (REG 06h[2])

If the VBUS fault is removed, Short Check State will automatically retry after 2 seconds, and then proceed to the VBUS Connect State

VBUS Connect State

If a short is not detected on V_{BUS} during the Short Check State, Q3 will fully turn on and provide a low impedance path between PMID and VBUS. The resistor between PMID and VBUS is left connected. This state ends when V_{BUS} rises above V_{PMID} −400 mV within a 1 ms period, at which point boost regulation is achieved and a Status bit is set.

APPLICABLE STATUS AND INTERRUPT

Status Bits:	BOOST (REG 01h[1])

If V_{BUS} fails to reach V_{PMID}−400 mV within 1 ms, a boost fault state is initiated, and an interrupt is issued.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	BSTFAIL (REG 05h[3])

Boost State

This is the normal operating mode of the boost regulator.

The minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$, which keeps the regulator’s switching frequency relatively constant in CCM.

Boost Alert

When the battery voltage falls below 3.0 V an interrupt is issued warning that the battery is depleted. The /INT pin is pulled low to alert the processor of the condition. BOOSTEN is not reset.

APPLICABLE STATUS AND INTERRUPT

Pins:	/INT
Interrupt Bits:	VBATLV (REG 05h[0])
Status Bits:	BATLO (REG 01h[0])

Boost Faults

If a BOOST fault occurs:

1. The /INT Pin is pulled low for Interrupt faults.
2. BOOSTEN bit is reset to “0”. OTG bit is reset to “0”. Q3 is opened.
3. BOOST status bit is cleared.
4. The power stage is in High−Impedance Mode.
5. Interrupt bits are set per Table 20.

BOOSTEN is reset on boost faults. Boost Mode can only be re−enabled by setting the BOOSTEN bit.

Boost Shutdown

When the boost regulator is shut down (BOOSTEN = “0”), current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

Table 20. FAULT BITS DURING BOOST MODE

Fault Name	Fault Bit	Fault Description
BSTOVP	REG 05h[5]	$V_{PMID} > V_{BOOST\_OVP}$
BSTFAIL	REG 05h[3]	V_{PMID} fails to achieve the voltage required to advance to the next state during soft−start or sustained (> 50 μs) current limit during the BST state.
BATUVL	REG 05h[2]	$V_{BAT} < UVLO_{BST}$
BSTTSD	REG 05h[4]	Thermal Shutdown ($T > T_{REGTH}$)
BSTWDTTO	REG 05h[1]	Boost Watch Dog Timer Fault

LDO

The FAN5451x provides a 4.95 V (typical), 10 mA LDO that is sourced by PMID. The LDO is automatically enabled 32 ms after V_{BUS} or V_{IN} Plug In.

The LDO can be disabled by setting LDO_OFF (REG 0Dh[5]) to “1”. The LDO output voltage can be programmed using the VLDO (REG 0Dh[4:3]) bits.

Whenever the FAN5451x is operating in boost mode (BOOSTEN = “1”), the LDO will be disabled. When the LDO is disabled, an internal switch pulls the output low through a 1.2 kΩ pull−down resistor.

LDO and GPO Configurations

FAN54511A, FAN54511AP, FAN54513A only

The LDO output sources the high side of the GPO1 and GPO2 CMOS output drivers, while the gate of the output drivers are controlled by the GPO2 (REG 0Dh [7]) and GPO1 (REG 0Dh [6]) control bits. LDO and GPO1 are enabled by default.

I²C INTERFACE

The FAN5451x’s serial interface is compatible with Standard, Fast, Fast Plus, and High−Speed Mode I2C bus specifications. The FAN5451x’s SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls low during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 21. I²C Slave Address Byte

7	6	5	4	3	2	1	0
1	1	0	1	0	1	1	R/W

In hex notation, the slave address assumes a “0” LSB. The hex slave address is D6H (8−bit write address) for all parts in the family. Other slave addresses can be accommodated upon request. Contact your ON Semiconductor representative.

Bus Timing

As shown in Data Transfer Timing, data is normally transferred when SCL is low. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

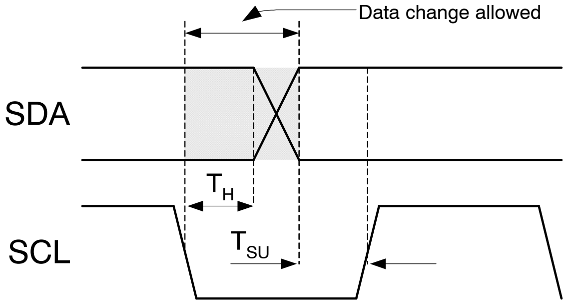


Figure 49. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH.

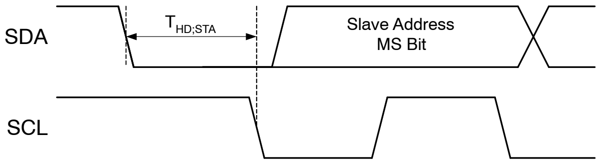


Figure 50. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from “0” to “1” with SCL high.

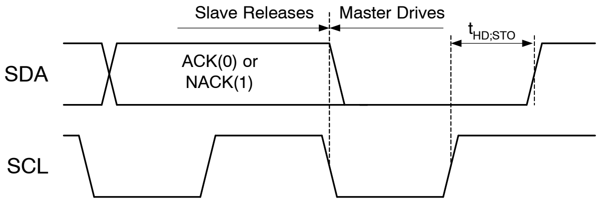


Figure 51. Stop Bit

During a read from the FAN5451x, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1−to−0 transition on SDA while SCL is high.

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (maximum 1 MHz clock); slaves do not ACK this transmission.

The master then generates a repeated start condition that causes all slaves on the bus to switch to HS Mode. The master then sends I2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit is sent by the master. While in HS Mode, packets are separated by repeated start conditions.

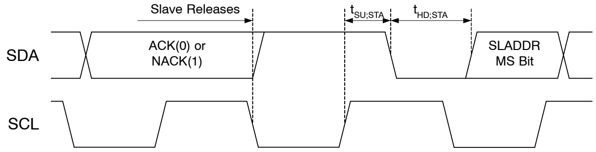


Figure 52. Repeated Start Time

READ AND WRITE TRANSACTIONS

Table 22. BIT DEFINITIONS

Symbol	Definition
S	START
A	ACK. The slave drives SDA to 0 acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	REPEATED START
P	STOP

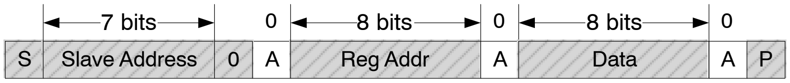


Figure 53. Write Transaction

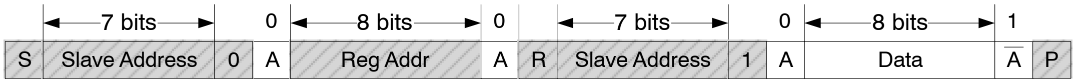


Figure 54. Read Transactions

SOLUTION DESIGN RECOMMENDATION

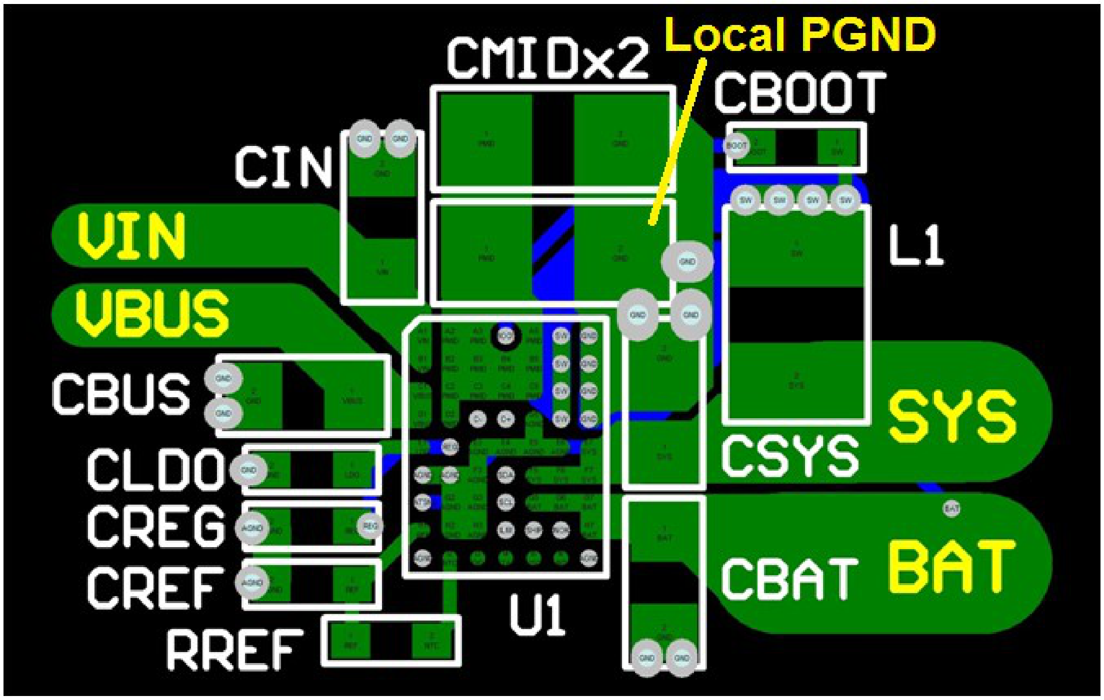


Figure 55. Recommended Component Placement and Routing

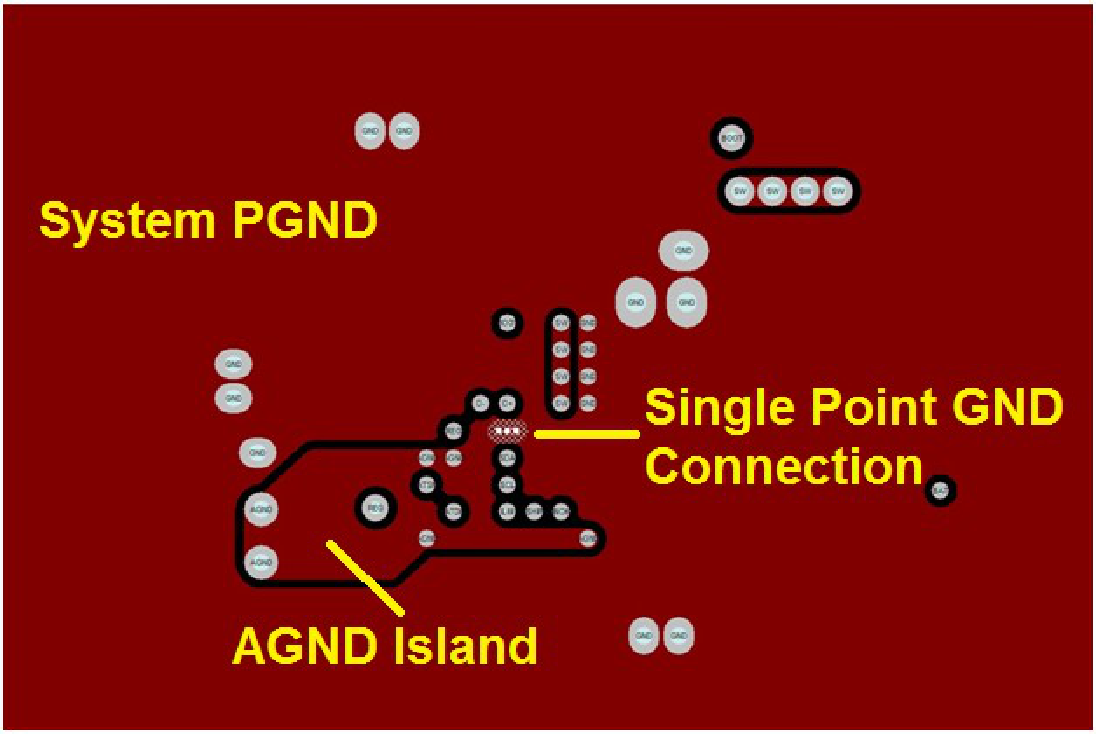


Figure 56. Recommended GND Connections

REGISTER AND BIT DESCRIPTIONS

The default states of the registers are with only the battery connected (VBUS and VIN not connected).

Table 23. I²C REGISTER MAP

REG NAME	ADR	DEFAULT	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS 0	00h	1000_0010	RESERVED	VINPWR	VBUSPWR	PWROK	STAT	PRE	SLEEP	NOBAT
STATUS 1	01h	0000_0000	LOIBAT	CHGDET		CHGCMP	TOCHG	DIVC	BOOST	BATLO
STATUS 2	02h	0000_0000	INPUTSEL	INPUTOVP	TEMPSD	TEMPFB	JEITA	TBAT	WDTTO	TMRTO
INT 0	04h	0000_0000	VALFAIL	VININT	VBUSINT	VLOWTH	CHGEND	CHGMOD	WKBAT	BATINT
INT 1	05h	0000_0000	IBATLO	RCHGN	BSTOVP	BSTTSD	BSTFAIL	BATUVL	BSTWDTTO	VBATLV
INT 2	06h	0000_0000	TOCMP	OVPINPUT	SHORTBAT	ICTEMP	BATTEMP	OTGOCP	BATOCP	TIMER
MINT 0	08h	0000_0000	MVALFAIL	MVININT	MVBUSINT	MVLOWTH	MCHGEND	MCHGMOD	MWKBAT	MBATINT
MINT 1	09h	0000_0000	MIBATLO	MRCHGN	MBSTOVP	MBSTTSD	MBSTFAIL	MBATUVL	RESERVED	MVBATLV
MINT 2	0Ah	0000_0000	MTOCMP	MOVPINPUT	MSHORTBAT	MICTEMP	MBATTEMP	MOTGOCP	MBATOCP	MTIMER
CONTROL 0	0Ch	0011_1111	RESERVED		VLOWV			VBATMIN		
CONTROL 1	0Dh	0101_0111	GP02	GPO1	LDO_OFF	VLDO		RESERVED	VSYS	
CONTROL 2	0Eh	0001_1100	CONT	RESERVED	RCHGDIS	NOBATOP	TE	TOEN	HZMODE	RESERVED
CONTROL 3	0Fh	0100_0000	RESET	TREGTH		RESERVED		PPOFFSLP	PPOFF	CE#
VFLOAT	11h	0110_1001	FLOAT							
IOCHRG	12h	0001_0000	RESERVED		IOCHRG					
IBAT	13h	1001_1000	ITERM				PRECHG			
IBUS	14h	0001_0000	RESERVED	IBUSLIM						
VBUS	15h	0010_0100	RESERVED		VBUSOVP		VBUSLIM			
IIN	16h	0001_1011	RESERVED	IINLIM						
VIN	17h	0001_0100	RESERVED		VINOVP		VINLIM			
NTC	18h	0000_1111	RESERVED		TEMPDIS	NTCOK	NTC4	NTC3	NTC2	NTC1
TIMER	19h	0001_1011	TMRRST	WDEN	RESERVED	PRETMR		FCTMR		
SAFETY	1Ah	1111_1111	SAFETY							
TOPOFF	1Bh	0000_0011	RESERVED				TO_BDETDIS	TOTMR		
BOOST	1Ch	0001_0010	RESERVED	OTG	BOOSTEN	RESERVED	VBOOST			
DPLUS	1Fh	0000_0000	FORCEDET	RESERVED						SETTMR0
MONITOR 0	20h	1000_0110	ITERMCMP	VBATCMP	VLOWVCMP	BATSHORT	HIVBAT	IBUS#	ICHG#	CV
MONITOR 1	21h	1010_0XXX	RESERVED	PMIDVBAT	PPON	BUCKON	ISRCCMP	NTCGND	DISPIN	ILIMPIN
IC_INFO	2Dh	10XX_XXXX	VENDOR CODE		PN			REV		
FEATURE CONTROL	30h	0010_0000	WDTEXP	RESERVED	DIVCON	DISREF	RESERVED		RESERVED	

Table 24. I²C REGISTER DESCRIPTIONS

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

STATUS 0				Register Address: 00h	Default Value = 1000 0010
Bit	**Name**	**Value**	**Type**	**Description**	
7	RESERVED	1	R	Reserved. This bit should always read “1”.	
6	VINPWR	0	R	A “1” indicates that an input source voltage at V_{IN} has risen above $V_{SOURCE(RISE)}$ and passed validation, and a valid VBUS is not present. To maintain a “1” $V_{SOURCE(FALL)} < V_{IN} < V_{INOVP}$ and $V_{IN} > V_{BAT} + V_{SLP}$. VINPWR will not be set to “1” if VBUSPWR = “1”.	
5	VBUSPWR	0	R	A “1” indicates that an input source voltage at V_{BUS} has risen above $V_{SOURCE(RISE)}$ and passed validation. To maintain a “1” $V_{SOURCE(FALL)} < V_{BUS} < V_{BUSOVP}$ and $V_{BUS} > V_{BAT} + V_{SLP}$.	
4	PWROK	0	R	A “1” indicates that $V_{BAT} > V_{LOWV}$ during charging. If HZ state is entered while PWROK is set to “1” and then V_{BAT} falls below V_{LOWV}, PWROK will not reset to “0” until after the source is re−validated and the IC returns to Charge Mode. Validation occurs whenever the part exits HZ State.	
3	STAT	0	R	A “1” indicates the /STAT pin is pulled low when charging is being performed. This bit goes to “0” during Top−Off charging.	
2	PRE	0	R	A “1” indicates that the charger is in Pre−Charge mode and a “0” indicates it is not. In conjunction with the STAT (REG 00h[3]) bit, the system processor can determine the type of charging being performed.	
1	SLEEP	1	R	A “1” indicates that the charger is in sleep mode. Sleep mode is entered when the highest available input source voltage drops below the higher of $V_{BAT} + V_{SLP}$ or $V_{SOURCE(FALL)}$.	
0	NOBAT	0	R	A “1” indicates that the IC has determined there is no battery connected.	

STATUS 1				Register Address: 01h	Default Value = 0000 0000
Bit	**Name**	**Value**	**Type**	**Description**	
7	LOIBAT	0	R	A “1” indicates that the battery is present but the current has fallen below the I_{TERM} threshold when TE= “0” or TOEN = “1”.	
6:5	CHGDET	00	R	Identifies the type of charger adapter connected to the VBUS input after adapter detection is completed. (FAN54510A, FAN54512A only). Binary Adapter Type 00 Detection not completed 01 SDP 10 CDP 11 DCP	
4	CHGCMP	0	R	A “1” indicates that the battery is charged ($I_{BAT} < I_{TERM}$) and that charging has completed when TE = “1”. This bit remains “0” during Top−Off charging.	
3	TOCHG	0	R	A “1” indicates Top−Off charging mode.	
2	DIVC	0	R	A “1” indicates that the Dynamic Input Voltage Control loop is active. If DIVC = “1”, the INPUTSEL (REG 02h[7]) status bit indicates whether the V_{BUSLIM} or V_{INLIM} voltage control loop is active.	
1	BOOST	0	R	A “1” indicates the device is in boost mode.	
0	BATLO	0	R	A “1” indicates that V_{BAT} < 3.0 V during Boost Operation only.	

Table 24. I^{2}C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

STATUS 2				**Register Address: 02h** **Default Value = 0000 0000**
Bit	**Name**	**Value**	**Type**	**Description**
7	INPUTSEL	0	R	Indicates which input is routed to PMID whenever a valid source is connected to VBUS or VIN. Binary Input 0 VBUS 1 VIN
6	INPUTOVP	0	R	A “1” indicates that V_{BUS} and/or V_{IN} is higher than its OVP threshold. Switching is stopped to protect the IC and the BATFET (Q4) is turned on to support the system load. If INPUTOVP = “1”, the INPUTSEL status bit (REG 02h[7]) state indicates whether the OVP condition exists on V_{BUS} or V_{IN}.
5	TEMPSD	0	R	A “1” indicates the charger is in thermal shutdown.
4	TEMPFB	0	R	A “1” indicates the charger is in thermal regulation.
3	JEITA	0	R	A “1” indicates the battery temperature is outside the JEITA normal temperature range during battery charging, charge current and float voltage have been reduced or charging has stopped, and NTC (REG 18h[3:0]) = “0000”,“0001”,“0111”, or “1111”. See (REG 18h[5:0]) for details on NTC operation.
2	TBAT	0	R	A “1” indicates the battery temperature is unsafe and, therefore, charging has been stopped and NTC (REG 18h[3:0]) = “0000” or “1111” See (REG 18h[5:0]) for details on NTC operation.
1	WDTTO	0	R	A “1” indicates the 100sec Watch Dog Timer has timed out in Charge Mode. When the watch dog timer expires, registers are reset to their default values and the WDEN (REG 19h[6]) control bit is cleared. Setting WDEN (REG 19h[6]) = “1” or a re−insertion of VBUS or VIN will reset WDTTO back to “0”.
0	TMRTO	0	R	A “1” indicates the safety timer expired during Pre−Charge or Fast Charge. A re−insertion of VBUS or VIN will reset WDTTO back to “0”.
INT 0				**Register Address: 04h** **Default Value = 0000 0000**
Bit	**Name**	**Value**	**Type**	**Description**
7	VALFAIL	0	RC	A “1” indicates that V_{BUS} or V_{IN} validation failed.
6	VININT	0	RC	VIN Plug In: A “1” indicates $V_{IN} > V_{SOURCE(RISE)}$. The bit will remain “0” if VBUS is already present. VIN Plug Out: A “1” indicates $V_{IN} < V_{SOURCE(FALL)}$ or $V_{IN} < V_{BAT}+V_{SLP}$. VBUS Plug Out with VIN Present: A “1” indicates that $V_{IN} > V_{SOURCE(RISE)}$. This VIN interrupt will not occur, though, until $V_{BUS} < V_{SOURCE(FALL)}$ or $V_{BUS} < V_{BAT}+V_{SLP}$.
5	VBUSINT	0	RC	VBUS Plug In: A “1” indicates $V_{BUS} > V_{SOURCE(RISE)}$. VBUS Plug Out: A “1” indicates $V_{BUS} < V_{SOURCE(FALL)}$ or $V_{BUS} < V_{BAT}+V_{SLP}$.
4	VLOWTH	0	RC	A “1” indicates the battery voltage has risen above or fallen below the V_{LOWV} threshold during charging or $V_{BAT} > V_{LOWV}$ at the start of charging. The interrupt will also occur at Plug Out if $V_{BAT} > V_{LOWV}$.
3	CHGEND	0	RC	A “1” indicates that the device has completed a normal charge cycle where I_{BAT} has fallen below the I_{TERM} threshold if TE = “1”. If configured to do so, the IC may continue charging in Top Off with CHGEND = “1”.
2	CHGMOD	0	RC	A “1” indicates that the charging mode has changed between Pre−Charge and Fast Charge modes.
1	WKBAT	0	RC	A “1” indicates the battery is below the V_{BATMIN} threshold set in VBATMIN (REG 0Ch[2:0]) at Plug In.
0	BATINT	0	RC	A “1” indicates that the IC has determined the battery presence has changed state. See NOBAT (REG 00h[0]) status bit.

Table 24. I²C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

INT 1				Register Address: 05h	Default Value = 0000 0000
Bit	**Name**	**Value**	**Type**	**Description**	
7	IBATLO	0	RC	A “1” indicates that the charging current has risen above or fallen below I_{TERM} when TE = “0”. The LOIBAT (REG 01h[7]) status bit should also be read to determine if the actual charging current is above or below the I_{TERM} threshold.	
6	RCHGN	0	RC	A “1” indicates that the battery voltage has fallen by V_{RCHG} below V_{FLOAT} after charging has completed.	
5	BSTOVP	0	RC	A “1” indicates that VBUS has risen above the boost OVP threshold.	
4	BSTTSD	0	RC	A “1” indicates that the IC junction temperature has exceeded the temperature shutdown threshold, T_{REGTH}, during boost operation.	
3	BSTFAIL	0	RC	V_{BUS} fails to achieve the voltage required to advance to the next state during soft–start or sustained (>50 μs) current limit during the boost state.	
2	BATUVL	0	RC	A “1” indicates that the battery voltage fell below $UVLO_{BST}$ during boost operation or that $V_{BAT}< UVLO_{BST}$ when the boost is first enabled.	
1	BSTWDTTO	0	RC	A “1” indicates the 100sec Watch Dog Timer has timed out during Boost Operation.	
0	VBATLV	0	RC	Provides an interrupt bit for indicating that the battery has fallen below 3.0 V during Boost Operation. Boost operation will continue until either BOOSTEN = “0” or $V_{BAT} < UVLO_{BST.}$	
INT 2				**Register Address: 06h**	**Default Value = 0000 0000**
Bit	**Name**	**Value**	**Type**	**Description**	
7	TOCMP	0	RC	A “1” indicates that Top–Off charging has completed with the expiration of the Top–Off timer when both TE=”1” and TOEN=”1”.	
6	OVPINPUT	0	RC	A “1” indicates that the V_{BUS} or V_{IN} voltage has risen above or fallen below the OVP threshold. See INPUTOVP (REG 02h[6]) Status bit.	
5	SHORTBAT	0	RC	A “1” indicates that V_{BAT} has fallen below V_{SHORT} during charging.	
4	ICTEMP	0	RC	A “1” indicates that the IC temperature has risen high enough to trigger Thermal Regulation (T_{REGTH}), or Thermal Shutdown ($T_{SHUTDOWN}$). If ICTEMP = “1”, see TEMPFB (REG 02h[4]) and TEMPSD (REG 02h[5]) Status bits to determine if the device is in Thermal Regulation or Thermal Shutdown.	
3	BATTEMP	0	RC	A “1” indicates that the battery temperature has changed status. If BATTEMP = “1”, see NTC (REG 18h[5:0]) for battery temperature details.	
2	OTGOCP	0	RC	A “1” indicates that the boost did not successfully pass the Short Check State.	
1	BATOCP	0	RC	A “1” indicates that the BATFET (Q4) has exceeded its discharge current limit.	
0	TIMER	0	RC	If running from the Safety Timer, a “1” indicates that the safety timer for Pre–Charge or Fast Charge has expired. See TMRTO (REG 02h[0]) Status bit. If running from the Watch Dog Timer, a “1” indicates that the watch dog timer has expired in boost or charge operation.	
MINT 0				**Register Address: 08h**	**Default Value = 0000 0000**
Bit	**Name**	**Value**	**Type**	**Description**	
7	MVALFAIL	0	R/W	Writing a “1” masks VALFAIL = “1” from driving the /INT pin LOW.	
6	MVININT	0	R/W	Writing a “1” masks VININT = “1” from driving the /INT pin LOW.	
5	MVBUSINT	0	R/W	Writing a “1” masks VBUSINT = “1” from driving the /INT pin LOW.	
4	MVLOWTH	0	R/W	Writing a “1” masks LOWTH = “1” from driving the /INT pin LOW.	
3	MCHGEND	0	R/W	Writing a “1” masks CHGEND = “1” from driving the /INT pin LOW.	
2	MCHGMOD	0	R/W	Writing a “1” masks CHGMOD = “1” from driving the /INT pin LOW.	
1	MWKBAT	0	R/W	Writing a “1” masks WKBAT = “1” from driving the /INT pin LOW.	
0	MBATINT	0	R/W	Writing a “1” masks BATINT = “1” from driving the /INT pin LOW.	

Table 24. I²C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

<table>
<tr><th colspan="4">MINT 1</th><th>Register Address: 09h</th><th>Default Value = 0000 0000</th></tr>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>MIBATLO</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks IBATLO = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>6</td><td>MRCHGN</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks RCHGN = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>5</td><td>MBSTOVP</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks BSTOVP = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>4</td><td>MBSTTSD</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks BSSTSD = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>3</td><td>MBSTFAIL</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks BSTFAIL = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>2</td><td>MBATUVL</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks BATULV = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>1</td><td>Reserved</td><td>0</td><td>R</td><td colspan="2"></td></tr>
<tr><td>0</td><td>MVBATLV</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks VBATLV = “1” from driving the /INT pin LOW.</td></tr>
<tr><th colspan="4">MINT 2</th><th>Register Address: 0Ah</th><th>Default Value = 0000 0000</th></tr>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>MTOCMP</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks TOCMP = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>6</td><td>MOVPINPUT</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks OVPINPUT = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>5</td><td>MSHORTBAT</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks SHORTBAT = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>4</td><td>MICTEMP</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks ICTEMP = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>3</td><td>MBATTEMP</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks BATTEMP = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>2</td><td>MOTGOCP</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks OTGOCP = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>1</td><td>MBATOCP</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks BATOCP = “1” from driving the /INT pin LOW.</td></tr>
<tr><td>0</td><td>MTIMER</td><td>0</td><td>R/W</td><td colspan="2">Writing a “1” masks TIMER = “1” from driving the /INT pin low if CONT = “1” (REG 0Eh [7]).
If CONT = “0”, MTIMER will be reset to “0” when a Pre−Charge or Fast Charge timer expires and will, therefore, not mask /INT bit.</td></tr>
<tr><th colspan="4">CONTROL 0</th><th>Register Address: 0Ch</th><th>Default Value = 0011 1111</th></tr>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7:6</td><td>Reserved</td><td>00</td><td>R</td><td colspan="2"></td></tr>
<tr><td>5:3</td><td>VLOWV</td><td>111</td><td>R/W</td><td colspan="2">This sets the good battery voltage threshold on the BAT pin, above which full system power is available to the user.
Binary V_{LOWV} (V)
000 3.0
001 3.1
010 3.2
011 3.3
100 3.4
101 3.5
110 3.6
111 3.7</td></tr>
<tr><td>2:0</td><td>VBATMIN</td><td>111</td><td>R/W</td><td colspan="2">This sets the voltage threshold on the BAT pin above which Fast Charge begins. VBATMIN should not be set lower than the minimum required system voltage.
Binary V_{BATmin} (V)
000 2.7
001 2.8
010 2.9
011 3.0
100 3.1
101 3.2
110 3.3
111 3.4</td></tr>
</table>

Table 24. I^{2}C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

CONTROL 1				Register Address: 0Dh	Default Value = 0101 0111
Bit	**Name**	**Value**	**Type**	**Description**	
7	GPO2	0	R/W	A “1” enables GPO2 to output logic high. GPO2 is sourced by the LDO. (FAN54511A, FAN54511AP, FAN54513A only)	
6	GPO1	1	R/W	A “1” enables GPO1 to output logic high. GPO1 is sourced by the LDO. (FAN54511A, FAN54511AP, FAN54513A only)	
5	LDO_OFF	0	R/W	A “1” disables the LDO.	
4:3	VLDO	10	R/W	Sets the LDO output voltage. The LDO input is sourced from PMID. Binary V_{LDO} (V) 00 3.30 01 3.60 10 4.95 11 5.05	
2	Reserved	1	R		
1:0	VSYS	11	R/W	Regulated system voltage in Pre−Charge Mode ($V_{BAT} < V_{BATMIN}$). VSYS should be programmed 250mV, or more, above the minimum required system voltage. With limited available input power, V_{SYS} can be up to 250 mV below its programmed target level. Binary V_{SYS} (V) 00 3.3 01 3.4 10 3.5 11 3.6	
CONTROL2				**Register Address: 0Eh**	**Default Value = 0001 1100**
Bit	**Name**	**Value**	**Type**	**Description**	
7	CONT	0	W	Writing a “1” ignores a Pre−Charge or Fast Charge Safety Timer expiration fault and allows the IC to continue charging. However, the TMRTO (REG 02h[0]) status bit and TIMER (REG 06h[0]) interrupt bit will still be set to “1” upon timer expiration. A “0” will reset all registers except SAFETY and put the charger IC into IDLE State when the Pre−Charge or Fast Charge Safety Timer expires. CONT does not affect the watchdog timer or top−off timer. Reading this bit always returns “0”.	
6	Reserved	0	R		
5	RCHGDIS	0	R/W	Writing a “1” disables the automatic recharge function with TE = “1” when the battery voltage falls below $V_{FLOAT} - V_{RCHG}$.	
4	NOBATOP	1	R/W	For a “0”, if no battery is detected during source plug−in or when a Full Battery (end of charge) is reached, the charger will not perform an additional battery absence test. The buck converter will stay on and the BATFET turns off allowing the host processor to continue to run with no battery. For a “1” if no battery is detected during source plug−in or when a Full Battery (end of charge) is reached, the charger will perform a battery absence test every 2 seconds until a battery is connected. The buck converter will stay on and the BATFET (Q4) turns off allowing the host processor to continue to run with no battery.	
3	TE	1	R/W	A “1” enables charge current termination and a “0” allows charging to continue even if $I_{BAT} < I_{TERM}$.	
2	TOEN	1	R/W	A “1” enables the Top−Off charging.	
1	HZMODE	0	R/W	A “1” puts the IC in the High−Z state. This bit will be ignored when BOOSTEN = “1”, but device will return to HZ state when BOOSTEN is set back to “0”. The bit will reset to “0” when V_{BAT} falls below V_{BATMIN}. When $V_{BAT} < V_{BATMIN}$, writes to this bit are ignored.	
0	Reserved	0	R		

Table 24. I^{2}C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

CONTROL3				**Register Address: 0Fh**	**Default Value = 0100 0000**
Bit	**Name**	**Value**	**Type**	**Description**	
7	RESET	0	R/W	Writing a “1” resets all registers to their defaults: writing a “0” has no effect. Read returns “0”.	
6:5	TREGTH	10	R/W	Temperature threshold at which the current is reduced to prevent the device from overheating. Binary T_{REGTH} (°C) 00 70 01 85 10 100 11 120	
4:3	Reserved	0	R		
2	PPOFFSLP	0	R/W	PPOFFSLP is for automatic Ship Mode entry once the input source (VBUS or VIN) is removed. When PPOFFSLP is set to a “1”, PPOFF will be automatically written to “1” when V_{BUS} or V_{IN} falls below $V_{SOURCE(FALL)}$. PPOFFSLP will be reset to “0” once a valid input power source is connected.	
1	PPOFF	0	R/W	Writing a “1” to this bit turns the BATFET (Q4) off immediately. While PPOFF is set to “1”, supplemental mode is not allowed. Bit Reset Behavior PPOFFSLP = “1” (Ship Mode): PPOFF and PPOFFSLP will be reset to “0” when a valid input source is connected. PPOFFSLP=”0”: PPOFF will be reset to “0” when a valid input source is either removed or connected.	
0	CE#	0	R/W	During a normal charging condition, a “0” enables the BATFET, Q4 and a “1” disables the BATFET (Q4) but will allow the battery to supplement the SYS load when V_{SYS} falls below V_{BAT}.	

Table 24. I²C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

VFLOAT				Register Address: 11h	Default Value=0110 1001
Bit	**Name**	**Value**	**Type**	**Description**	
7:0	FLOAT	01101001	R/W	Charger output “float” voltage, V_{FLOAT}. Programmable from 3.3 V to 4.72 V in 10 mV increments. Default is 4.35 V	

Hex	V_{FLOAT}(V)	Hex	V_{FLOAT}(V)	Hex	V_{FLOAT}(V)
00	3.30	37	3.85	6E	4.40
01	3.31	38	3.86	6F	4.41
02	3.32	39	3.87	70	4.42
03	3.33	3A	3.88	71	4.43
04	3.34	3B	3.89	72	4.44
05	3.35	3C	3.90	73	4.45
06	3.36	3D	3.91	74	4.46
07	3.37	3E	3.92	75	4.47
08	3.38	3F	3.93	76	4.48
09	3.39	40	3.94	77	4.49
0A	3.40	41	3.95	78	4.50
0B	3.41	42	3.96	79	4.51
0C	3.42	43	3.97	7A	4.52
0D	3.43	44	3.98	7B	4.53
0E	3.44	45	3.99	7C	4.54
0F	3.45	46	4.00	7D	4.55
10	3.46	47	4.01	7E	4.56
11	3.47	48	4.02	7F	4.57
12	3.48	49	4.03	80	4.58
13	3.49	4A	4.04	81	4.59
14	3.50	4B	4.05	82	4.60
15	3.51	4C	4.06	83	4.61
16	3.52	4D	4.07	84	4.62
17	3.53	4E	4.08	85	4.63
18	3.54	4F	4.09	86	4.64
19	3.55	50	4.10	87	4.65
1A	3.56	51	4.11	88	4.66
1B	3.57	52	4.12	89	4.67
1C	3.58	53	4.13	8A	4.68
1D	3.59	54	4.14	8B	4.69
1E	3.60	55	4.15	8C	4.70
1F	3.61	56	4.16	8D	4.71
20	3.62	57	4.17	8E	4.72
21	3.63	58	4.18		
22	3.64	59	4.19		
23	3.65	5A	4.20		
24	3.66	5B	4.21		
25	3.67	5C	4.22		
26	3.68	5D	4.23		
27	3.69	5E	4.24		
28	3.70	5F	4.25		
29	3.71	60	4.26		
2A	3.72	61	4.27		
2B	3.73	62	4.28		
2C	3.74	63	4.29		
2D	3.75	64	4.30		
2E	3.76	65	4.31		
2F	3.77	66	4.32		
30	3.78	67	4.33		
31	3.79	68	4.34		
32	3.80	69	4.35		
33	3.81	6A	4.36		
34	3.82	6B	4.37		
35	3.83	6C	4.38		
36	3.84	6D	4.39		

Bits 8Fh − FFh = 4.72 V

Table 24. I2C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

IOCHRG	Register Address: 12h	Default Value=0001 0000

Bit	Name	Value	Type	Description
7:6	Reserved	00	R	
5:0	IOCHRG	010000	R/W	Sets the typical battery charging current, I_{OCHRG}, during Fast Charging. Programmable from 0.200 A to 3.200 A in 50 mA increments. Default is 1.000 A.

Hex	I_{OCHRG}(A)	Hex	I_{OCHRG}(A)	Hex	I_{OCHRG}(A)
00	0.200	15	1.250	2A	2.300
01	0.250	16	1.300	2B	2.350
02	0.300	17	1.350	2C	2.400
03	0.350	18	1.400	2D	2.450
04	0.400	19	1.450	2E	2.500
05	0.450	1A	1.500	2F	2.550
06	0.500	1B	1.550	30	2.600
07	0.550	1C	1.600	31	2.650
08	0.600	1D	1.650	32	2.700
09	0.650	1E	1.700	33	2.750
0A	0.700	1F	1.750	34	2.800
0B	0.750	20	1.800	35	2.850
0C	0.800	21	1.850	36	2.900
0D	0.850	22	1.900	37	2.950
0E	0.900	23	1.950	38	3.000
0F	0.950	24	2.000	39	3.050
10	1.000	25	2.050	3A	3.100
11	1.050	26	2.100	3B	3.150
12	1.100	27	2.150	3C	3.200
13	1.150	28	2.200		
14	1.200	29	2.250		

Bits 3Dh – 3Fh = 3.200 A

IBAT	Register Address: 13h	Default Value = 1001 1000

Bit	Name	Value	Type	Description
7:4	ITERM	1001	R/W	Sets the termination current threshold, I_{TERM}. Programmable from 100 mA to 600 mA. Default is 300 mA. If TE = “1” and the charge current falls below the termination current threshold, charging will stop.

Binary	I_{TERM} (A)	Binary	I_{TERM} (A)
0000	Reserved	1000	0.250
0001	Reserved	1001	0.300
0010	Reserved	1010	0.350
0011	0.100	1011	0.400
0100	0.125	1100	0.450
0101	0.150	1101	0.500
0110	0.175	1110	0.550
0111	0.200	1111	0.600

Bit	Name	Value	Type	Description
3:0	PRECHG	1000	R/W	Sets the typical battery charging current, I_{PP}, during Pre−Charge Mode. Programmable from 200 mA to 800 mA. Default is 450 mA.

Binary	I_{PP} (A)	Binary	I_{PP} (A)
0000	Reserved	1000	0.450
0001	Reserved	1001	0.500
0010	Reserved	1010	0.550
0011	0.200	1011	0.600
0100	0.250	1100	0.650
0101	0.300	1101	0.700
0110	0.350	1110	0.750
0111	0.400	1111	0.800

Table 24. I^2C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

IBUS				**Register Address: 14h**	**Default Value = 0001 0000**
Bit	**Name**	**Value**	**Type**	**Description**	
7	Reserved	0	R		
6:0	IBUSLIM	0010000	R/W	This sets the maximum input current limit, I_{BUSLIM}, from the VBUS input. Programmable from 100 mA to 3.00 A in 25 mA steps. Default is 500 mA. There are 3 FET segmentation ranges: 00h (100 mA) to 08h (300 mA), 09h (325 mA) to 23h (975 mA), and 24h (1000 mA) to 7Fh (3000 mA). Refer to the Electrical Specifications table for the associated $R_{DS(ON)}$ values.	

Hex	I_{BUSLIM} (A)	Hex	IBUSLIM (A)	Hex	I_{BUSLIM} (A)	Hex	I_{BUSLIM} (A)
00	0.100	1D	0.825	3A	1.550	57	2.275
01	0.125	1E	0.850	3B	1.575	58	2.300
02	0.150	1F	0.875	3C	1.600	59	2.325
03	0.175	20	0.900	3D	1.625	5A	2.350
04	0.200	21	0.925	3E	1.650	5B	2.375
05	0.225	22	0.950	3F	1.675	5C	2.400
06	0.250	23	0.975	40	1.700	5D	2.425
07	0.275	24	1.000	41	1.725	5E	2.450
08	0.300	25	1.025	42	1.750	5F	2.475
09	0.325	26	1.050	43	1.775	60	2.500
0A	0.350	27	1.075	44	1.800	61	2.525
0B	0.375	28	1.100	45	1.825	62	2.550
0C	0.400	29	1.125	46	1.850	64	2.600
0D	0.425	2A	1.150	47	1.875	65	2.625
0E	0.450	2B	1.175	48	1.900	66	2.650
0F	0.475	2C	1.200	49	1.925	67	2.675
10	0.500	2D	1.225	4A	1.950	68	2.700
11	0.525	2E	1.250	4B	1.975	69	2.725
12	0.550	2F	1.275	4C	2.000	6A	2.750
13	0.575	30	1.300	4D	2.025	6B	2.775
14	0.600	31	1.325	4E	2.050	6C	2.800
15	0.625	32	1.350	4F	2.075	6D	2.825
16	0.650	33	1.375	50	2.100	6E	2.850
17	0.675	34	1.400	51	2.125	6F	2.875
18	0.700	35	1.425	52	2.150	70	2.900
19	0.725	36	1.450	53	2.175	71	2.925
1A	0.750	37	1.475	54	2.200	72	2.950
1B	0.775	38	1.500	55	2.225	73	2.975
1C	0.800	39	1.525	56	2.250	74	3.000

Bits 75h – 7Fh = 3.000 A

Table 24. I²C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

<table>
<tr><th colspan="4">VBUS</th><th>Register Address: 15h</th><th>Default Value = 0010 0100</th></tr>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7:6</td><td>Reserved</td><td>00</td><td>R</td><td colspan="2"></td></tr>
<tr><td>5:4</td><td>VBUSOVP</td><td>10</td><td>R/W</td><td colspan="2">This sets the V_{BUS_OVP} threshold.
Binary V_{BUS_OVP} (V)
00 6.5
01 10.5
10 13.7
11 Reserved</td></tr>
<tr><td>3:0</td><td>VBUSLIM</td><td>0100</td><td>R/W</td><td colspan="2">This sets the V_{BUS} voltage, V_{BUSLIM}, which the Dynamic Input Voltage Control loop will regulate to in a charging scenario where a current−limited weak adapter is connected to VBUS.
Binary V_{BUSLIM} (V)
0000 4.240
0001 4.320
0010 4.400
0011 4.480
0100 4.560
0101 4.640
0110 4.720
0111 4.800
1000 7.632
1001 7.776
1010 7.920
1011 8.064
1100 8.208
1101 8.352
1110 8.496
1111 8.640</td></tr>
</table>

Table 24. I²C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

<table>
<tr><th colspan="4">IIN</th><th>Register Address: 16h</th><th>Default Value = 0001 1011</th></tr>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>Reserved</td><td>0</td><td>R</td><td colspan="2"></td></tr>
<tr><td>6:0</td><td>IINLIM</td><td>0011011</td><td>R/W</td><td colspan="2">This sets the maximum input current limit from the VIN input.
Programmable from 325 mA to 2 A in 25 mA steps. Default is 1 A.
<table>
<tr><td>Hex</td><td>I_{INLIM} (A)</td><td>Hex</td><td>I_{INLIM} (A)</td><td>Hex</td><td>I_{INLIM} (A)</td></tr>
<tr><td>00</td><td>0.325</td><td>1D</td><td>1.050</td><td>3A</td><td>1.775</td></tr>
<tr><td>01</td><td>0.350</td><td>1E</td><td>1.075</td><td>3B</td><td>1.800</td></tr>
<tr><td>02</td><td>0.375</td><td>1F</td><td>1.100</td><td>3C</td><td>1.825</td></tr>
<tr><td>03</td><td>0.400</td><td>20</td><td>1.125</td><td>3D</td><td>1.850</td></tr>
<tr><td>04</td><td>0.425</td><td>21</td><td>1.150</td><td>3E</td><td>1.875</td></tr>
<tr><td>05</td><td>0.450</td><td>22</td><td>1.175</td><td>3F</td><td>1.900</td></tr>
<tr><td>06</td><td>0.475</td><td>23</td><td>1.200</td><td>40</td><td>1.925</td></tr>
<tr><td>07</td><td>0.500</td><td>24</td><td>1.225</td><td>41</td><td>1.950</td></tr>
<tr><td>08</td><td>0.525</td><td>25</td><td>1.250</td><td>42</td><td>1.975</td></tr>
<tr><td>09</td><td>0.550</td><td>26</td><td>1.275</td><td>43</td><td>2.000</td></tr>
<tr><td>0A</td><td>0.575</td><td>27</td><td>1.300</td><td></td><td></td></tr>
<tr><td>0B</td><td>0.600</td><td>28</td><td>1.325</td><td></td><td></td></tr>
<tr><td>0C</td><td>0.625</td><td>29</td><td>1.350</td><td></td><td></td></tr>
<tr><td>0D</td><td>0.650</td><td>2A</td><td>1.375</td><td></td><td></td></tr>
<tr><td>0E</td><td>0.675</td><td>2B</td><td>1.400</td><td></td><td></td></tr>
<tr><td>0F</td><td>0.700</td><td>2C</td><td>1.425</td><td></td><td></td></tr>
<tr><td>10</td><td>0.725</td><td>2D</td><td>1.450</td><td></td><td></td></tr>
<tr><td>11</td><td>0.750</td><td>2E</td><td>1.475</td><td></td><td></td></tr>
<tr><td>12</td><td>0.775</td><td>2F</td><td>1.500</td><td></td><td></td></tr>
<tr><td>13</td><td>0.800</td><td>30</td><td>1.525</td><td></td><td></td></tr>
<tr><td>14</td><td>0.825</td><td>31</td><td>1.550</td><td></td><td></td></tr>
<tr><td>15</td><td>0.850</td><td>32</td><td>1.575</td><td></td><td></td></tr>
<tr><td>16</td><td>0.875</td><td>33</td><td>1.600</td><td></td><td></td></tr>
<tr><td>17</td><td>0.900</td><td>34</td><td>1.625</td><td></td><td></td></tr>
<tr><td>18</td><td>0.925</td><td>35</td><td>1.650</td><td></td><td></td></tr>
<tr><td>19</td><td>0.950</td><td>36</td><td>1.675</td><td></td><td></td></tr>
<tr><td>1A</td><td>0.975</td><td>37</td><td>1.700</td><td></td><td></td></tr>
<tr><td>1B</td><td>1.000</td><td>38</td><td>1.725</td><td></td><td></td></tr>
<tr><td>1C</td><td>1.025</td><td>39</td><td>1.750</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td colspan="4"></td><th colspan="2">Bits 44h – 7Fh = 2.000 A</th></tr>
</table>

Table 24. I^{2}C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

VIN				Register Address: 17h Default Value = 0001 0100
Bit	**Name**	**Value**	**Type**	**Description**
7:6	Reserved	00	R	
5:4	VINOVP	01	R/W	This sets the V_{IN_OVP} threshold. Binary V_{IN_OVP} (V) 00 6.5 01 10.5 10 13.7 11 Reserved
3:0	VINLIM	0100	R/W	This sets the V_{IN} voltage, $V_{INLIM,}$ which the Dynamic Input Voltage Control loop will regulate to in a charging scenario where a current−limited weak adapter is connected to VIN. Binary V_{INLIM} (V) 0000 4.240 0001 4.320 0010 4.400 0011 4.480 0100 4.560 0101 4.640 0110 4.720 0111 4.800 1000 7.632 1001 7.776 1010 7.920 1011 8.064 1100 8.208 1101 8.352 1110 8.496 1111 8.640

NTC				Register Address: 18h Default Value = 0000 1111
Bit	**Name**	**Value**	**Type**	**Description**
7:6	Reserved	00	R	
5	TEMPDIS	0	R/W	This controls whether the NTC circuit affects the charge current. Temperature measurements will continue to be updated every 1 second in the NTC1 − 4 monitor bits. Binary NTC Operation 0 NTC measurement affects charge parameters 1 NTC measurement does not affect charge parameters
4	NTCOK	0	R	“0” if NTC is either shorted to ground, open or shorted to REF.
3	NTC4	1	R	A “1” indicates that NTC is above the T4 threshold. (Note 14)
2	NTC3	1	R	A “1” indicates that NTC is above the T3 threshold. (Note 14)
1	NTC2	1	R	A “1” indicates that NTC is above the T2 threshold. (Note 14)
0	NTC1	1	R	A “1” indicates that NTC is above the T1 threshold. (Note 14)

Table 24. I^2C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

TIMER				Register Address: 19h	Default Value = 0001 1011
Bit	**Name**	**Value**	**Type**	**Description**	
7	TMRRST	0	W	Writing a “1” resets the Watch Dog Timer; writing a “0” has no effect. Reading this bit always returns “0”.	
6	WDEN	0	R/W	Writing a “1” enables the Watchdog timer (t_{WD}) and disables the Safety timer.	
5	Reserved	0	R		
4:3	PRETMR	11	R/W	These bits set the Pre−Charge safety timer. SETTMR0 (REG 1Fh[0] must be set to “1” immediately after the Pre−Charge timer value is changed to restart the timer in the programmed configuration. Binary Pre−Charge Safety Timer 00 Follows FCTMR (REG 19h[2:0]) programming 01 100 seconds 10 15 minutes 11 36 minutes	
2:0	FCTMR	011	R/W	This sets the Fast Charge safety timer. Binary Fast Charge Safety Timer (Hours) 000 Never Expires 001 4 010 6 011 8 100 10 101 12 110 14 111 16	

SAFETY				Register Address: 1Ah	Default Value = 1111 1111
Bit	**Name**	**Value**	**Type**	**Description**	
7:4	VSAFE	1111	R/W	These bits set the maximum programmable FLOAT (REG 11h[7:0]) value. Binary V_{FLOAT} Max. (Hex) V_{FLOAT} Max. (V) 0000 00 3.30 0001 0A 3.40 0010 14 3.50 0011 1E 3.60 0100 28 3.70 0101 32 3.80 0110 3C 3.90 0111 46 4.00 1000 50 4.10 1001 5A 4.20 1010 64 4.30 1011 6E 4.40 1100 78 4.50 1101 82 4.60 1110 8C 4.70 1111 8E − FF 4.72	
3:0	ISAFE	1111	R/W	These bits set the maximum programmable IOCHRG (REG 12h[5:0]) value. Binary I_{OCHRG} Max. (Hex) I_{OCHRG} Max. (A) 0000 00 0.20 0001 04 0.40 0010 08 0.60 0011 0C 0.80 0100 10 1.00 0101 14 1.20 0110 18 1.40 0111 1C 1.60 1000 20 1.80 1001 24 2.00 1010 28 2.20 1011 2C 2.40 1100 30 2.60 1101 34 2.80 1110 38 3.00 1111 3C 3.20	

Table 24. I^{2}C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

TOPOFF				**Register Address: 1Bh**	**Default Value = 0000 0011**
Bit	**Name**	**Value**	**Type**	**Description**	
7:4	Reserved	0000	R		
3	TO_BDETDIS	0	R/W	Setting this bit “1” disables the periodic battery check during top−off charging.	
2:0	TOTMR	011	R/W	This sets the Top−Off charge timer. Binary Top Off Timer (min.) 000 Never Expires 001 10 010 20 011 30 100 40 101 50 110 60 111 70	

BOOST				**Register Address: 1Ch**	**Default Value = 0001 0010**
Bit	**Name**	**Value**	**Type**	**Description**	
7	Reserved	0	R		
6	OTG	0	R/W	Connects PMID to VBUS when the boost is enabled (BOOSTEN = “1”). This will reset when BOOSTEN = “0”.	
5	BOOSTEN	0	R/W	This programs the operation of the switch−mode converter to charge or boost mode. If a fault occurs during boost mode the BOOSTEN bit and the OTG bit will reset. BOOSTEN Switch−Mode Converter 0 Charge Mode 1 Boost Mode	
4	Reserved	1	R		
3:0	VBOOST	0010	R/W	This sets the boost converter output voltage, V_{BOOST}. Programmable from 4.947 V to 5.347 V in 26.67 mV steps. Default is 5.00 V. Binary V_{BOOST} (V) 0000 4.947 0001 4.973 0010 5.000 0011 5.027 0100 5.053 0101 5.080 0110 5.107 0111 5.133 1000 5.160 1001 5.187 1010 5.213 1011 5.240 1100 5.267 1101 5.293 1110 5.320 1111 5.347	

DPLUS				**Register Address: 1Fh**	**Default Value = 0000 0000**
Bit	**Name**	**Value**	**Type**	**Description**	
7	FORCEDET	0	R/W	Setting this bit to “1” forces a BC1.2 detection on D+ and D−.	
6:1	Reserved	000000	R		
0	SETTMR0	0	W	While operating on the Safety Timer a “1” restarts the timer. During Pre−Charge, SETTMR0 must be set to “1” immediately after the Pre−Charge timer (PRETMR (REG 19h [4:3]) value is changed in order to restart the timer in the programmed configuration. Reading this bit always returns “0”.	

Table 24. I^{2}C REGISTER DESCRIPTIONS (continued)

This table defines the operation of each register bit for all IC versions. Default values are with VBAT = 3.8 V and VBUS = VIN = open.

MONITOR 0				**Register Address: 20h**	**Default Value = 1000 0110**
Bit	**Name**	**Value**	**Type**	**Description**	
7	ITERMCMP	1	R	I_{TERM} comparator output: “1” when I_{BAT} > ITERM reference or VBUS/ VIN not present.	
6	VBATCMP	0	R	Output of VBAT comparator: “1” when $V_{BAT} > V_{BATMIN}$.	
5	VLOWVCMP	0	R	Output of VLOWV comparator. In Fast Charge mode, a “1” indicates when $V_{BAT} > V_{LOWV}$. In Pre−Charge mode, a “1” indicates when $V_{SYS} > V_{BATMIN}$. In Boost mode, a “1” indicates when V_{BAT} > VBATLV threshold.	
4	BATSHORT	0	R	A “1” indicates that $V_{BAT} > V_{SHORT}$ in any charge mode or HZ. In Boost mode, a “1” indicates that $V_{SYS} > UVLO_{BST}$.	
3	HIVBAT	0	R	A “1” indicates that $V_{BAT} \geq V_{FLOAT}$ when charge termination, TE bit is set to “0”.	
2	IBUS#	1	R	A “0” indicates the I_{BUS} or I_{IN} loop is controlling the battery charge current.	
1	ICHG#	1	R	A “0” indicates the I_{OCHRG} loop is controlling the battery charge current.	
0	CV	0	R	A “1” indicates the constant−voltage (CV) loop is controlling the charger and all current loops have released.	
MONITOR 1				**Register Address: 21h**	**Default Value = 1010 0XXX**
Bit	**Name**	**Value**	**Type**	**Description**	
7	Reserved	1	R		
6	PMIDVBAT	0	R	A “1” indicates that $V_{PMID} > V_{BAT}$.	
5	PPON	1	R	A “1” if charging and $V_{BAT} > V_{SHORT}$ or if the IC is in Standby or HZ.	
4	BUCKON	0	R	A “1” indicates the buck converter is on.	
3	ISRCCMP	0	R	A “1” indicates that either V_{BUS} or V_{IN} has risen above $V_{SOURCE(RISE)}$ and is currently above $V_{SOURCE(RISE)}$. A “0” indicates that both V_{BUS} and V_{IN} are below $V_{SOURCE(FALL)}$.	
2	NTCGND	X	R	A “1” indicates that the NTC pin was tied to ground at V_{BUS}_POR.	
1	DISPIN	X	R	A “1” indicates that the DIS pin has been externally driven HIGH.	
0	ILIMPIN	X	R	A “1” indicates that the ILIM pin has been externally driven HIGH.	
IC_INFO				**Register Address: 2Dh**	**Default Value = 10XX XXXX**
Bit	**Name**	**Value**	**Type**	**Description**	
7:6	Vendor Code	10	R	Identifies ON Semiconductor as the IC supplier.	
5:3	PN	XXX	R	Part numbers bits, see the Ordering Info in Table 2.	
2:0	REV	XXX	R	IC Revision	
FEATURE CONTROL				**Register Address: 30h**	**Default Value = 0010 0000**
Bit	**Name**	**Value**	**Type**	**Description**	
7	WDTEXP	0	R/W	A “1” will reset all registers except SAFETY and put the charger IC into IDLE State when the Watch Dog Timer (WDT) expires.	
6	Reserved	0	R		
5	DIVCON	1	R/W	A “0” disables Dynamic Input Voltage Control (DIVC).	
4	DISREF	0	R/W	A “1” will disable the REF output and NTC functionality. JEITA not enforced.	
3	Reserved	0	R		
2	Reserved	0	R		
1	Reserved	0	R		
0	Reserved	0	R		

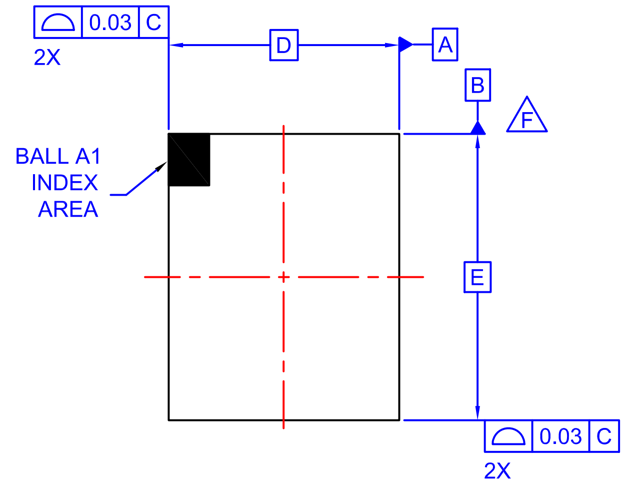
14. Without power from VBUS or VIN, the reference will not be powered and the NTC pin will be at ground. See applications section for more detail.

PRODUCT−SPECIFIC DIMENSIONS (MM)

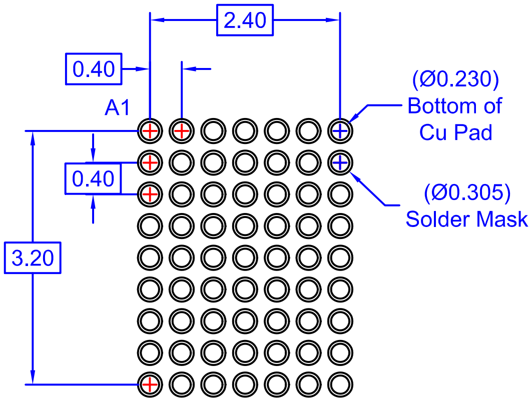
Product	E	D	X	Y
FAN5451xAUCX	3.63 ± 0.03	2.83 ± 0.03	0.195	0.195

WLCSP63 3.63x2.83x0.522
CASE 567TM
ISSUE O

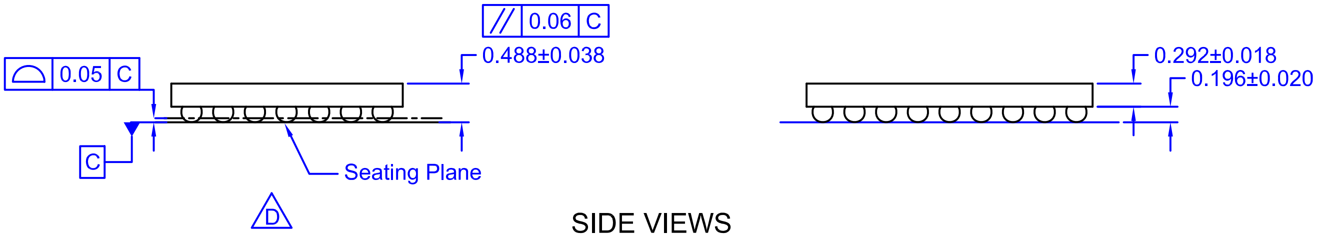
DATE 31 MAR 2017



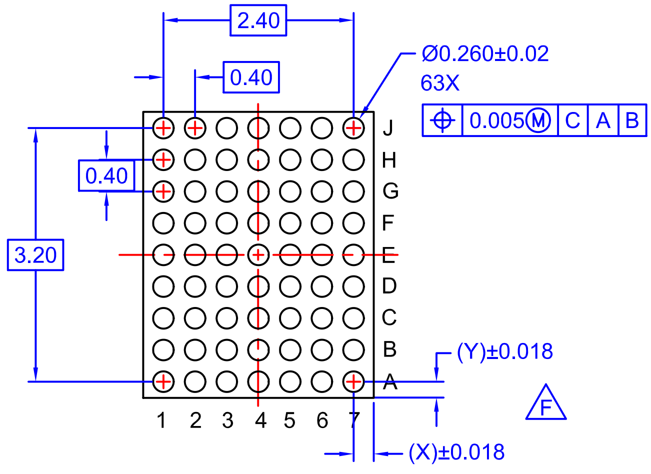
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.

△D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

△E. PACKAGE NOMINAL HEIGHT IS 488 ± 38 MICRONS (450-526 MICRONS).

△F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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DESCRIPTION:	**WLCSP63 3.63x2.83x0.522**	**PAGE 1 OF 1**

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