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FAN6291QF/FAN6291QH

Compact Secondary-Side Adaptive Charging Controller Synchronous Rectifier Control and USB Type-C Control

FAN6291QF/FAN6291QH are highly integrated, secondary-side power adaptor controllers compatible with the Quick Charge 3.0 (QC3.0) protocol. Internally adopted synchronous rectifier control helps for less BOM counts as well as for easy design.

FAN6291QF/FAN6291QH are also a source only USB Type-C controllers which are optimized for mobile chargers and power adapters. It supports standard 3 A VBUS current level. N-Channel MOSFET is compatible as a load switch, and helps to reduce BOM cost.

The internal two operational amplifiers control adaptive constant output voltage and adaptive constant output current. The outputs of the two amplifiers are tied together in open-drain configuration.

FAN6291QF/FAN6291QH enables adaptor output voltage and current adjustment when Quick Charge 3.0 protocol is acknowledged. According to request from a battery charger of a Portable Device, output voltage is adjusted up to 12 V. When a portable device that implements non-compliant protocols is attached, it just maintains the default output, (5 V) for safety of the portable device.

FAN6291QF/FAN6291QH incorporates adaptive output over-voltage and under-voltage protections to improve system reliability.

Features

- Compatible with Quick Charge 3.0 (QC3.0) Protocol
- Auto-detection supporting 2.4 A Apple products
- Type-C Control for Standard 3 A VBUS Current
- N-Channel MOSFET Control as a Type-C Load Switch
- Internal Synchronous Rectifier Control Circuit
- Secondary-Side Constant Voltage (CV) and Constant Current (CC) Regulation with Two Operational Amplifiers
- Small Current Sensing Resistor (30 mΩ) for High Efficiency
- Protections for Safe Operation ; Output Over-Voltage-Protection, Output Under-Voltage-Protection for QC2.0, Data line (D+/D-) Over-Voltage-Protection
- Built-in output capacitor bleeding function for fast discharging during change of output mode
- Built-in Cable-Drop Compensation

Typical Applications

- Battery Chargers for Smart Phones, Feature Phones, and Tablet PCs
- AC-DC Adapters for Portable Devices that Require CV/CC Control

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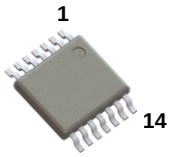
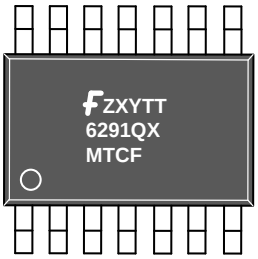


TSSOP-14

MARKING DIAGRAM

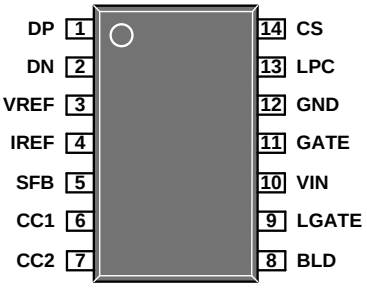


1st Line:
F: Corporate Logo
Z: Assembly Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code

2nd Line:
6291Q: IC Part Name
X: Series Line-up Name

3rd Line: MTCF

PIN CONNECTIONS



(TOP View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

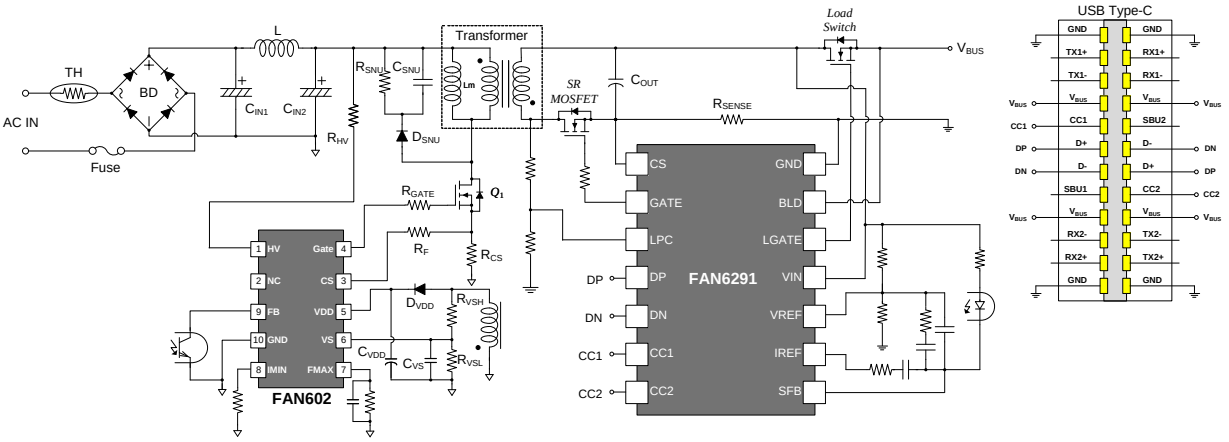


Figure 1 FAN6291QF and FAN6291QH Typical Application Schematic

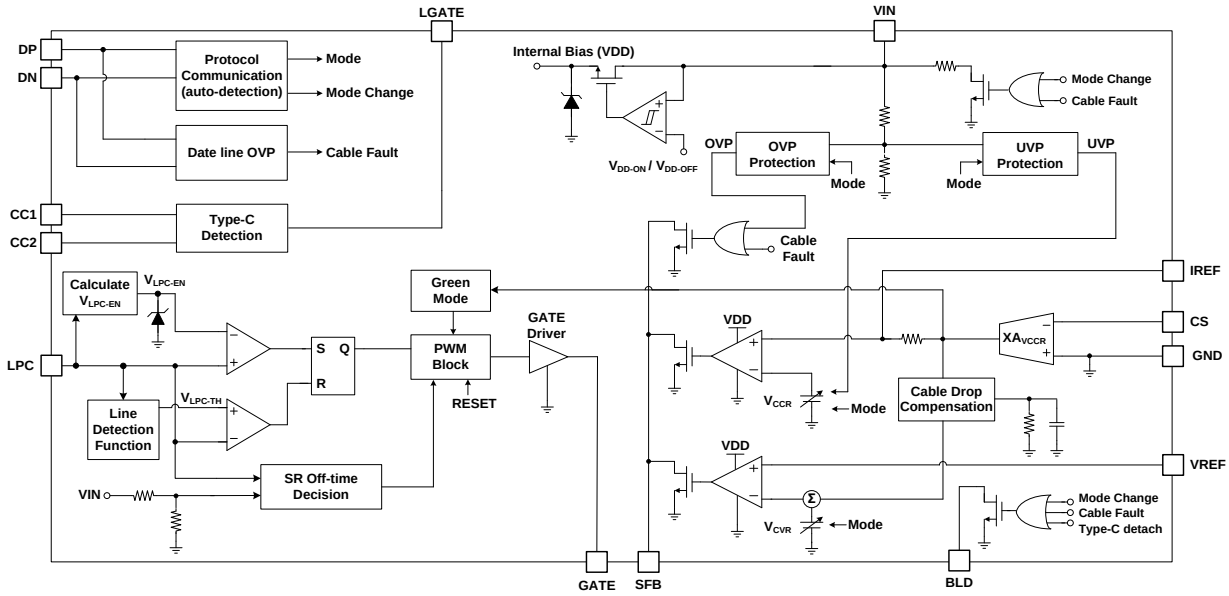


Figure 2. FAN6291QF and FAN6291QH Function Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	DP	Communication Interface Positive Terminal. This pin is tied to the USB D+ data line input.
2	DN	Communication Interface Negative Terminal. This pin is tied to the USB D- data line input.
3	VREF	Output Voltage Sensing Terminal. Non-inverting terminal of the internal CV loop amplifier. This pin is used for constant voltage regulation.
4	IREF	Constant Current Amplifying Signal. The voltage on this pin represents the amplified current sense signal, also used for constant current regulation. It is tied to the internal CC loop amplifier's non-inverting terminal.
5	SFB	Secondary Feedback. Common output of the open-drain operation amplifiers. Typically an opto-coupler is connected to this pin to provide feedback signal to the primary-side PWM controller.
6	CC1	Configuration Channel 1. This pin is used to detect connections of Type-C cables and connectors. It is tied to the USB Type-C CC1.
7	CC2	Configuration Channel 2. This pin is used to detect connections of Type-C cables and connectors. It is tied to the USB Type-C CC2.
8	BLD	Bleeder. This pin is tied to the VBUS pin of type-C connector to discharge an output capacitor.
9	LGATE	Load Switch Gate. This pin is tied to the gate of the load switch
10	VIN	Input Voltage. This pin is tied to the output of the adaptor not only to monitor output voltage but also to supply internal bias. IC operating current, and MOSFET gate-drive current are supplied through this pin.
11	GATE	Gate Drive Output. Totem-pole output to drive an external SR MOSFET.
12	GND	Ground.
13	LPC	SR MOSFET Drain Voltage Detection. This pin detects the voltage on the secondary winding for Synchronous Rectifier control.
14	CS	Current Sensing Amplifier Negative Terminal. Output current is sensed through this terminal for green mode control, cable drop compensation, and constant current control.

Series Line-up Table

Name	Output Voltage and its Nominal Output Current			UVP Operation
	V_O = 3.6 ~ 6 V	V_O = 6.2 ~ 9 V	V_O = 9.2 ~ 12 V	
FAN6291QF	3.0 A	2.0 A	1.5 A	Pull-down SFB
FAN6291QH	3.0 A	3.0 A	2.0 A	Reduce CC

MAXIMUM RATINGS (Note 1,2,3)

Rating	Symbol	Value	Unit
VIN Pin Input Voltage	V_{IN}	20	V
SFB Pin Input Voltage	V_{SFB}	20	V
BLD Pin Input Voltage	V_{BLD}	20	V
LGATE Pin Input Voltage	V_{LGATE}	20	V
CC1 Pin Input Voltage	V_{CC1}	-0.3 to 6	V
CC2 Pin Input Voltage	V_{CC2}	-0.3 to 6	V
IREF Pin Input Voltage	V_{IREF}	-0.3 to 6	V
VREF Pin Input Voltage	V_{VREF}	-0.3 to 6	V
CS Pin Input Voltage	V_{CS}	-0.3 to 6	V
DP Pin Input Voltage	V_{DP}	-0.3 to 14	V
DN Pin Input Voltage	V_{DN}	-0.3 to 14	V
LPC Pin Input Voltage	V_{LPC}	-0.3 to 6.5	V
GATE Pin Input Voltage	V_{GATE}	-0.3 to 6	V
Power Dissipation (T_A=25°C)	P_D	0.62	W
Operating Junction Temperature	T_J	-40 to 150	°C
Storage Temperature Range	T_{STG}	-40 to 150	°C
Lead Temperature, (Soldering, 10 Seconds)	T_L	260	°C
Human Body Model, ANSI/ESDA/JEDEC JS-001-2012 (Note 4)	ESD_{HBM}	3	kV
Charged Device Model, JESD22-C101 (Note 4)	ESD_{CDM}	1.75	kV

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. All voltage values, except differential voltages, are given with respect to the GND pin.
3. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
4. Meets JEDEC standards JS-001-2012 and JESD 22-C101.

THERMAL CHARACTERISTICS (Note 5)

Rating	Symbol	Value	Unit
Thermal Characteristics, Thermal Resistance, Junction-to-Air Thermal Reference, Junction-to-Top	 $R_{\theta JA}$ $R_{\psi JT}$	 162 16.5	°C/W

5. T_A=25°C unless otherwise specified.

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol	Min	Max	Unit
VIN Pin Input Voltage	V_{IN}	0	16	V
SFB Pin Input Voltage	V_{SFB}	0	16	V
BLD Pin Input Voltage	V_{BLD}	0	16	V
LGATE Pin Input Voltage	V_{LGATE}	0	19.5	V
CC1 Pin Input Voltage	V_{CC1}	0	5.8	V
CC2 Pin Input Voltage	V_{CC2}	0	5.8	V
IREF Pin Input Voltage	V_{IREF}	0	1	V
VREF Pin Input Voltage	V_{VREF}	0	3.5	V
CS Pin Input Voltage	V_{CS}	-0.1	0	V
DP Pin Input Voltage	V_{DP}	0	6	V
DN Pin Input Voltage	V_{DN}	0	6	V
LPC Pin Input Voltage	V_{LPC}	0	5	V
GATE Pin input Voltage	V_{GATE}	0	5.5	V

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN}=5 V, LPC=1.5 V, LPC width=2 μs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VIN Section						
Continuous Operating Voltage[7]		V_{IN-OP}			16	V
Operating Supply Current	V_{IN}=5 V, V_{CS}= -60 mV	$I_{IN-OP-5V}$		8		mA
Operating Supply Current	V_{IN}=12 V, V_{CS}= -60 mV	$I_{IN-OP-12V}$		8		mA
5 V Green Mode Operating Supply Current	V_{IN}=5 V, V_{CS}=0 mV	$I_{IN-Green}$		1.2	1.6	mA
VIN-UVP Section						
Voltage difference between GND and CS for fixed UVP current ($I_{O-UVP.typ}$=217 mA)	Only for FAN6291QH	V_{CS-UVP}	3.0	6.5	10.0	mV
V_{IN} Under-Voltage-Protection Enable, 9 V	For QC2.0 9 V Mode	$V_{IN-UVP-L-9V}$	5.00	5.50	6.00	V
V_{IN} Under-Voltage-Protection Enable, 12 V	For QC2.0 12 V Mode	$V_{IN-UVP-L-12V}$	7.50	8.00	8.50	V
V_{IN} Under-Voltage-Protection Disable, 9 V	For QC2.0 9 V Mode	$V_{IN-UVP-H-9V}$	5.50	6.00	6.50	V
V_{IN} Under-Voltage-Protection Disable, 12 V	For QC2.0 12 V Mode	$V_{IN-UVP-H-12V}$	8.00	8.50	9.00	V
CC Mode UVP Debounce Time		$t_{D-VIN-UVP}$	45	60	75	ms
VIN-OVP Section						
Output Over-Voltage Protection through V_{IN} Pin at V_O=3.6 ~ 5 V		$V_{IN-OVP-5V}$	5.5	6.0	6.5	V
Output Over-Voltage Protection through V_{IN} Pin at V_O=5.2 ~ 6 V		$V_{IN-OVP-6V}$	8.1	8.4	8.7	V
Output Over-Voltage Protection through V_{IN} Pin at V_O=6.2 ~ 9 V		$V_{IN-OVP-9V}$	10.3	10.8	11.3	V
Output Over-Voltage Protection through V_{IN} Pin at V_O=9.2 ~ 12 V		$V_{IN-OVP-12V}$	13.6	14.4	15.0	V
OVP Debounce Time		t_{D-OVP}	22	33	44	μs
Internal Bias Section						
Turn-On Threshold Voltage	V_{IN} Increases	V_{IN-ON}	2.9	3.2	3.4	V
Turn-Off Threshold Voltage	V_{IN} Decreases after V_{IN}=V_{IN-ON}	V_{IN-OFF}	2.8	2.9	3.0	V
Hysteresis of Turn-Off Threshold Voltage	V_{IN} Decreases after V_{IN}=V_{IN-ON}	$V_{IN-OFF-HYS}$		0.3		V
Turn-On Debounce Time		$t_{VIN-on-debounce}$			50	μs
Turn-Off Debounce Time		$t_{VIN-off-debounce}$			200	μs
Output Voltage Releasing Latch Mode[8]		$V_{LATCH-OFF}$	1.5	2.0	2.5	V
Constant Current Sensing Section						
Current-Sense Amplifier Gain[7]	V_{IN}=5 V, V_{CS}= -60 mV	A_{V-CCR}		10		V/V
Voltage difference between GND and CS at $I_{O-NOMINAL}$=3.0 A of FAN6291QF[8]	I_O=3.0~3.4 A, I_{OTYP}=3.2 A (3 mV Offset)	$V_{CS-3.0A-QF}$	90.0	93.0	96.0	mV
Voltage difference between GND and CS at $I_{O-NOMINAL}$=2.0 A of FAN6291QF [8]	I_O=2.0~2.3 A, I_{OTYP}=2.15 A (3 mV Offset)	$V_{CS-2.0A-QF}$	59.5	62.0	64.5	mV
Voltage difference between GND and CS at $I_{O-NOMINAL}$=1.5 A of FAN6291QF[8]	I_O=1.5~1.8 A, I_{OTYP}=1.65 A (3 mV Offset)	$V_{CS-1.5A-QF}$	43.5	46.0	48.5	mV
Voltage difference between GND and CS at $I_{O-NOMINAL}$=3.0 A of FAN6291QH[8]	I_O=3.0~3.4 A, I_{OTYP}=3.2 A (3 mV Offset)	$V_{CS-3.0A-QH}$	90.0	93.0	96.0	mV
Voltage difference between GND and CS at $I_{O-NOMINAL}$=2.0 A of FAN6291QH[8]	I_O=2.0~2.4 A, I_{OTYP}=2.2 A (3 mV Offset)	$V_{CS-2.0A-QH}$	62.5	65.0	67.5	mV
Current-Sensing Input Impedance[8]		Z_{CS}	4			MΩ
Voltage difference between GND and CS for Green Mode	R_{CS}=30 mΩ	$V_{CS-Green}$	2	5	8	mV

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN}=5 V, LPC=1.5 V, LPC width=2 μs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Constant Current Sensing Section (continued)						
Voltage difference between GND and CS for Green Mode	Only for under 4.8 V Mode of QC3.0, R_{CS}=30 mΩ	$V_{CS\text{-}Green\text{-}LowQC3.0}$	34	39	44	mV
Green Mode Enable Debounce Time	After V_{CS}<$V_{CS\text{-}Green}$	$T_{Green\text{-}EN\text{-}Debounce}$			100	μs
Green Mode Disable Debounce Time	After V_{CS}>$V_{CS\text{-}Green}$	$T_{Green\text{-}DIS\text{-}Debounce}$	8	12	16	ms
Constant Voltage Sensing Section						
Reference Voltage at 5 V	V_{IN}=5 V, V_{CS}=0 V, V_{DP}=0.6 V, V_{DN}=0 V	$V_{CVR\text{-}5V}$	0.98	1.00	1.02	V
Reference Voltage at 9 V	V_{IN}=9 V, V_{CS}=0 V, V_{DP}=0.6 V, V_{DN}=0 V	$V_{CVR\text{-}9V}$	1.76	1.80	1.84	V
Reference Voltage at 12 V	V_{IN}=12 V, V_{CS}=0 V, V_{DP}=0.6 V, V_{DN}=0 V	$V_{CVR\text{-}12V}$	2.335	2.400	2.465	V
Reference Voltage of Increment Step via continuous Mode of QC3.0 Protocol	V_{IN}=12 V, V_{CS}=0 V, V_{DP}=0.6 V, V_{DN}=3.3 V	$V_{CVR\text{-}STEP\text{-}INC}$	35	40	45	mV
Reference Voltage of Decrement Step via Continuous Mode of QC3.0 Protocol	V_{IN}=12 V, V_{CS}=0 V, V_{DP}=0.6 V, V_{DN}=3.3 V	$V_{CVR\text{-}STEP\text{-}DEC}$	35	40	45	mV
Reference Voltage Soft-drop Time[7]	During Mode change from V_{IN} to Low V_{IN}	$t_{CVR\text{-}Soft\text{-}drop}$		40		ms
Cable Drop Compensation Section						
Cable Compensation Voltage[8]	V_{CS}=-60 mV	$V_{COMR\text{-}CDC}$	64.5	68.0	71.5	mV
OVP Cable Compensation Voltage[8]	V_{CS}=-60 mV	$V_{COMR\text{-}OVP}$	360	510	660	mV
Constant Current Amplifier Section						
Disable Constant Current Amplifier Time during Startup	After V_{IN}>$V_{IN\text{-}ON}$	$t_{Start\text{-}Dis\text{-}CC}$	1.3	2.5	6.0	ms
Internal Amplifier Transconductance[7]		Gm_{CC}		3.5		ʊ
Internal Amplifier Dominant Pole[7]		$f_{P\text{-}CC}$		10		kHz
Internal CC Amplifier Input Resistor		$R_{CC\text{-}IN}$	8.50	13.75	19.00	kΩ
Constant Voltage Amplifier Section						
Internal Amplifier Dominant Pole[7]		$f_{P\text{-}CV}$		10		kHz
CV Bias Current[7]		$I_{Bias\text{-}CV}$			30	nA
Bleeder Section						
Voltage difference between GND and CS to enable BLD ($I_{O\text{-}EN\text{-}BLD.typ}$=0.42 A)	Decreasing V_{CS}, R_{CS}=30 mΩ	$V_{CS\text{-}EN\text{-}BLD}$	8	12	16	mV
Debounce time to decide enable BLD	Decreasing V_{CS}, R_{CS}=30 mΩ	$t_{CS\text{-}EN\text{-}BLD}$		0.6	1.0	ms
VIN Pin Sink Current through when Bleeding[7]	V_{IN}=9 V	$I_{VIN\ -Sink}$	200			mA
BLD Pin Sink Current through when Bleeding[7]	V_{IN}=9 V	$I_{BLD\ -Sink}$	150			mA
VIN Pin and BLD Pin Internal MOSFET parasitical resistor[7]		$R_{DS\_on\_BLD}$			40	Ω
Maximum Discharging Time when Bleeding	Disabling OVP & SR Gate	$t_{BLD\text{-}MAX}$	275	320	365	ms
Feedback Section						
Feedback Pin Maximum Sink Current		$I_{SFB\text{-}Sink\text{-}MAX}$	2			mA

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN}=5 V, LPC=1.5 V, LPC width=2 μs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Protocol Section_Quick Charge 2.0 Interface						
DP Low Threshold Voltage		V_{DPL}	0.24	0.25	0.28	V
DP High Threshold Voltage		V_{DPH}	1.95	2.05	2.15	V
DN Low Threshold Voltage		V_{DNL}	0.30	0.35	0.40	V
DN High Threshold Voltage		V_{DNH}	1.95	2.05	2.15	V
DP and DN High Debounce Time		$t_{BC1.2}$	1.0	1.2	1.4	s
DP Disconnect Debounce Time		$t_{DISCONNECT}$	5	10	15	ms
DN Low Debounce Time, VDN < VDNL		t_{TOGGLE}			1.0	ms
Mode-Change Debounce Time		t_{V_CHANGE}	20	40	60	ms
Blanking Time after Mode Change		$t_{V\_REQUEST}$	60		100	ms
DP Pull Low Resistance		R_{DP}	300	1120	1500	kΩ
DN Pull Low Resistance		R_{DN}	14.25	19.53	24.80	kΩ
Protocol Section_Quick Charge 3.0 Interface						
Mode-Change Debounce Time	V_{DP}=0.6, V_{DN}=3.3 V	t_{V_CHANGE}	20	40	60	ms
Mode-Change Debounce Time for Continuous Mode	For T_{ACTIVE} and $T_{INACTIVE}$	t_{CONT_CHANGE}	100	150	200	μs
VIN Voltage Range for Continuous Mode[7]		$V_{IN\_CONT\_RANGE}$	3.6		12	V

Table 1. Quick Charge 3.0 & 2.0 Output Modes

Mode	V_{DP} (Typ.)	V_{DN} (Typ.)	V_{OUT}
Mode 1	0.6 V	0 V	5 V
Mode 2	3.3 V	0.6 V	9 V
Mode 3	0.6 V	0.6 V	12 V
Mode 4	0.6 V	3.3 V	Continuous Mode
Mode 5	3.3 V	3.3 V	Reserved

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN}=5 V, LPC=1.5 V, LPC width=2 μs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Type-C Section						
Source Current on CC1 Pin	V_{IN}=5 V, V_{CC2}=0 V	I_{P-CC1}	304	330	356	μA
Source Current on CC2 Pin	V_{IN}=5 V, V_{CC1}=0 V	I_{P-CC2}	304	330	356	μA
Input Impedance on CC1 Pin		$Z_{OPEN-CC1}$	126			kΩ
Input Impedance on CC2 Pin		$Z_{OPEN-CC1}$	126			kΩ
Ra Impedance Detection Threshold on CC1 Pin	V_{IN}=5 V, V_{CC2}=0 V, Decreasing V_{CC1}	V_{RA-CC1}	0.75	0.80	0.85	V
Ra Impedance Detection Threshold on CC2 Pin	V_{IN}=5 V, V_{CC1}=0 V, Decreasing V_{CC2}	V_{RA-CC2}	0.75	0.80	0.85	V
Rd Impedance Detection Threshold on CC1 Pin	V_{IN}=5 V, V_{CC2}=0 V, Increasing V_{CC1}	V_{RD-CC1}	2.45	2.60	2.75	V
Rd Impedance Detection Threshold on CC2 Pin	V_{IN}=5 V, V_{CC1}=0 V, Increasing V_{CC2}	V_{RD-CC2}	2.45	2.60	2.75	V
UFP Attachment Debounce Time	V_{IN}=5 V, V_{CC2}=0 V, Increasing V_{CC1}	$t_{CC-Attach-debounce}$	150	200	250	ms
UFP Detachment Debounce Time	V_{IN}=5 V, V_{CC2}=0 V, Decreasing V_{CC1}	$t_{CC-Detach-debounce}$	10	15	20	ms
Gate High Voltage at 5.5 V	V_{IN}=5.5 V	$V_{NGATE-5.5V}$	9.0			V
Gate High Voltage at 9 V	V_{IN}=9 V	$V_{NGATE-9V}$	12.5			V
Gate High Voltage at 12 V	V_{IN}=12 V	$V_{NGATE-12V}$	15.5			V
Protocol Section_Auto Detection						
Default DP Voltage when Floating	2.75 V Supply Mode	$V_{DP\_2.75V}$	2.65	2.75	2.85	V
Default DN Voltage when Floating	2.75 V Supply Mode	$V_{DN\_2.75V}$	2.65	2.75	2.85	V
DP Pin Output Impedance in Default Mode	2.75 V Supply Mode	$R_{DP\_2.75V}$	23	28	33	kΩ
DN Pin Output Impedance in Default Mode	2.75 V Supply Mode	$R_{DN\_2.75V}$	23	28	33	kΩ
Increment of VDP for exiting 2.75 V Supply Mode	Increment from $V_{DP\_2.75V}$	V_{DP_INC}	115	170	225	mV
Debounce Time for exiting 2.75 V Supply Mode		t_{EXIT_MODE1}	3	4	5	ms
Delay Time to recover to 2.75 V Supply Mode	V_{DP}< V_{DPL} in BC1.2 Mode	t_{REC_MODE1}	3	4	5	sec
Output Driver Section						
Output Voltage Low	V_{IN}=5 V, I_{GATE}=100 mA	V_{OL}		0.16	0.25	V
Output Voltage High	V_{IN}=5 V	V_{OH}	4.5			V
Rising Time[7]	V_{IN}=5 V, C_L=3300 pF, GATE=1 V ~ 4 V	t_R		20	35	ns
Falling Time[7]	V_{IN}=5 V, C_L=3300 pF, GATE=4 V~ 1 V	t_F		9		ns
Propagation Delay to OUT High (LPC Trigger)	V_{IN}=5 V, GATE=1 V	$t_{PD-HIGH-LPC}$		44	80	ns
Propagation Delay to OUT Low (LPC Trigger)[7]	V_{IN}=5 V, GATE=4 V	$t_{PD-LOW-LPC}$		30		ns
Gate Inhibit Time[7]		$t_{INHIBIT}$		1.4		μs

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN}=5 V, LPC=1.5 V, LPC width=2 μs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Internal RES Section						
Internal RES Ratio[7]	V_{IN}=5~12 V	K_{RES}		0.150		V/V
VIN Dropping Protection Ratio with Two Cycle	LPC Width=5 μs, V_{IN}=5 V to 3.5 V	$K_{VIN-DROP}$	70		90	%
Debounce Time for Disable SR when VIN Dropping Protection		t_{SR_OFF}	3.8	5.5	7.2	ms
LPC Section						
Linear Operation Range of LPC Pin Voltage[7]	$V_{IN\ -OFF}$ < V_{IN} ≤ 5 V	V_{LPC}	0.5		V_{IN} -1	V
LPC Sink Current	V_{LPC}=1 V	$I_{LPC-SINK}$		100		nA
SR Enabled Threshold Voltage @High-Line		$V_{LPC-HIGH-H}$			1.58	V
Threshold Voltage on LPC Rising Edge @High-Line[7]	$V_{LPC-HIGH-H}$ *0.875=$V_{LPC-TH-H}$	$V_{LPC-TH-H}$		1.31		V
SR Enabled Threshold Voltage @ Low-Line	$V_{LPC-HIGH-L-5.5V}$=$V_{LPC-TH-L-5.5V}$ / 0.875	$V_{LPC-HIGH-L-5.5V}$			0.86	V
Threshold Voltage on LPC Rising Edge @ Low-Line[7]	Spec.=0.45+0.05*V_{IN}, V_{IN}=5.5 V	$V_{LPC-TH-L-5.5V}$		0.725		V
SR Enabled Threshold Voltage @ Low-Line	$V_{LPC-HIGH-L-9V}$=$V_{LPC-TH-L-9V}$ / 0.875	$V_{LPC-HIGH-L-9V}$			1.06	V
Threshold Voltage on LPC Rising Edge @ Low-Line[7]	Spec.=0.45+0.05*V_{IN}, V_{IN}=9 V	$V_{LPC-TH-L-9V}$		0.90		V
SR Enabled Threshold Voltage @ Low-Line	$V_{LPC-HIGH-L-12V}$=$V_{LPC-TH-L-12V}$ / 0.875	$V_{LPC-HIGH-L-12V}$			1.23	V
Threshold Voltage on LPC Rising Edge @ Low-Line[7]	Spec.=0.45+0.05*V_{IN}, V_{IN}=12 V	$V_{LPC-TH-L-12V}$		1.05		V
Falling Edge Threshold Voltage to Trigger SR[7]		$V_{LPC-TH-TRIG}$		70		mV
Low-to-High Line Threshold Voltage on LPC Pin	V_{IN}=5.5 V	$V_{LINE-H-5.5V}$	1.84	1.93	2.02	V
High-to-Low Line Threshold Voltage on LPC Pin	V_{IN}=5.5 V	$V_{LINE-L-5.5V}$	1.75	1.83	1.91	V
Line Change Threshold Hysteresis	$V_{LINE-HYS-5.5V}$=$V_{LINE-H-5.5V}$ - $V_{LINE-L-5.5V}$	$V_{LINE-HYS-5.5V}$		0.1		V
Low-to-High Line Threshold Voltage on LPC Pin	V_{IN}=9 V	$V_{LINE-H-9V}$	2.05	2.14	2.23	V
High-to-Low Line Threshold Voltage on LPC Pin	V_{IN}=9 V	$V_{LINE-L-9V}$	1.96	2.04	2.12	V
Line Change Threshold Hysteresis	$V_{LINE-HYS-9V}$=$V_{LINE-H-9V}$ - $V_{LINE-L-9V}$	$V_{LINE-HYS-9V}$		0.1		V
Low -to-High Line Threshold Voltage on LPC Pin	V_{IN}=12 V	$V_{LINE-H-12V}$	2.23	2.32	2.41	V
High-to-Low Line Threshold Voltage on LPC Pin	V_{IN}=12 V	$V_{LINE-L-12V}$	2.14	2.22	2.30	V
Line Change Threshold Hysteresis	$V_{LINE-HYS-12V}$=$V_{LINE-H-12V}$ - $V_{LINE-L-12V}$	$V_{LINE-HYS-12V}$		0.1		V
Higher Clamp Voltage		$V_{LPC-CLAMP-H}$	5.4	6.2	7.0	V
LPC Threshold Voltage to Disable SR Gate Switching	V_{IN}=5 V. LPC=3 V↑	$V_{LPC-DIS}$	V_{IN} - 0.6			V
Enable $V_{LPC-DIS}$	Increasing V_{IN}	$V_{EN-LPC-DIS}$	4.30	4.45	4.60	V
Disable $V_{LPC-DIS}$	Decreasing V_{IN}	$V_{DIS-LPC-DIS}$	4.10	4.25	4.40	V
Line Change Debounce from Low-Line to High-Line		$t_{LPC-LH-debounce}$	15	23	31	ms
Line Change Debounce from High-Line to Low-Line[7]		$t_{LPC-HL-debounce}$		15		μs

ELECTRICAL CHARACTERISTICS (CONTINUED)

V_{IN}=5 V, LPC=1.5 V, LPC width=2 μs at T_J= -40~125 °C, F_{LPC}=100 kHz, unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Internal Timing Section						
Ratio between V_{LPC} & V_{RES}	V_{IN}=5.5 V, F_{LPC}=50 kHz, K_{RES}=0.15	$Ratio_{LPC-RES}$	3.88	4.09	4.30	
Minimum LPC Time to Enable the SR Gate @ High-Line	V_{LPC}=3 V	$t_{LPC-EN-H}$	150	250	350	ns
Minimum LPC Time to Enable the SR Gate @ Low-Line	V_{LPC}=1.5 V	$t_{LPC-EN-L}$	520	620	720	ns
Minimum Gate Width(7)		t_{MIN}	0.35	0.50	0.65	μs
Minimum Gate Limit On-time		$t_{gate-limit-min}$	0.6	1.0	1.4	μs
$t_{on-SR}(n+1)- t_{on-SR}(n) < t_{gate-limit}$		$t_{gate-limit}$		500		ns
Limitation between LPC Rising Edge to next LPC Rising Edge Max. Period		$t_{MAX-PERIOD}$	28	40	52	μs
Forced internal CT Reset Time(7)		$t_{CT-RESET}$		10		ns
Reverse Current Mode Section						
Reverse Current Mode Entry Debounce Time	V_{IN}=5 V, V_{LPC}=0 V	$T_{reverse-debounce}$	350	500	650	ms
Operating Current during Reverse Current Mode	V_{IN}=5 V, V_{LPC}=0 V	$I_{OP.reverse}$			1.7	mA
Source Current on CC1 Pin during Reverse Current Mode	V_{IN}=5 V, V_{LPC}=0 V	$I_{P-CC1.reverse}$			10	μA
Source Current on CC2 Pin during Reverse Current Mode	V_{IN}=5 V, V_{LPC}=0 V	$I_{P-CC2.reverse}$			10	μA
AUX Pin Current during Reverse Current Mode	V_{IN}=5 V, V_{LPC}=0 V, After $t_{BLD-MAX}$	$I_{BLD.reverse}$			10	μA
Data line Over-Votlage Protection						
DP Pin Over-Voltage Protection	Excepting 2.75 V Supply Mode	V_{DP-OVP}	4.10	4.35	4.60	V
DN Pin Over-Voltage Protection	Excepting 2.75 V Supply Mode	V_{DN-OVP}	4.10	4.35	4.60	V
DP/DN Pin OVP Debounce Time	$V_{DN} > V_{DN-SD}$	$t_{DN-DP-OVP-Debounce}$	1.5	3.0	4.5	ms

7. Guaranteed by Design.
8. Guaranteed at -5° ~ 85°C.

TYPICAL CHARACTERISTICS

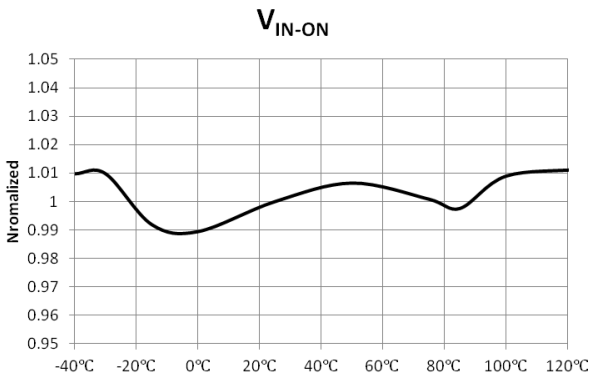


Figure 3 Turn-On Threshold Voltage (V_{IN-ON}) vs. Temperature

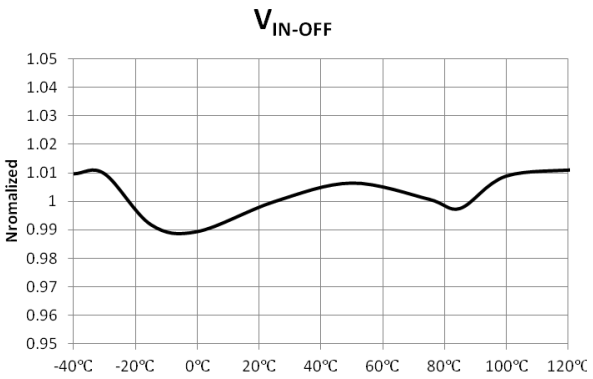


Figure 4 Turn-Off Threshold Voltage (V_{IN-OFF}) vs. Temperature

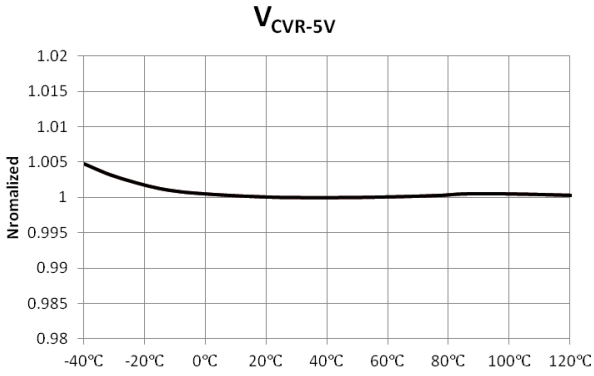


Figure 5 Reference Voltage at 5 V (V_{CVR-5V}) vs. Temperature

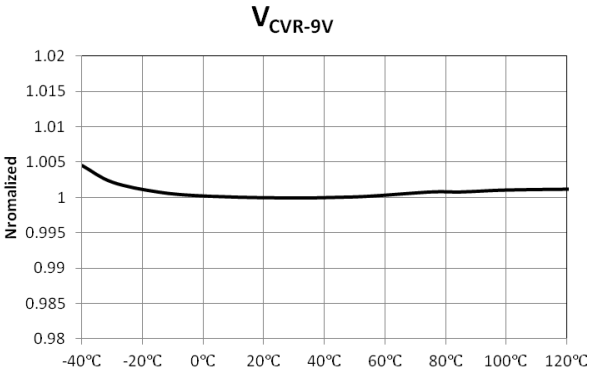


Figure 6 Reference Voltage at 9 V (V_{CVR-9V}) vs. Temperature

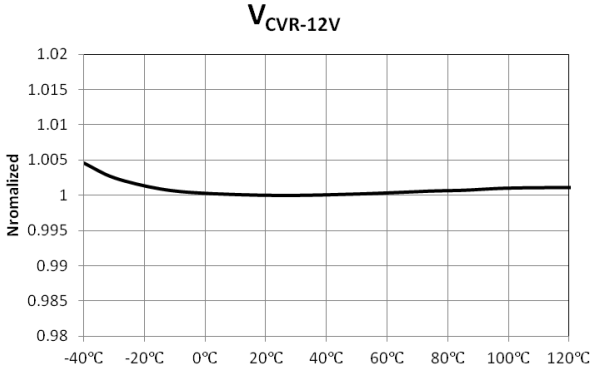


Figure 7 Reference Voltage at 12 V ($V_{CVR-12V}$) vs. Temperature

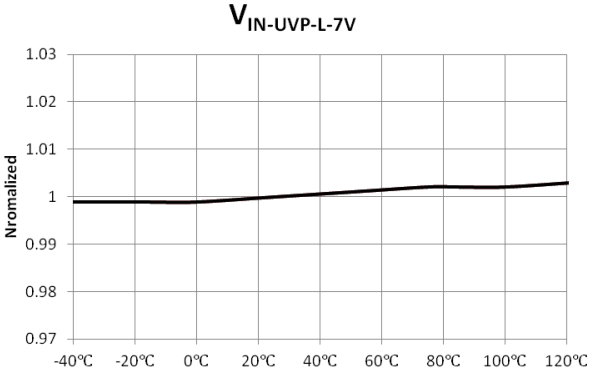


Figure 8 V_{IN} Under-Voltage-Protection Enable, 7 V ($V_{IN-UVP-L-7V}$) vs. Temperature

TYPICAL CHARACTERISTICS

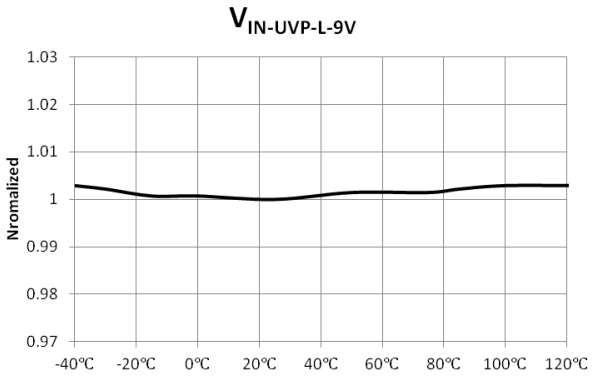


Figure 9 V_{IN} Under-Voltage-Protection Enable, 9 V ($V_{IN-UVP-L-9V}$) vs. Temperature

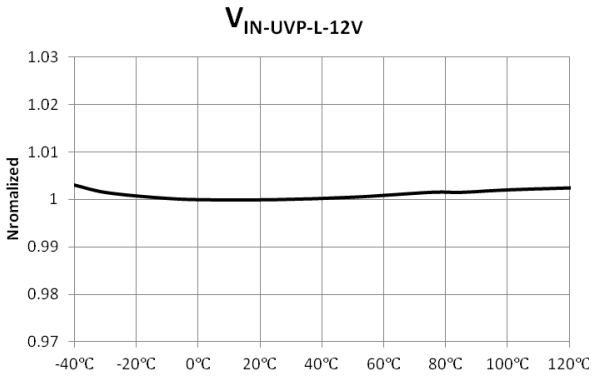


Figure 10 V_{IN} Under-Voltage-Protection Enable, 12 V ($V_{IN-UVP-L-12V}$) vs. Temperature

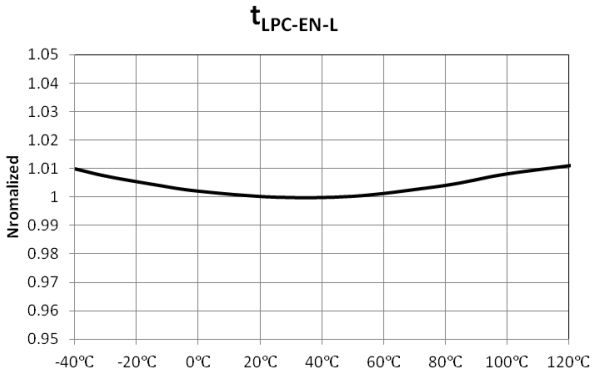


Figure 11 Minimum LPC Time to Enable the SR Gate @ Low-Line ($t_{LPC-EN-L}$) vs. Temperature

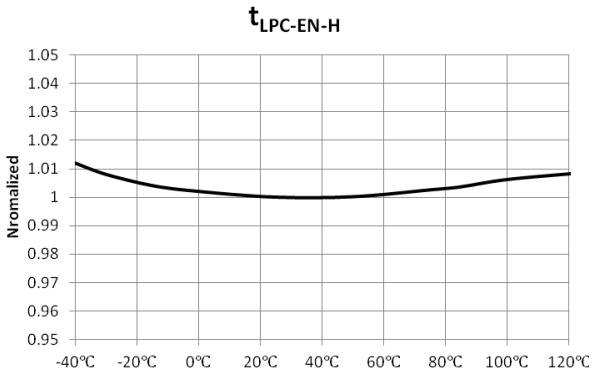


Figure 12 Minimum LPC Time to Enable the SR Gate @ High-Line ($t_{LPC-EN-H}$) vs. Temperature

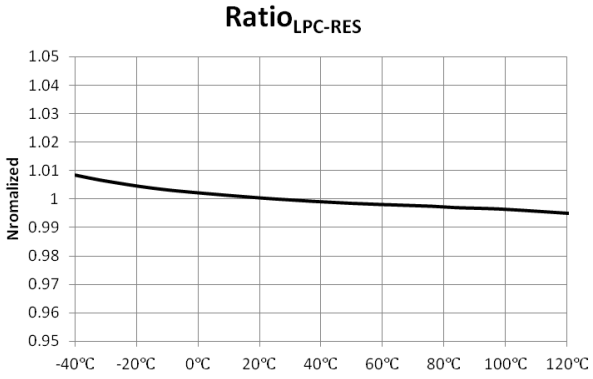


Figure 13 Ratio between V_{LPC} & V_{RES} ($Ratio_{LPC-RES}$) vs. Temperature

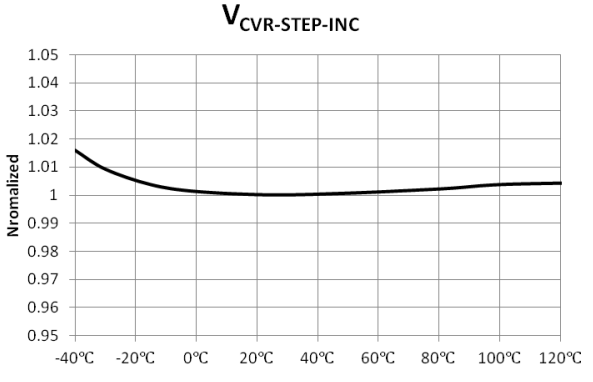


Figure 14 Reference Voltage of Increment Step via Continuous Mode of QC3.0 Protocol ($V_{CVR-STEP-INC}$) vs. Temperature

TYPICAL CHARACTERISTICS

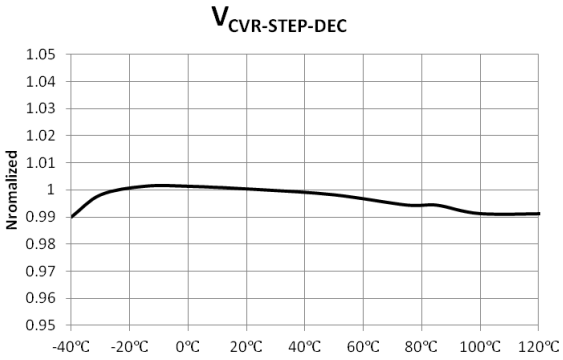


Figure 15 Reference Voltage of Decrement Step via Continuous Mode of QC3.0 Protocol ($V_{CVR-STEP-DEC}$) vs. Temperature

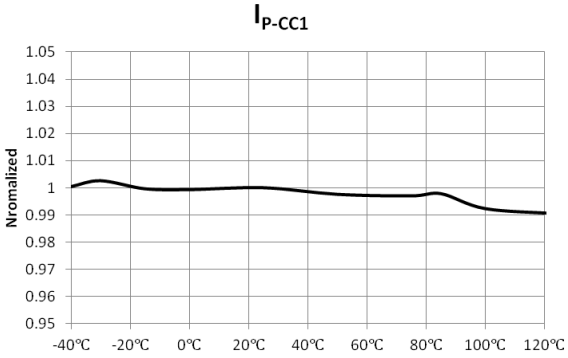


Figure 16 Source Current on CC1 Pin (I_{P-CC1}) vs. Temperature

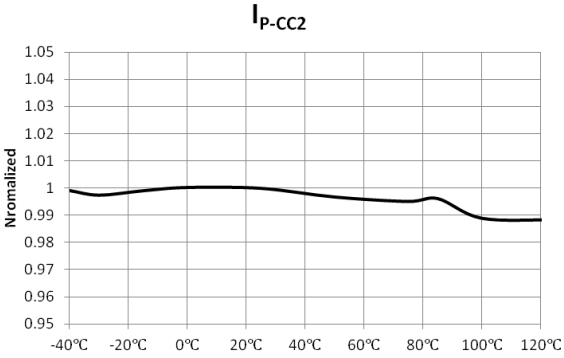


Figure 17 Source Current on CC2 Pin (I_{P-CC2}) vs. Temperature

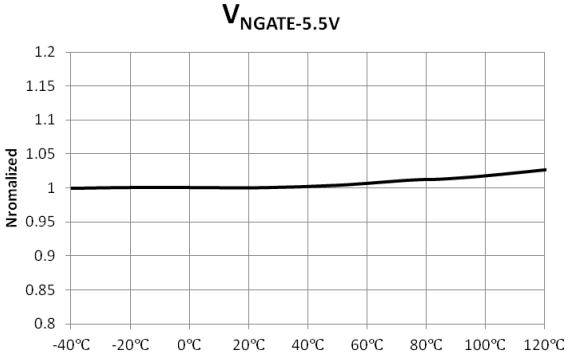


Figure 18 Gate High Voltage at 5.5 V ($V_{NGATE-5.5V}$) vs. Temperature

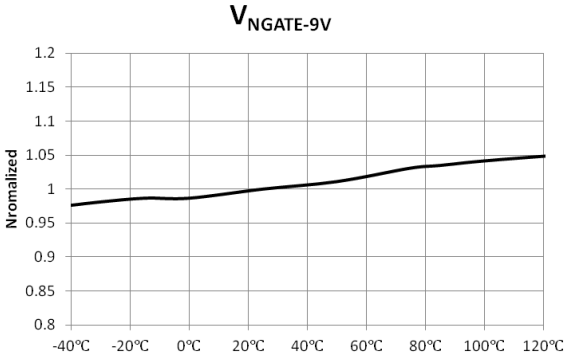


Figure 19 Gate High Voltage at 9 V ($V_{NGATE-9V}$) vs. Temperature

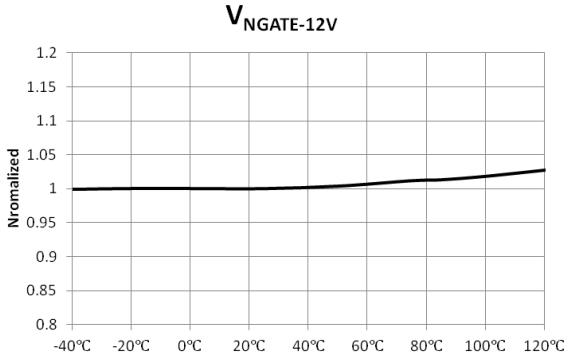


Figure 20 Gate High Voltage at 12 V ($V_{NGATE-12V}$) vs. Temperature

Table 2. Device Line-up Table

Series Name	Output Voltage and its Nominal Output Load			UVP Operation
	3.6~6.0 V	6.2~9.0 V	9.2~12.0 V	
FAN6291QF	3.0 A	2.0 A	1.5 A	Pull-down SFB
FAN6291QH	3.0 A	3.0 A	2.0 A	Reduce CC

FAN6291QF and FAN6291QH implement different operation methods when the UVP is triggered. FAN6291QH reduces constant current level after triggering UVP. When a foldback level is performed on the system, resistive load is normally used. Since this reduced constant current is lower than the resistive load in the UVP, the output voltage is collapsed and foldback can be achieved. FAN6291QF pulls-down SFB pin after UVP is triggered. It then enters Latch Mode Operation (Refer to Figure 28 and Figure 29). According to Latch Mode Operation, the output voltage is collapsed and foldback can be achieved.

Type-C Control Function Description

N-channel MOSFET for Load Switch

FAN6291Q implements Type-C block to enable and disable an external load switch. Internally adapted charge pump lets FAN6291Q control N-channel MOSFET as a load switch. It helps whole system be more cost competitive compared to P-channel MOSFET as a load switch. Since the minimum pumped voltage is V_{BUS}+3 V, it is recommended to use N-channel MOSFET supporting lower gate threshold levels.

Detail of Load Switch Control

FAN6291Q supports output current higher than 1.5 A. In order to meet Type-C specification, 330 μA is applied on CC1 pin and CC2 pin. When Rd (5.1 kΩ) is attached on either CC1 or CC2, load switch is turned-on after 150 ms debounce time. As soon as load switch is enabled, BC1.2 counter is enabled. To acknowledge detachment, it needs 15 ms debounce time. When load switch is turned-off, bleeder is also enabled at the same time. If VIN voltage was boosted higher than 5 V before acknowledging detachment, VIN voltage is returned to 5 V.

Protocols (Auto-detection)

2.75 V Supply Mode

Some Apple products charge higher current when a dedicated charging port sources specific voltage on D+ and D- lines. FAN6291Q supports 2.75 V on D+ and D- lines, respectively. Apple products regard it as the attached charging port supports 2.4 A, and it charges with maximum 2.4 A. Once FAN6291Q is enabled, D+ and D- supplies 2.75 V as default. ON's intelligent auto-detection acknowledges BC1.2. As soon as BC1.2 gets started, FAN6291Q leaves 2.75 V supply mode immediately. After acknowledging QC3.0 or QC2.0, FAN6291Q does not return 2.75 V supply mode as long as a portable device is not detached.

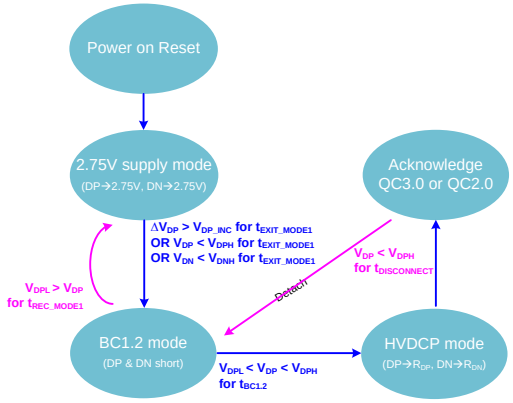


Figure 21 Sequence of Auto-detection

Quick Charge 3.0 (QC3.0) and Quick Charge 2.0 (QC2.0) Protocols

As described in Table 3, FAN6291Q supports up to 12 V (Class A) through QC3.0 protocol.

Table 3. Output Mode of FAN6291Q according to Quick Charge 3.0

V_{DP}	V_{DN}	HVDCP Output Mode
0.6 V	0 V	5 V Mode (Backward compatible with QC2.0)
3.3 V	0.6 V	9 V Mode (Backward compatible with QC2.0)
0.6 V	0.6 V	12 V Mode (Backward compatible with QC2.0)
0.6 V	3.3 V	Continuous Mode
3.3 V	3.3 V	Reserve (Keep previous status)

Within continuous mode, output-voltage can be increased or decreased with 200 mV step per an increment or decrement protocol, respectively. (Refer to Figure 22 and Figure 23 which are examples of increment and decrement). FAN6291Q can enter continuous mode from any of 5 V, 9 V and 12 V modes. However, it can return to 5 V mode from continuous mode.

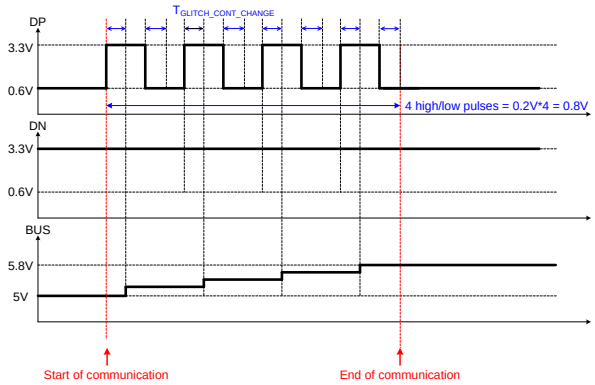


Figure 22 Example of Increment Timing Diagram (800 mV Increment from 5 V)

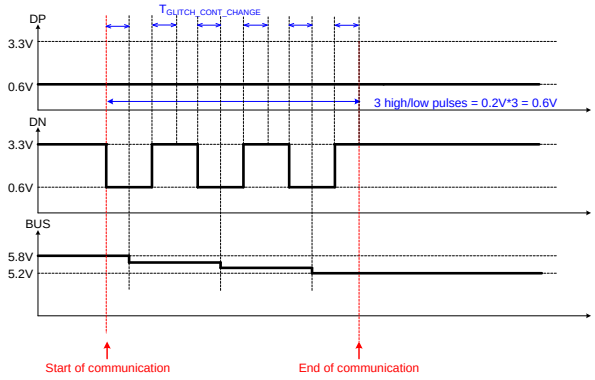


Figure 23 Example of Decrement Timing Diagram (600 mV Decrement from 5.8 V)

Communication Function Description

Constant Voltage Control

The internal constant voltage control block regulates adaptive output voltages. Output voltage is sensed through an external resistor divider. The sensed output voltage is connected to the VREF which is the non-inverting input terminal of the internal operational amplifier. The inverting input terminal is connected to the internal voltage reference (V_{CVR}) which can be adjusted according to the requested output voltage via Quick Charge 3.0 protocol. The amplifier and an internal switch operate as a shunt regulator. The output of the shunt regulator is connected to the external opto-coupler, and this pin is named as Secondary Feedback (SFB). To compensate output voltage regulation being stable, one capacitor and one resistor are connected typically between the SFB and VREF pins as shown in Figure 24. The output voltage can be derived as shown in equation (1) and the recommended ratio of the resistor divider is 5.

$$V_O = V_{CVR} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \quad (1)$$

Constant Current Control

In order to support adaptive constant output current, FAN6291Q incorporates the constant-current control circuit internally. Output current is sensed via a current-sense resistor, R_{CS}, which is connected between the CS pin and GND pin. The sensed signal is internally amplified, and this amplified voltage is connected to the non-inverting input of the internal operation amplifier. Likewise the constant voltage amplifier circuit, it also plays a role as a shunt regulator to regulate the constant output current. In order to compensate output current regulation, one capacitor and one resistor are connected between IREF and SFB pins typically as the Figure 24. The constant output current is decided by the equation (2). 30 mΩ is typically used for the sense resistor.

$$I_{O\_CC} = \frac{1}{A_{V-CCR}} \cdot \frac{V_{CCR}}{R_{CS}} \quad (2)$$

Since CS pin senses small amounts of voltage, the sensing resistor should be positioned as close as possible to CS pin. Shown in Figure 24, an RC low pass filter can be added on the CS pin to be immunized from noise.

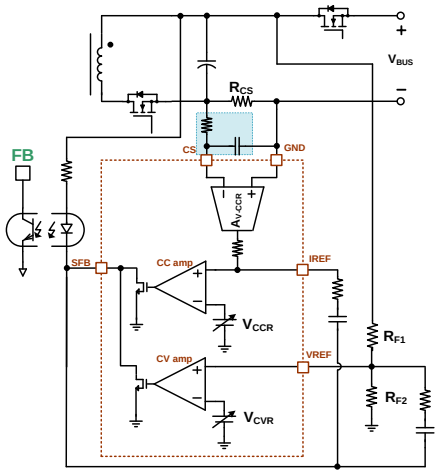


Figure 24 Constant Voltage and Constant Current Circuit

Green Mode Operation

In order to reduce power consumption at light-load conditions, FAN6291Q enters the green mode. When V_{CS} which is the voltage between CS and GND pins is smaller than $V_{CS\text{-}Green}$ with longer duration than $t_{Green\text{-}EN\text{-}Debounce}$, FAN6291Q enters the green mode. Typical output current entering the green mode is 170 mA. While it operates in the green mode, some internal blocks are disabled such as Synchronous Rectifier control block. Therefore, the operating current can be reduced to 1.2 mA (typ.). It leaves green mode when V_{CS} is larger than $V_{CS\text{-}Green}$ with longer duration that $t_{Green\text{-}DIS\text{-}Debounce}$.

Cable Drop Compensation

To regulate the output voltage constantly at the end of a cable regardless of output current, the cable drop compensation function is implemented. The weight of compensation is internally fixed. The compensated output voltage is described in equation (3).

$$V_{OUT-COMPENSATION} = V_{COMR-CDC} \cdot \frac{R_{F1} + R_{F2}}{R_{F2}} \cdot \frac{I_{OUT}}{2} \quad (3)$$

Output OVP also implements cable drop compensation. Ratio of cable drop compensation for output OVP is different with cable drop compensation for constant voltage regulation shown in equation (4).

$$V_{OVP} = V_{IN-OVP} + V_{COMR-OVP} \cdot \frac{I_{OUT}}{2} \quad (4)$$

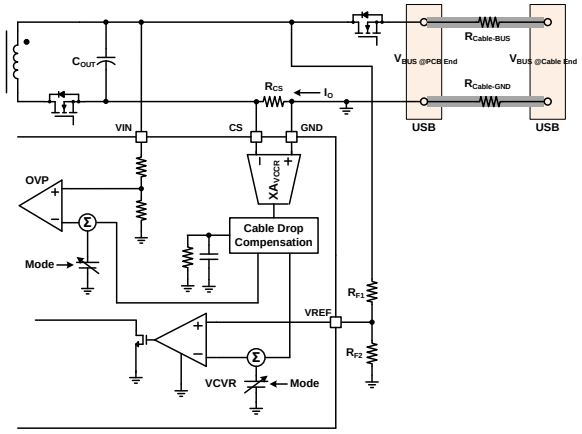


Figure 25 Cable-Drop Compensation Block

Bleeder Section

When a portable device requests to reduce output voltage via Quick Charge 3.0, BUS voltage should be decreased. When the portable device is detached, VIN voltage should be returned to 5 V and BUS voltage should be discharged to zero within a short time. Since the discharging time is very long at light-load condition, FAN6291Q supports the bleeding function. The bleeder function is enabled during $t_{BLD-MAX}$. The bleeding current via VIN pin cannot be controlled. However, the amount of bleeding current through BLD pin can be controlled by the external resistor (R_{BLD}) shown in equation (5).

$$I_{BLD-RType} = \frac{V_{O\_MAX}}{R_{BLD} + R_{Internal}} \quad (5)$$

Since there can be output voltage undershoot during bleeding time if summation of output load current and bleeding current is larger than CC level, bleeding function is disabled when output current is larger than 400 mA (typ.).

Output Over-Voltage Protection

Figure 26 shows the output Over-Voltage Protection (OVP) block, which is adaptive according to output voltage status. Once the sensed output voltage via VIN pin is larger than V_{IN-OVP} longer than t_{D-OVP}, the internal OVP switch is enabled with latch mode. And the latch mode of FAN6291Q is reset when $V_{IN} < V_{LATCH-OFF}$. When FAN6291Q is compatible with FAN602, V_{S-UVP} of FAN602 can be triggered after releasing latch mode of FAN6291Q. According to protection mode of V_{S-UVP} of FAN602, V_{IN-OVP} of FAN6291Q is operated as Extended Auto-Restart mode or latch mode.

Table 2. Over-Voltage Protection Threshold Level

Symbol	V_{OUT} Range	OVP Level (Typ.)
$V_{IN-OVP-5V}$	3.6 V ~ 5.0 V	6.0 V
$V_{IN-OVP-6V}$	5.2 V ~ 6.0 V	8.4 V
$V_{IN-OVP-9V}$	6.2 V ~ 9.0 V	10.8 V
$V_{IN-OVP-12V}$	9.2 V ~ 12.0 V	14.4 V

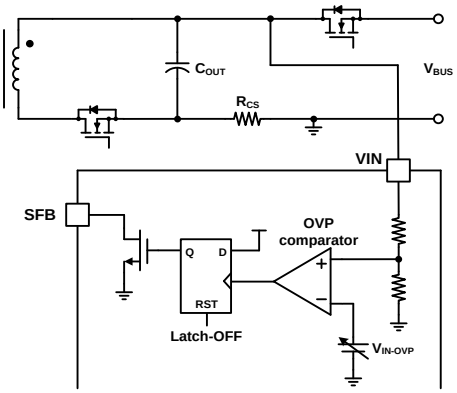


Figure 26 Output Over-Voltage Protection Block

Output Under-Voltage Protection

In order to support foldback level of each output mode, the output under voltage protection (UVP) function is incorporated. The UVP function can reduce power delivery during output soft-short fault. Figure 26 shows its implementation. Once VIN voltage is lower than $V_{IN-UVP-L}$ longer than $t_{D-VIN-UVP}$, the constant current level is reduced to 220 mA (typ.). FAN6291Q leaves UVP when VIN voltage is higher than $V_{IN-UVP-H}$. While the UVP is operated, the synchronous rectifier control is disabled to avoid shoot-through. Some option versions enter the latch mode instead of reducing output current after triggering UVP. The UVP function is only enabled when QC2.0 protocol is accepted. For QC3.0 mode, UVP function is disabled.

Table 3. Under-Voltage Protection Threshold Level

Symbol	V_{OUT} Range	UVP Level (Typ.)
$V_{IN-UVP-L-9V}$	9 V of QC2.0	5.50 V
$V_{IN-UVP-H-9V}$		6.00 V
$V_{IN-UVP-L-12V}$	12 V of QC2.0	8.00 V
$V_{IN-UVP-H-12V}$		8.50 V

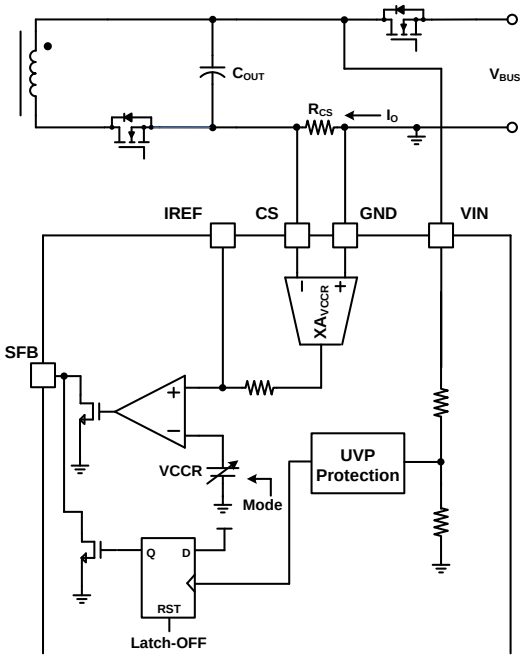


Figure 27 Output Under-Voltage Protection Block

D+/D- Data Line Over-Voltage Protection

Even though severe fault is occurred between BUS and Ground, monitoring data line status also can protect USB fault condition indirectly because data lines (D+/D-) may be polluted at the same time with BUS line pollution. Therefore, FAN6291Q implements data line Over-Voltage-Protection. It can protect when the BUS and D+/D- are short-circuited with small impedance. When voltage on D+ line and/or D- line is higher than V_{DP-OVP} and/or V_{DP-OVP} longer than $V_{DN-DP-OVP-Debounce}$, Over Voltage Protection is triggered. After detecting fault condition, FAN6291Q enters latch mode. When FAN6291Q releases the latch mode, FAN602 enters VS-UVP.

Latch Mode Operation

FAN6291Q implements latch mode operation to deliver fault conditions which are detected on secondary-side to primary-side. When one fault condition is triggered among cable fault Protections, over-voltage protection and under-voltage protection, SFB is started to be pulled-down with latch mode. This latch mode is released when VIN voltage is lower than $V_{Latch-off}$ which is lower than V_{IN-OFF}. As shown on Figure 29, after the Latch Mode is released, the primary-side controller leaves burst mode and starts switching again. Since the $V_{Latch-off}$ is much lower than output voltage level which triggers V_{S-UVP} of the primary-side controller, after releasing latch mode, the primary-side controller triggers V_{S-UVP}. Therefore, throughout implementing the latch mode operation, the primary-side controller can trigger V_{S-UVP}, and the system can enter latch mode. When not only V_{IN-OVP} and cable fault protection are triggered, but also VIN voltage is lower than V_{IN-OFF}, the latch mode is enabled, either. The latch mode operation for V_{IN-OFF} avoids that system becomes open-loop when $V_{IN} < V_{IN-OFF}$.

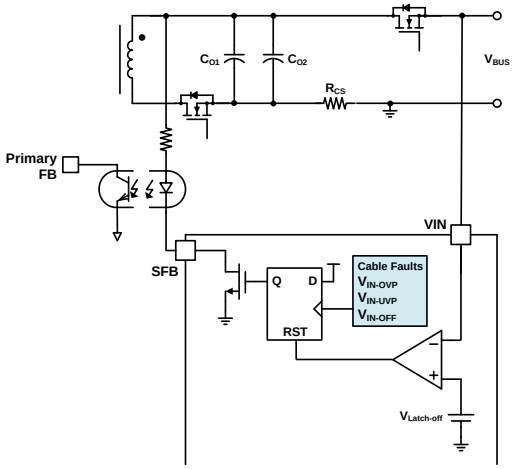


Figure 28 Conceptual Latch Mode Block

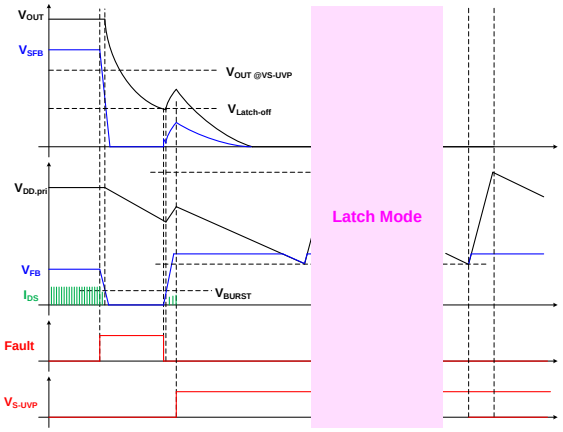


Figure 29 Waveform of Latch Mode Operation

Reset Circuit on VREF and IREF

VREF and IREF pins are connected to V_{IN} through compensation circuits. When CV and CC amplifiers are not enabled, VREF and IREF pin voltages are also increased according to increased V_{IN} voltage (dot lines on Figure 30). The voltages on VREF and IREF are higher than target threshold levels. The Reset circuit on VREF and IREF are implemented as each pin is connected to ground through internal switches. The IREF pin is additionally reset during $t_{Start-Dis-CC}$. Reset circuit pulls-down current, and these currents (IRESET_VREF and IRESET_IREF) can flow through compensation circuits. If current flowing through the opto-coupler is large enough, the primary controller enters burst mode and triggers VS-UVP-H, because of this startup may fail. Rbias helps to decrease current flowing through the opto-coupler, to avoid startup failure. The Rbias design depends on compensation design, typically 2~6 kΩ is recommended.

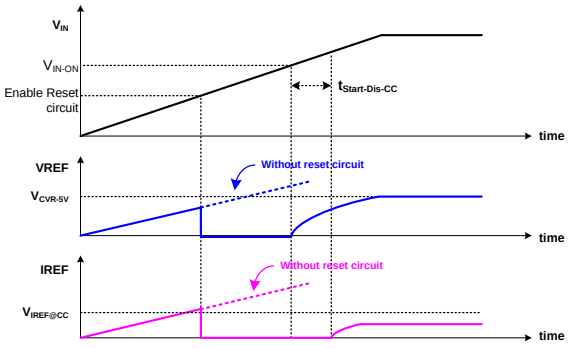


Figure 30 Reset Circuit Operation

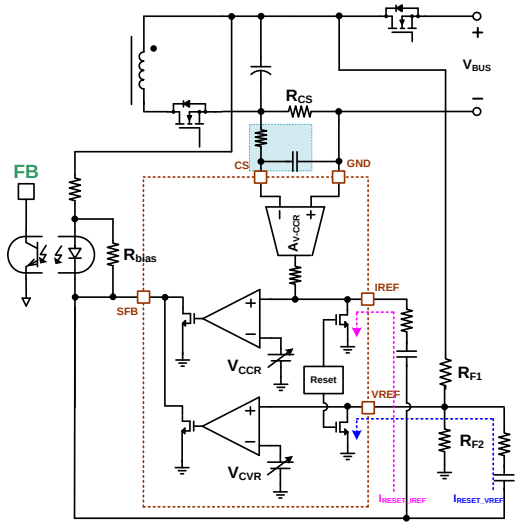


Figure 31 Reset Circuit and R_{bias}

PCB Layout Guidelines

Printed Circuit Board (PCB) layout and design are very important for switching mode power supplies where the voltage and current change with high speed. Good PCB layout minimizes Electro-Magnetic Interference (EMI) and prevents excessive noise from surge or Electro-Static Discharging (ESD). As shown in Figure 33 C_{OUT1} and C_{OUT2} are the output capacitors; Q_2 is the secondary-side SR MOSFET. The following guidelines are recommended for layout designs.

- The main power flows through Q2, C_{OUT1}, C_{OUT2} and R_{CS}. This power path should be separated with signal grounds which are connected to FAN6291Q. In addition, it is recommended that power ground is directly connected to Y-cap. Refer to Figure 32.
- The sensed voltage via R_{CS} is very small value. In order to avoid offset voltage or avoid inducing switching noise on the sensed voltage, R_{CS} should be connected between ground of C_{OUT2} and power ground. And R_{CS} should be positioned as close as possible to CS pin and GND pin. Refer to Figure 33.
- To avoid switching noise ınterference to Synchronous Rectifier operation, R_{LPC-H} and R_{LPC-L} should be close to FAN6291Q. And power path should be apart from LPC path.

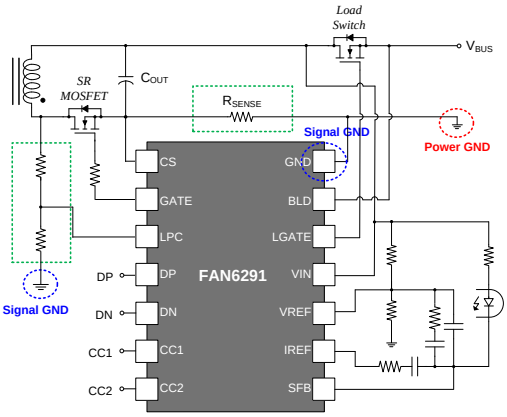


Figure 32 Power and Signal Ground on the Secondary-Side

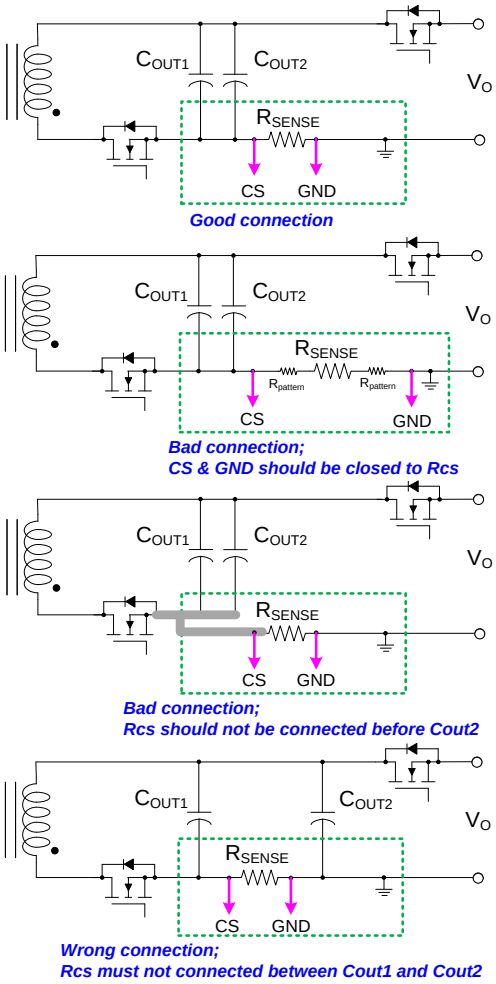
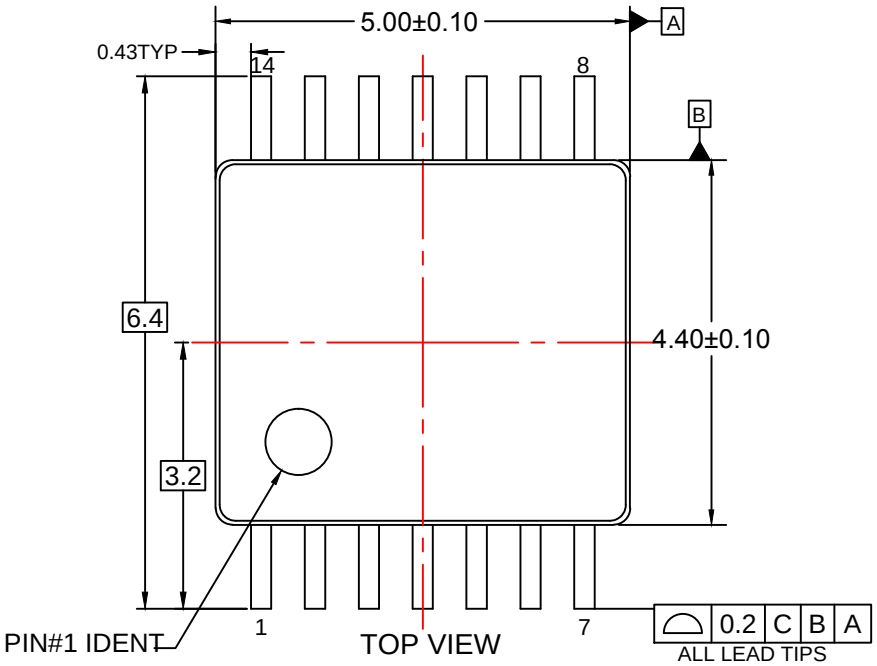


Figure 33 Examples of Sensing Resistor Connection

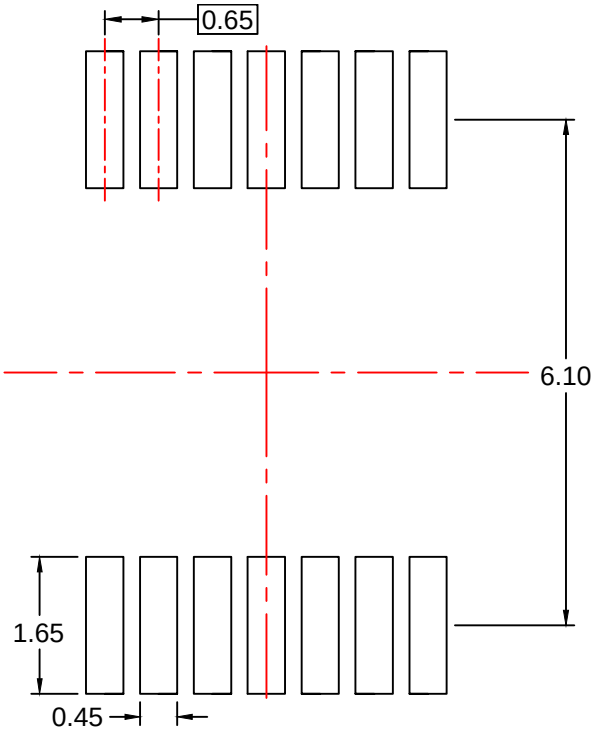
ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method
FAN6291QFMTCX	-40°C to +125°C	14-Lead, TSSOP JEDEC MO-153, 4.4 mm Wide	Tape & Reel
FAN6291QHMTCX	-40°C to +125°C	14-Lead, TSSOP JEDEC MO-153, 4.4 mm Wide	Tape & Reel

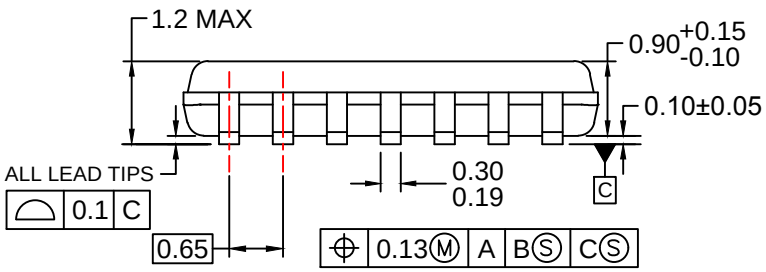
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D



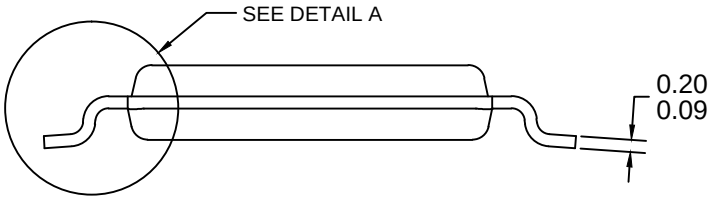
TOP VIEW

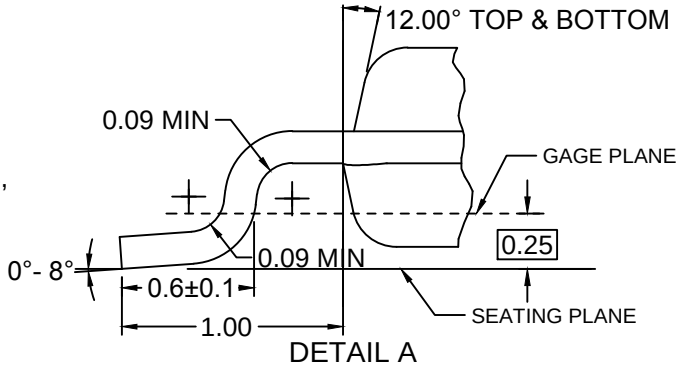


RECOMMENDED LAND PATTERN



FRONT VIEW





DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

FAIRCHILD

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