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# FAN7382

## High- and Low-Side Gate Driver



### Features

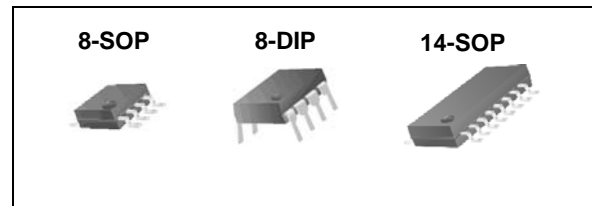
- Floating Channels Designed for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative  $V_S$  Swing to -9.8V for Signal Propagation at  $V_{CC}=V_{BS}=15V$
- $V_{CC}$  &  $V_{BS}$  Supply Range from 10V to 20V
- UVLO Functions for Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50nsec
- Output In-phase with Input Signal

### Description

The FAN7382, a monolithic high and low side gate-drive IC, can drive MOSFETs and IGBTs that operate up to +600V. Fairchild's high-voltage process and common-mode noise canceling technique provides stable operation of the high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to  $V_S=-9.8V$  (typical) for  $V_{BS}=15V$ . The input logic level is compatible with standard TTL-series logic gates. UVLO circuits for both channels prevent malfunction when  $V_{CC}$  or  $V_{BS}$  is lower than the specified threshold voltage. Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for fluorescent lamp ballasts, PDP scan drivers, motor controls, etc.

### Applications

- PDP Scan Driver
- Fluorescent Lamp Ballast
- SMPS
- Motor Driver



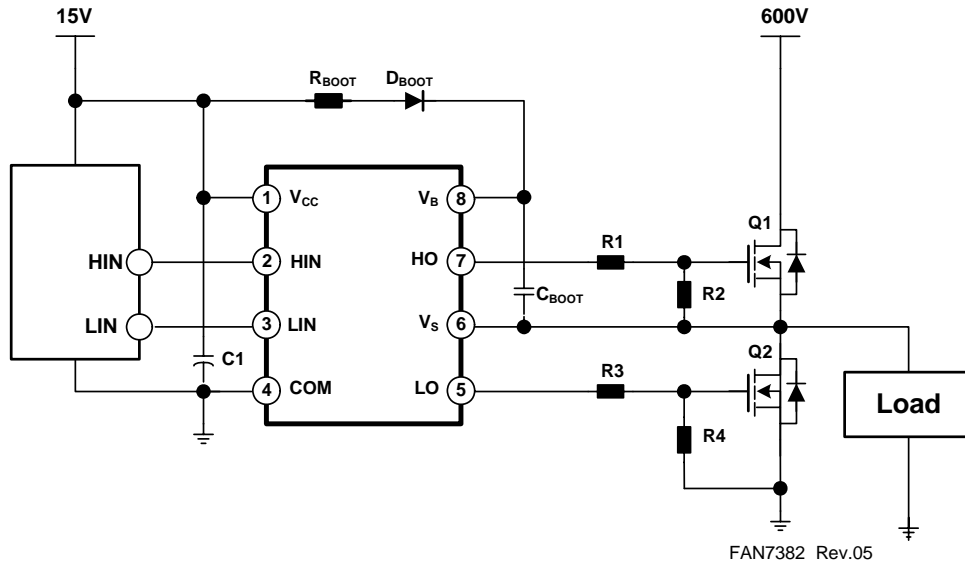
### Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7382N	8-DIP	Yes	-40°C ~ 125°C	Tube
FAN7382M <sup>(1)</sup>	8-SOP			Tube
FAN7382MX <sup>(1)</sup>				Tape & Reel
FAN7382M1 <sup>(1)</sup>	14-SOP			Tube
FAN7382M1X <sup>(1)</sup>				Tape & Reel

#### Note:

1. These devices passed wave soldering test by JESD22A-111.

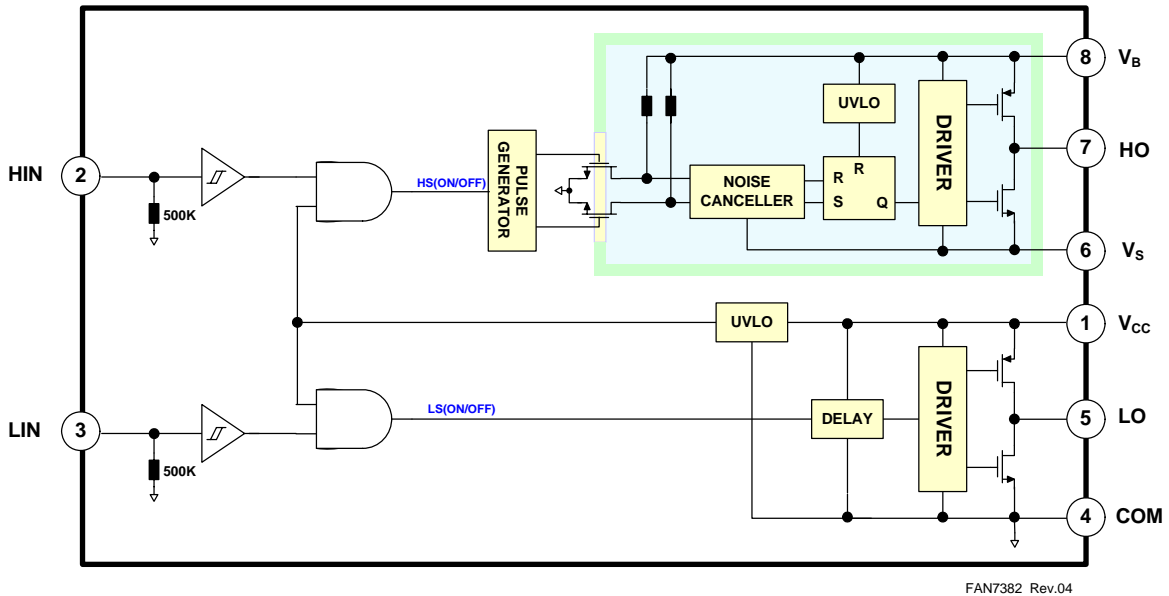
Typical Application Circuit



FAN7382 Rev.05

Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram



FAN7382 Rev.04

Figure 2. Functional Block Diagram

## Pin Assignments

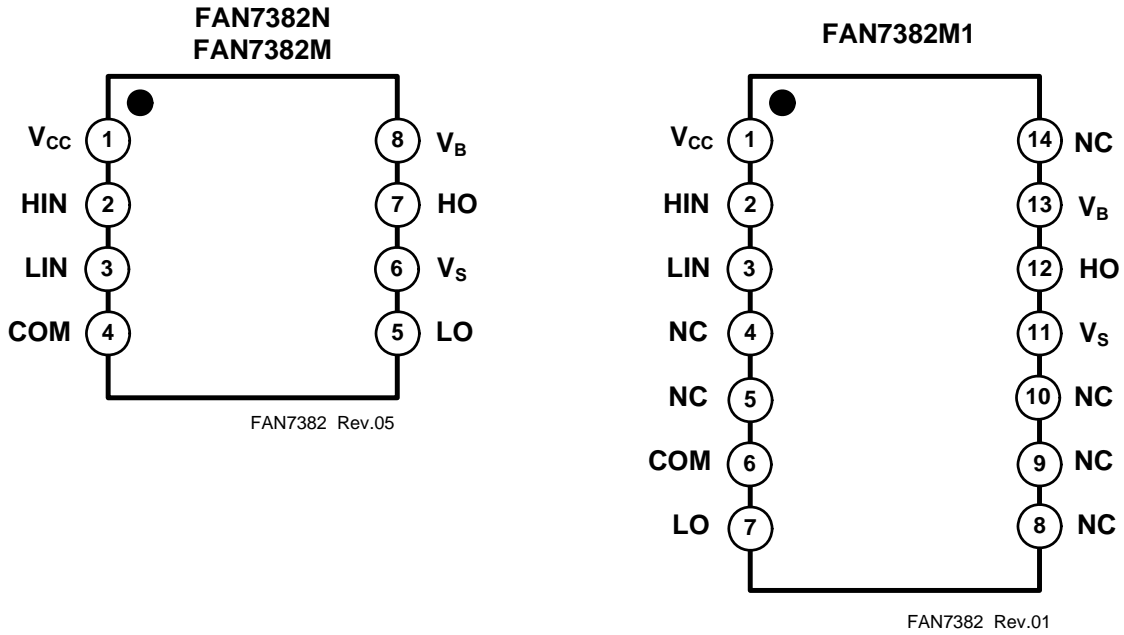


Figure 3. Pin Configuration (Top View)

## Pin Definitions

Name	Description
$V_{CC}$	Low-Side Supply Voltage
HIN	Logic Input for High-Side Gate Driver Output
LIN	Logic Input for Low-Side Gate Driver Output
COM	Logic Ground and Low-Side Driver Return
LO	Low-Side Driver Output
$V_S$	High-Voltage Floating Supply Return
HO	High-Side Driver Output
$V_B$	High-Side Floating Supply

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Characteristics	Min.	Max.	Unit
$V_S$	High-side offset voltage	$V_B-25$	$V_B+0.3$	V
$V_B$	High-side floating supply voltage	-0.3	625	
$V_{HO}$	High-side floating output voltage HO	$V_S-0.3$	$V_B+0.3$	
$V_{CC}$	Low-side and logic fixed supply voltage	-0.3	25	
$V_{LO}$	Low-side output voltage LO	-0.3	$V_{CC}+0.3$	
$V_{IN}$	Logic input voltage (HIN, LIN)	-0.3	$V_{CC}+0.3$	
COM	Logic ground	$V_{CC}-25$	$V_{CC}+0.3$	
$dV_S/dt$	Allowable offset voltage slew rate		50	V/ns
$P_D^{(2)(3)(4)}$	Power dissipation	8-SOP	0.625	W
		14-SOP	1.0	
		8-DIP	1.2	
$\theta_{JA}$	Thermal resistance, junction-to-ambient	8-SOP	200	°C/W
		14-SOP	110	
		8-DIP	100	
$T_J$	Junction temperature		150	°C
$T_{STG}$	Storage temperature		150	°C

### Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
  - JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
  - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- Do not exceed  $P_D$  under any circumstances.

## Recommended Operating Ratings

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_B$	High-side floating supply voltage	$V_S+10$	$V_S+20$	V
$V_S$	High-side floating supply offset voltage	$6-V_{CC}$	600	
$V_{HO}$	High-side (HO) output voltage	$V_S$	$V_B$	
$V_{LO}$	Low-side (LO) output voltage	COM	$V_{CC}$	
$V_{IN}$	Logic input voltage (HIN, LIN)	COM	$V_{CC}$	
$V_{CC}$	Low-side supply voltage	10	20	
$T_A$	Ambient temperature	-40	125	°C

## Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ )=15.0V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified. The  $V_{IN}$  and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to  $V_S$  and COM and are applicable to the respective outputs HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply under-voltage positive going threshold		8.2	9.2	10.0	V
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply under-voltage negative going threshold		7.6	8.7	9.6	
$V_{CCUVH}$ $V_{BSUVH}$	$V_{CC}$ supply under-voltage lockout hysteresis			0.6		
$I_{LK}$	Offset supply leakage current	$V_B=V_S=600\text{V}$			50	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	$V_{IN}=0\text{V}$ or $5\text{V}$		45	120	
$I_{QCC}$	Quiescent $V_{CC}$ supply current	$V_{IN}=0\text{V}$ or $5\text{V}$		70	180	
$I_{PBS}$	Operating $V_{BS}$ supply current	$f_{IN}=20\text{kHz}$ , rms value			600	$\mu\text{A}$
$I_{PCC}$	Operating $V_{CC}$ supply current	$f_{IN}=20\text{kHz}$ , rms value			600	
$V_{IH}$	Logic "1" input voltage		2.9			V
$V_{IL}$	Logic "0" input voltage				0.8	
$V_{OH}$	High-level output voltage, $V_{BIAS}-V_O$	$I_O=20\text{mA}$			1.0	
$V_{OL}$	Low-level output voltage, $V_O$				0.6	
$I_{IN+}$	Logic "1" input bias current	$V_{IN}=5\text{V}$		10	20	$\mu\text{A}$
$I_{IN-}$	Logic "0" input bias current	$V_{IN}=0\text{V}$		1.0	2.0	
$I_{O+}$	Output high short-circuit pulsed current	$V_O=0\text{V}$ , $V_{IN}=5\text{V}$ with $PW<10\mu\text{s}$	250	350		mA
$I_{O-}$	Output low short-circuit pulsed current	$V_O=15\text{V}$ , $V_{IN}=0\text{V}$ with $PW<10\mu\text{s}$	500	650		
$V_S$	Allowable negative $V_S$ pin voltage for HIN signal propagation to HO			-9.8	-7.0	V

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ )=15.0V,  $V_S=COM$ ,  $C_L=1000\text{pF}$  and,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on propagation delay	$V_S=0\text{V}$	100	170	300	ns
$t_{off}$	Turn-off propagation delay	$V_S=0\text{V}$ or $600\text{V}^{(5)}$	100	200	300	
$t_r$	Turn-on rise time		20	60	140	
$t_f$	Turn-off fall time			30	80	
MT	Delay matching, HS & LS turn-on/off				50	

### Note:

5. This parameter guaranteed by design.

Typical Characteristics

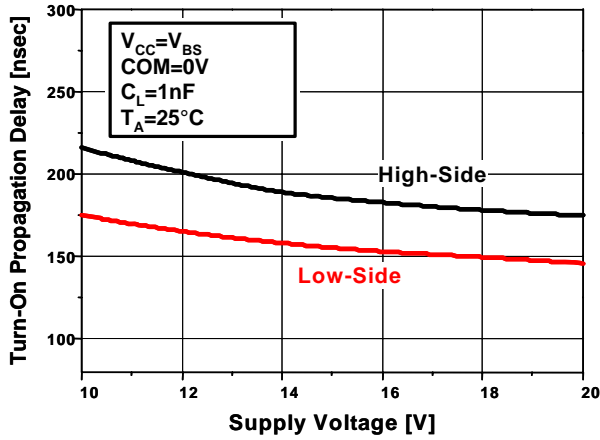


Figure 4. Turn-On Propagation Delay vs. Supply Voltage

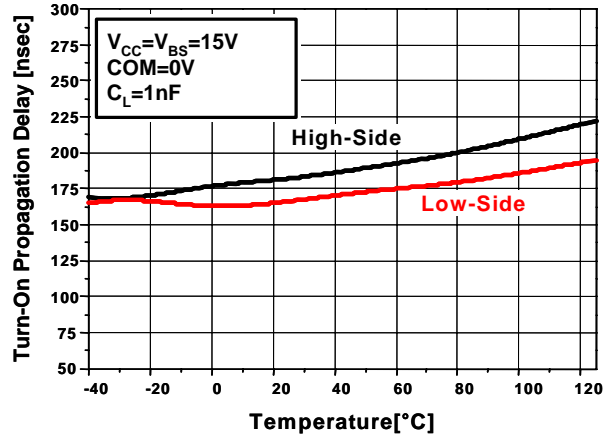


Figure 5. Turn-On Propagation Delay vs. Temp.

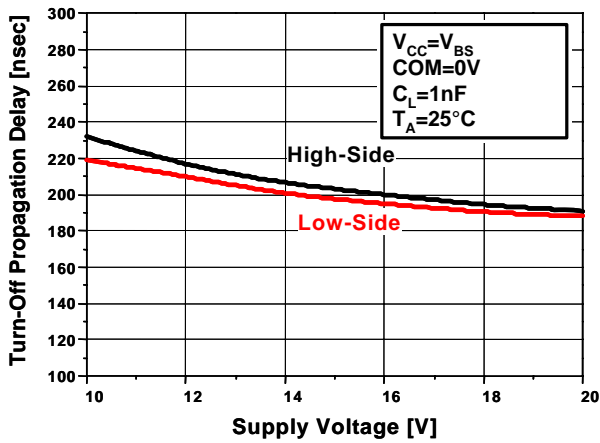


Figure 6. Turn-Off Propagation Delay vs. Supply Voltage

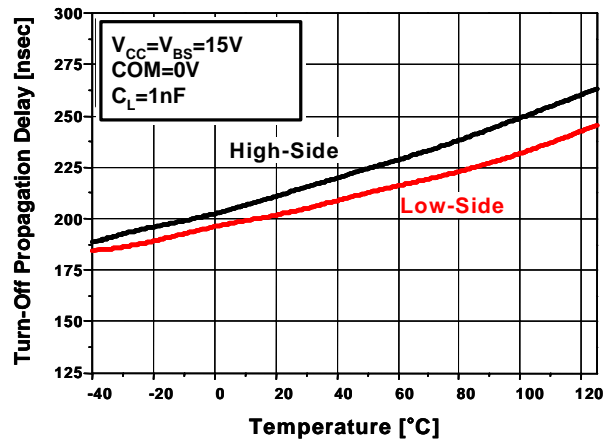


Figure 7. Turn-Off Propagation Delay vs. Temp.

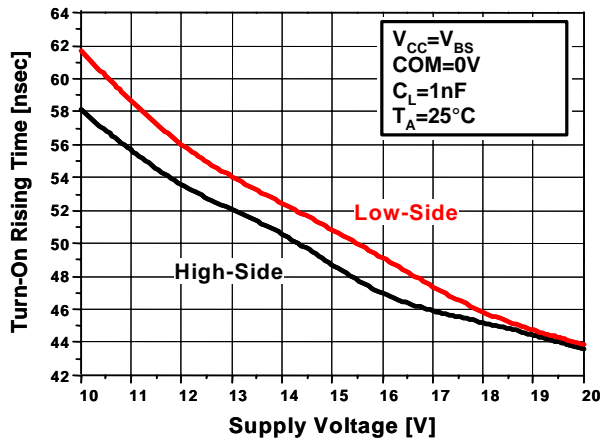


Figure 8. Turn-On Rising Time vs. Supply Voltage

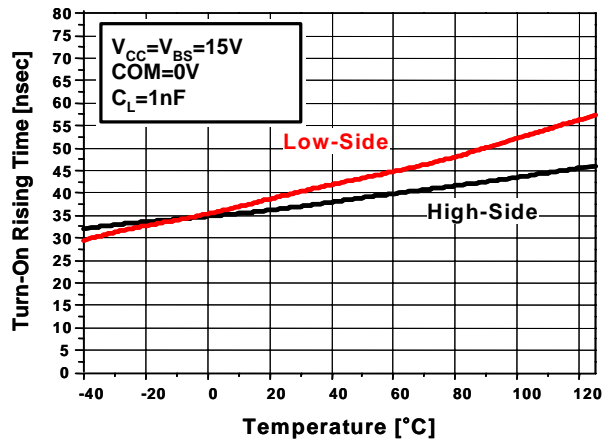


Figure 9. Turn-On Rising Time vs. Temp.

Typical Characteristics (Continued)

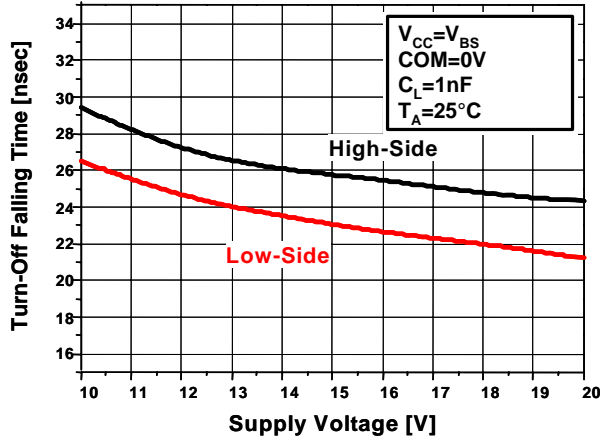


Figure 10. Turn-Off Falling Time vs. Supply Voltage

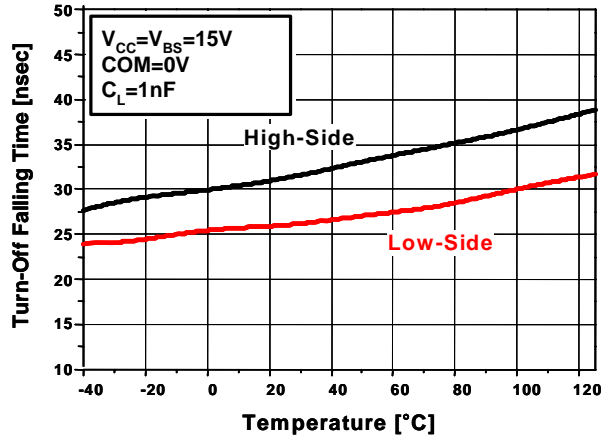


Figure 11. Turn-Off Falling Time vs. Temp.

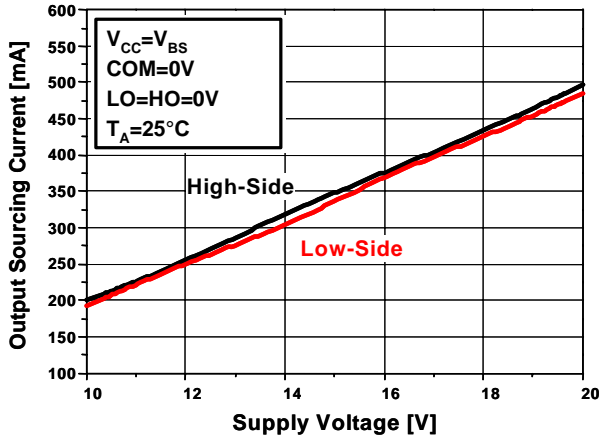


Figure 12. Output Sourcing Current vs. Supply Voltage

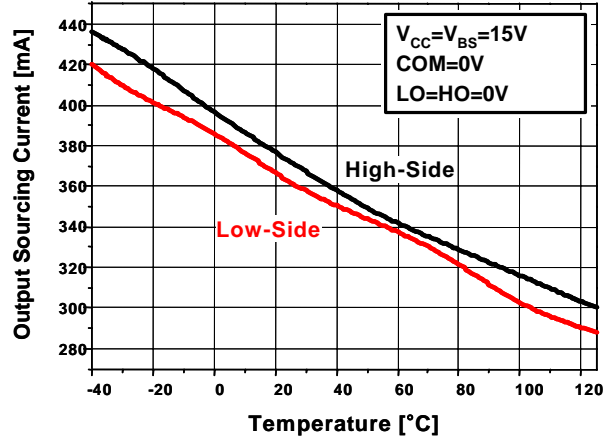


Figure 13. Output Sourcing Current vs. Temp

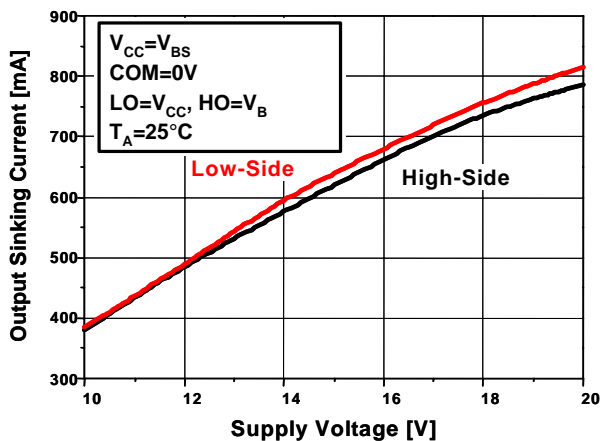


Figure 14. Output Sinking Current vs. Supply Voltage

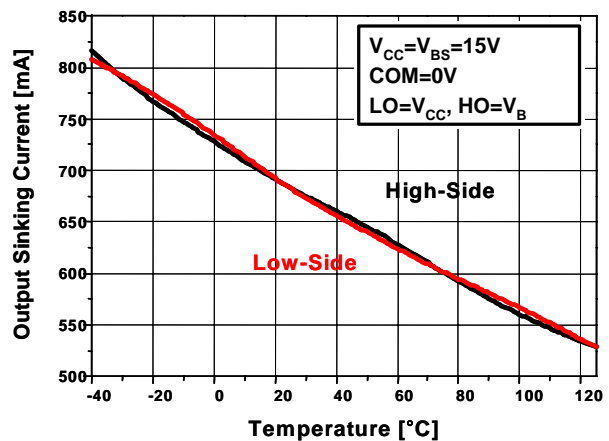


Figure 15. Output Sinking Current vs. Temp.



Typical Characteristics (Continued)

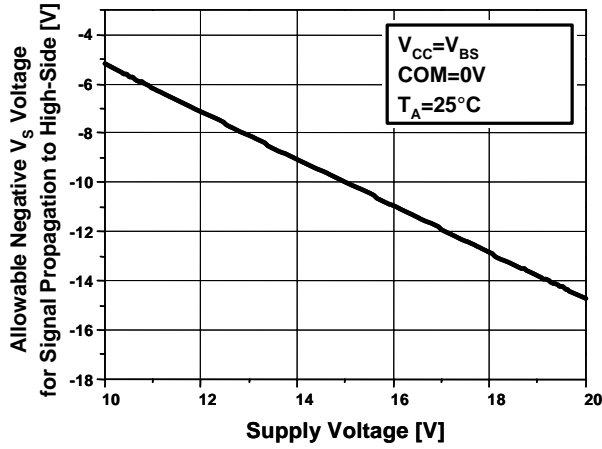


Figure 16. Allowable Negative  $V_S$  Voltage for Signal Propagation to High Side vs. Supply Voltage

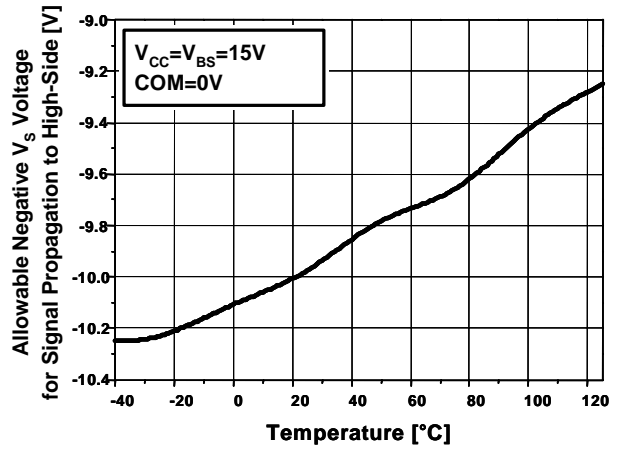


Figure 17. Allowable Negative  $V_S$  Voltage for Signal Propagation to High Side vs. Temp.

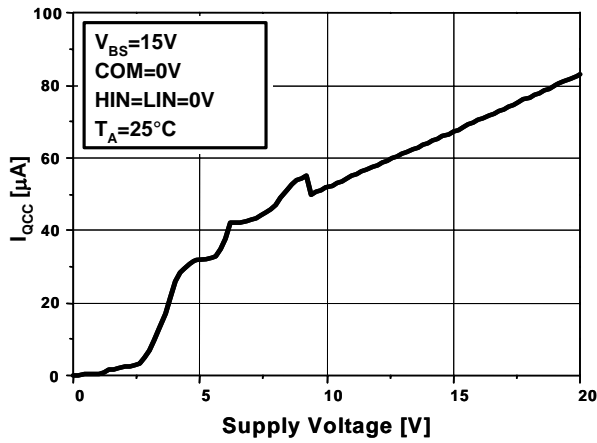


Figure 18.  $I_{QCC}$  vs. Supply Voltage

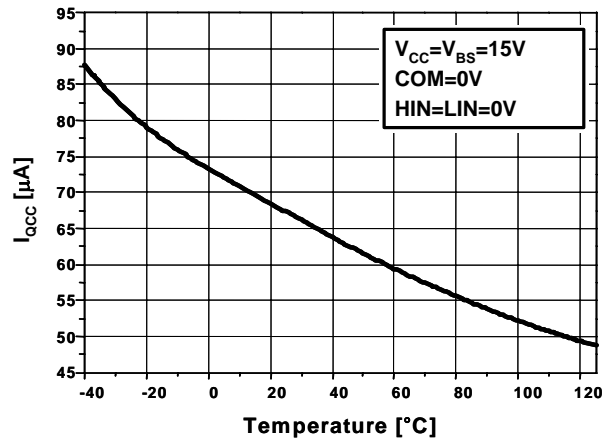


Figure 19.  $I_{QCC}$  vs. Temp.

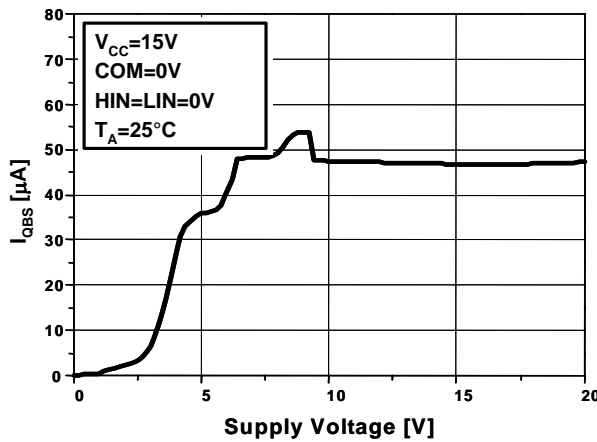


Figure 20.  $I_{QBS}$  vs. Supply Voltage

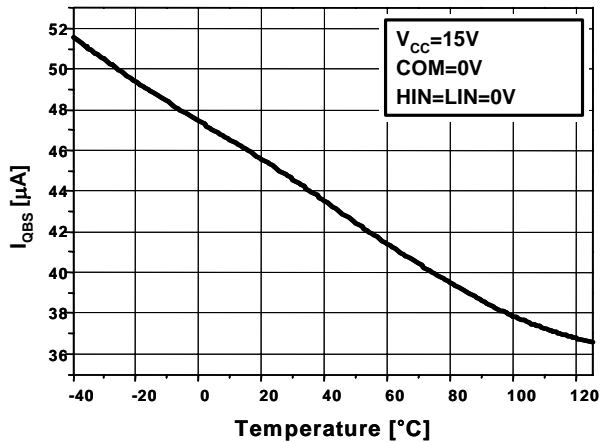


Figure 21.  $I_{QBS}$  vs. Temp.

Typical Characteristics (Continued)

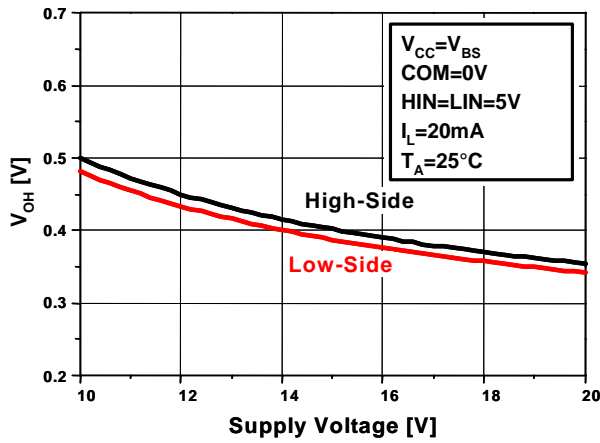


Figure 22. High-Level Output Voltage vs. Supply Voltage

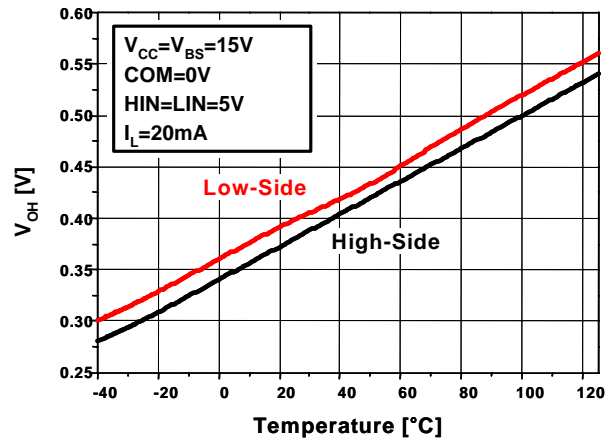


Figure 23. High-Level Output Voltage vs. Temp.

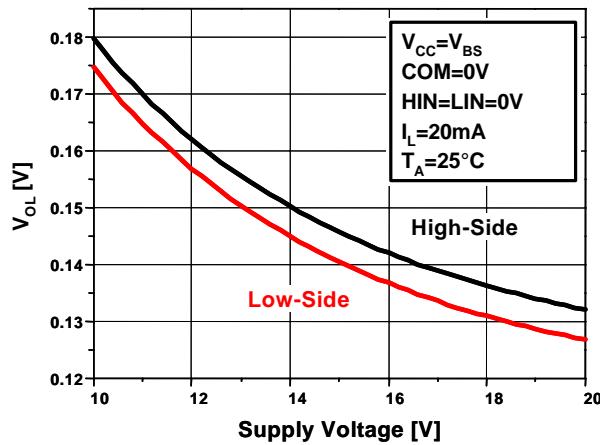


Figure 24. Low-Level Output Voltage vs. Supply Voltage

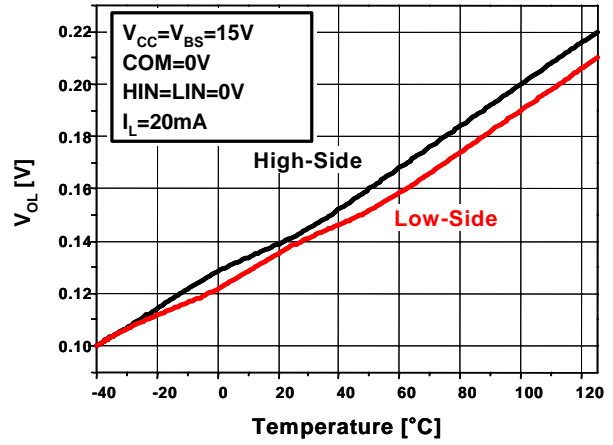


Figure 25. Low-Level Output Voltage vs. Temp.

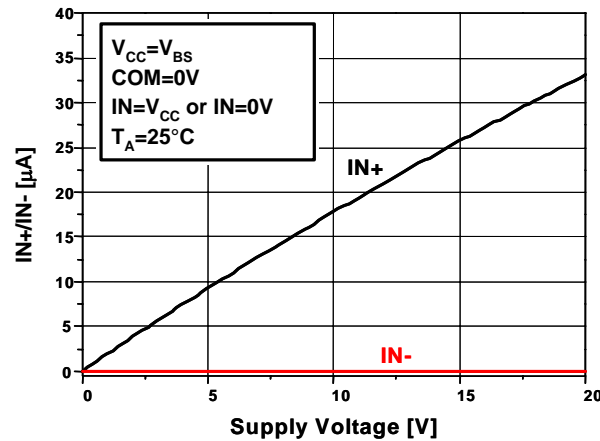


Figure 26. Input Bias Current vs. Supply Voltage

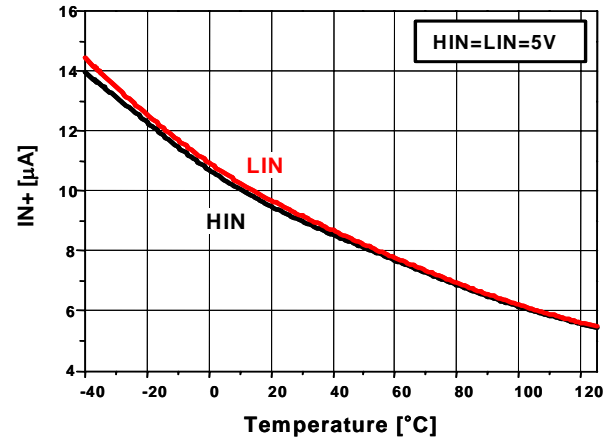


Figure 27. Input Bias Current vs. Temp.

Typical Characteristics (Continued)

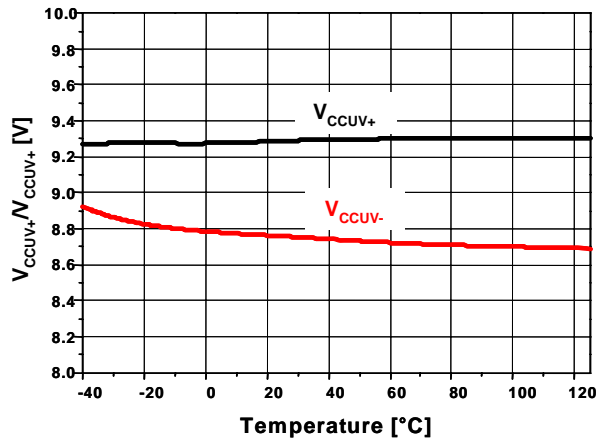


Figure 28. V<sub>CC</sub> UVLO Threshold Voltage vs. Temp.

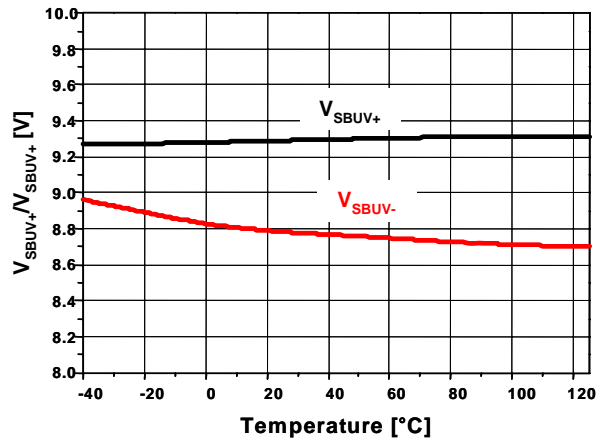


Figure 29. V<sub>BS</sub> UVLO Threshold Voltage vs. Temp.

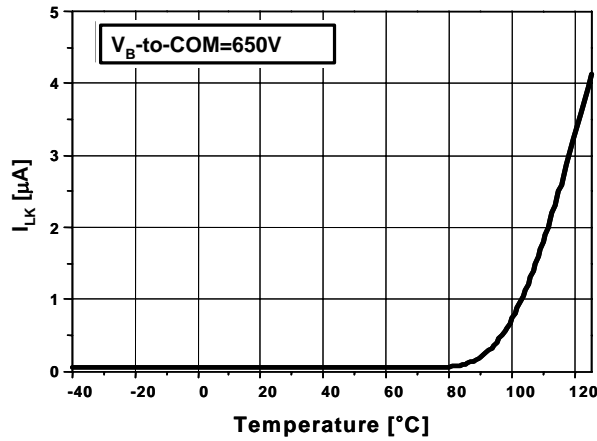


Figure 30. V<sub>B</sub> to COM Leakage Current vs. Temp.

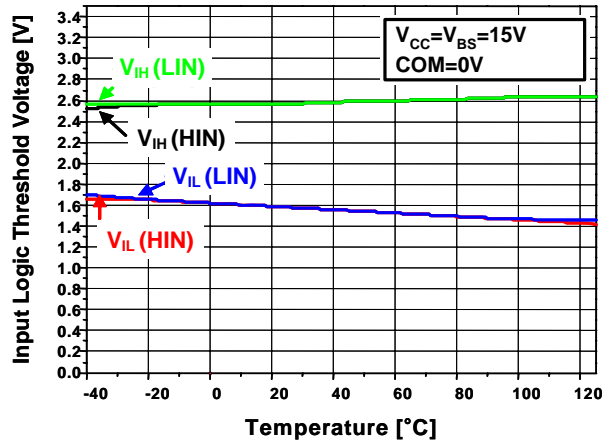
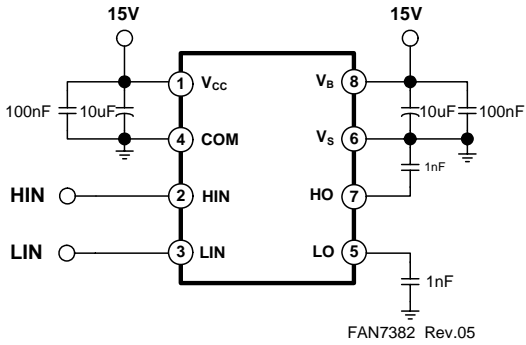
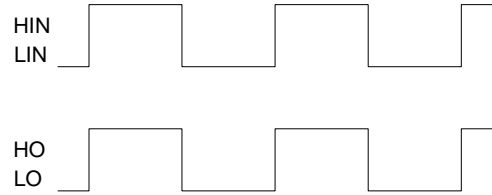


Figure 31. Input Logic Threshold Voltage vs. Temp.

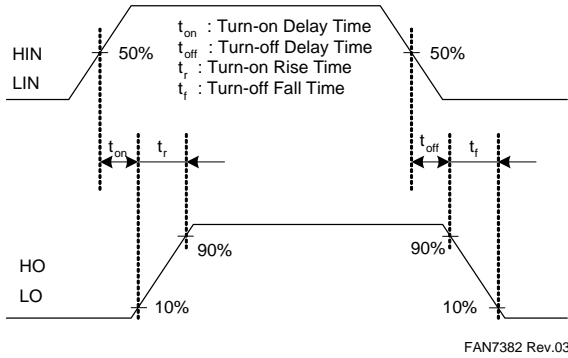
**Typical Characteristics** (Continued)



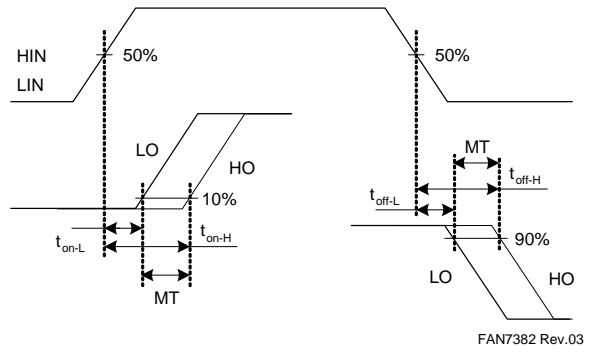
**Figure 32. Switching Time Test Circuit**



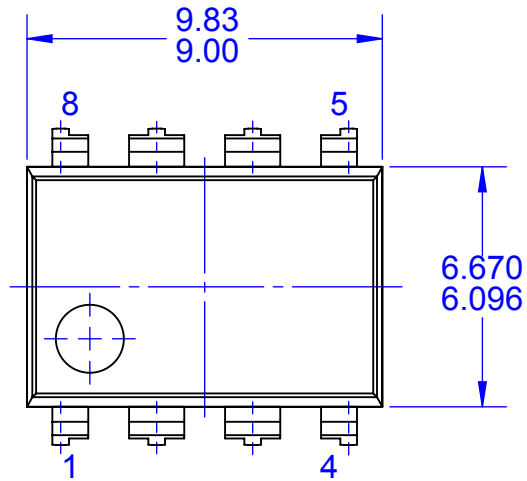
**Figure 33. Input / Output Timing Diagram**



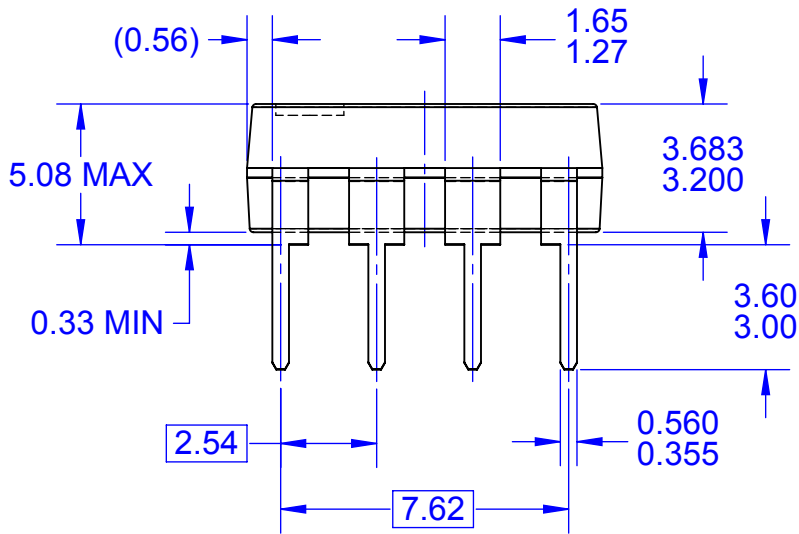
**Figure 34. Switching Time Waveform Definition**



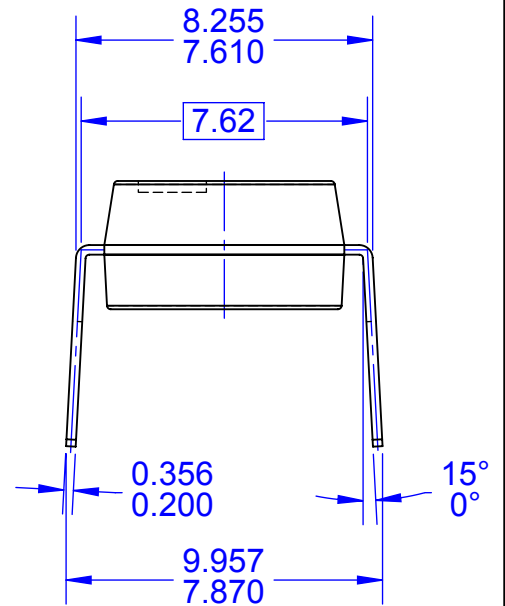
**Figure 35. Delay Matching Waveform Definition**



TOP VIEW



FRONT VIEW

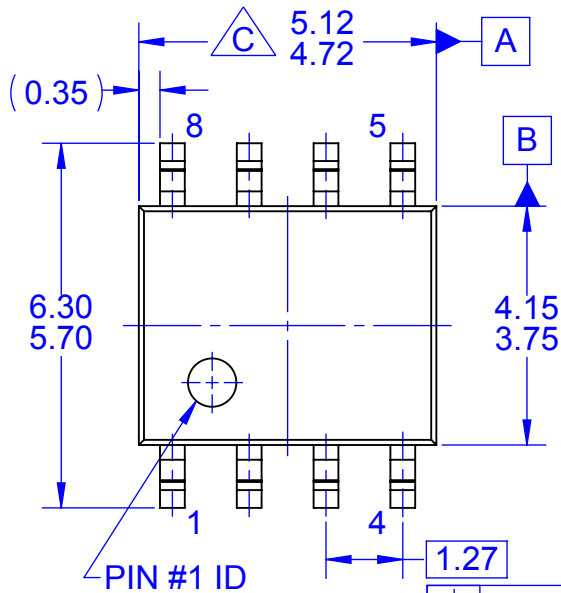


SIDE VIEW

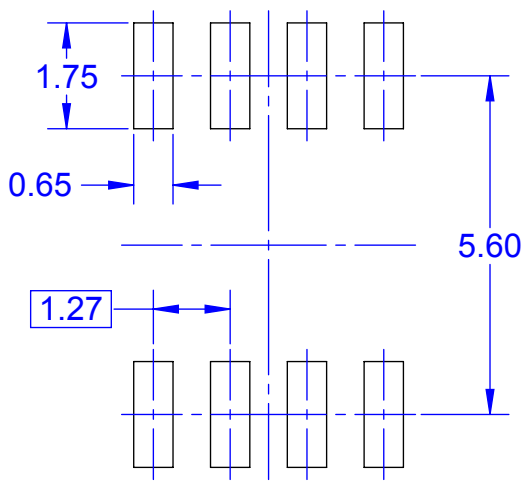
NOTES:

- A. CONFORMS TO JEDEC MS-001, VARIATION BA
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009
- E. DRAWING FILENAME: MKT-N08Frev3

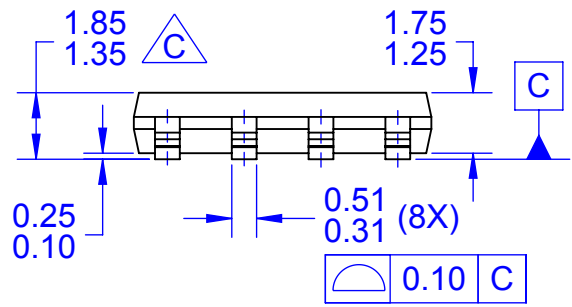




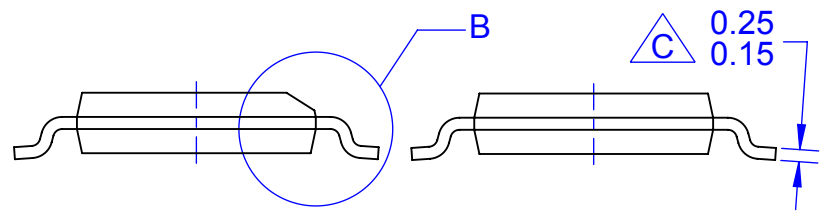
TOP VIEW



LAND PATTERN RECOMMENDATION



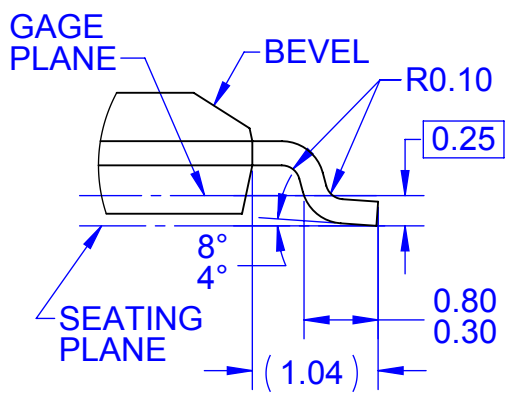
FRONT VIEW



OPTION A  
BEVEL EDGE

OPTION B  
NON-BEVEL EDGE

SIDE VIEW

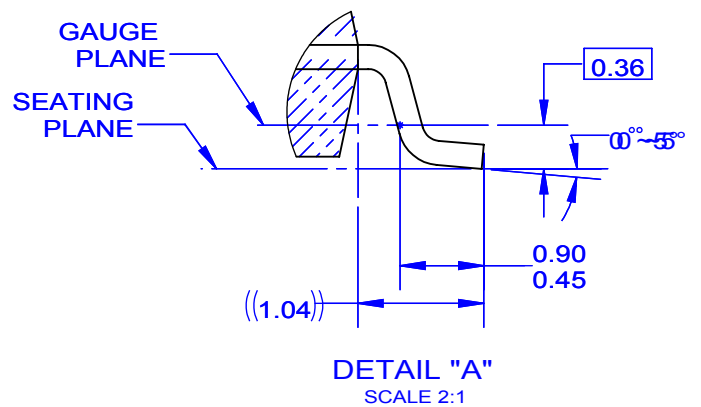
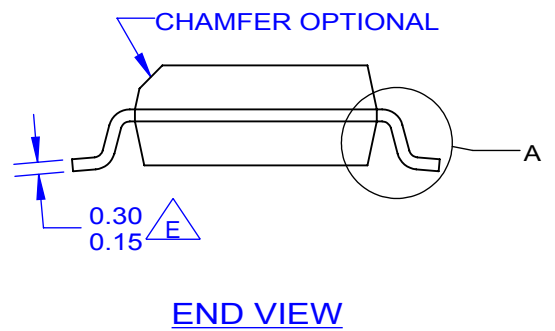
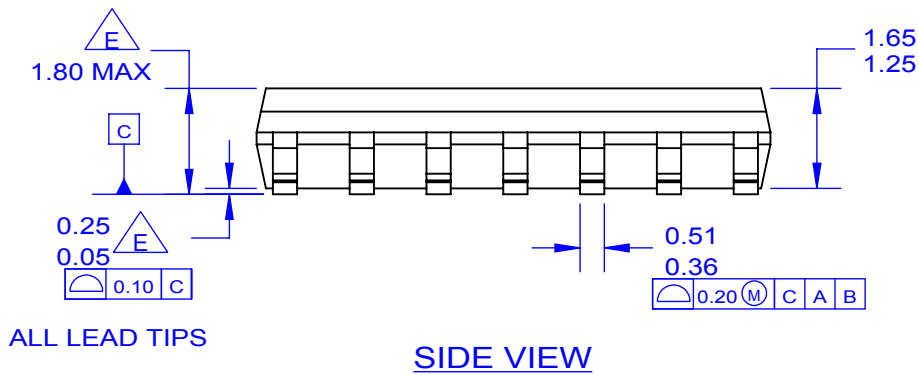
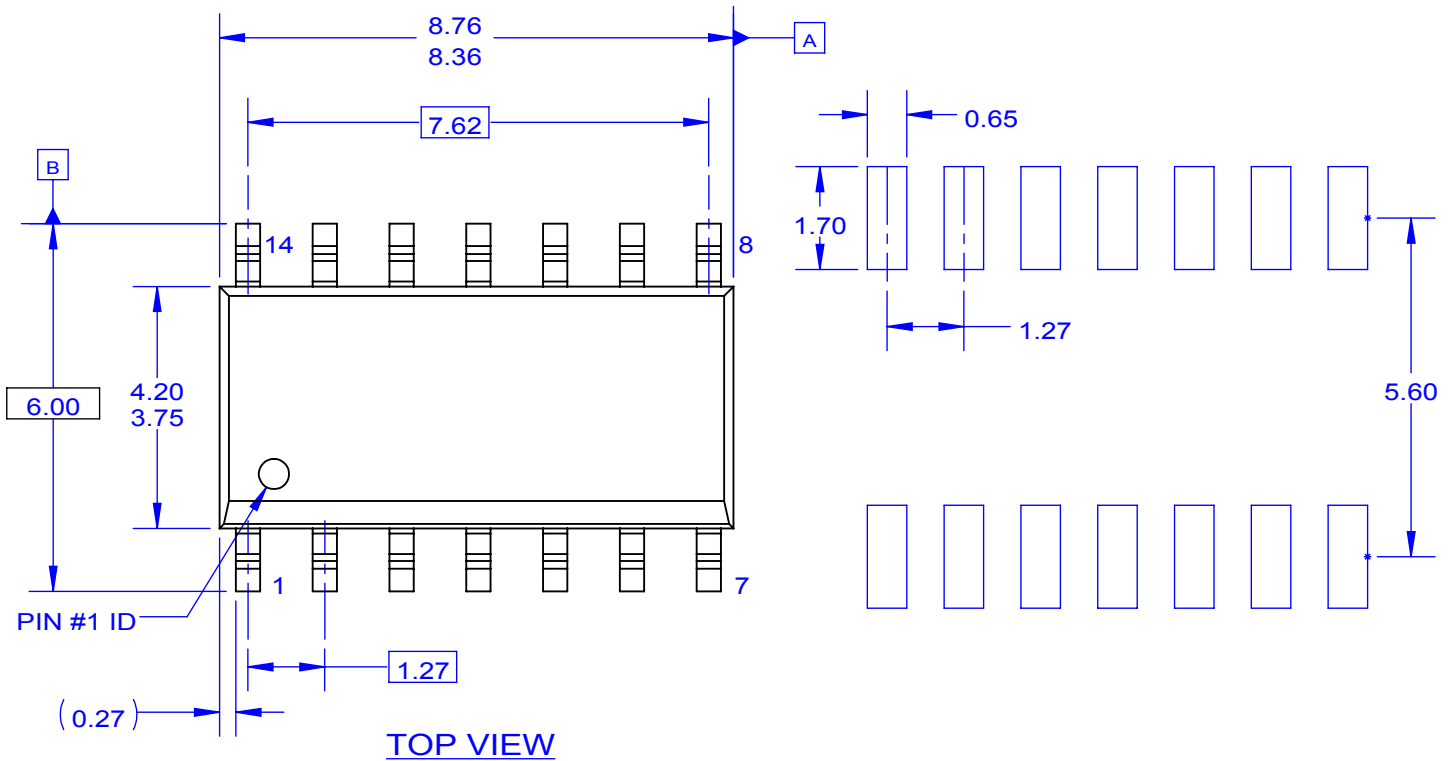


DETAIL "B"  
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

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- B. ALL DIMENSIONS ARE IN MILLIMETERS
- $\triangle C$  OUT OF JEDEC STANDARD VALUE
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- E. LAND PATTERN AS PER IPC SOIC127P600X175-8M
- F. DRAWING FILENAME: MKT-M08Brev2





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C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

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E. OUT OF JEDEC STANDARD VALUE.

F. LAND PATTERN STANDARD: SOIC127P600X145-14M.

G. FILE NAME: MKT-M14C REV2

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