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Sept 2017

FCA47N60F N-Channel SuperFET® FRFET® MOSFET 600 V, 47 A, 73 m Ω

Features

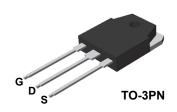
- 650 V @ T_{.I} = 150 °C
- Typ. R_{DS(on)} = 62 mΩ
- Fast Recovery Time (Typ. T_{rr} = 240 ns)
- Ultra Low Gate Charge (Typ. Q_q = 210 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 420 pF$)
- · 100% Avalanche Tested
- · RoHS Compliant

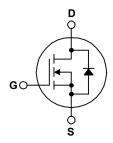
Applications

- · Solar Inverter
- · AC-DC Power Supply

Description

SuperFET® MOSFET is ON Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FCA47N60F	Unit
V_{DSS}	Drain-Source Voltage		600	V	
I _D	Drain Current	- Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		47 29.7	A A
I _{DM}	Drain Current	- Pulsed	(Note 1)	141	Α
V _{GSS}	Gate-Source voltage		± 30	V	
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	1800	mJ
I _{AR}	Avalanche Current		(Note 1)	47	A
E _{AR}	Repetitive Avalanche Energy		(Note 1)	41.7	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	50	V/ns
P _D	Power Dissipation	(T _C = 25°C) - Derate Above 25°C		417 3.33	W W/°C
T _{J,} T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C	

Thermal Characteristics

Symbol	Parameter	FCA47N60F	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.3	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	41.7	°C/W	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCA47N60F	FCA47N60F	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 25^{\circ}\text{C}$	600			V
		$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 150^{\circ}\text{C}$	-	650		V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	0.6		V/°C
BV _{DS}	Drain to Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 47 A		700		V
I _{DSS}	Zero Gate Voltage Drain Current	Vero Gate Voltage Drain Current $V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}, V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$			10 100	μA μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	-		100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	-		-100	nA
On Charac	cteristics			I.		
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 23.5 A		0.062	0.073	Ω
9 _{FS}	Forward Transconductance $V_{DS} = 20 \text{ V}, I_D = 23.5 \text{ A}$			40		S
Dynamic 0	Characteristics			l .		
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,		5900	8000	pF
C _{oss}	Output Capacitance	f = 1 MHz	-	3200	4200	pF
C _{rss}	Reverse Transfer Capacitance		-	250		pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1 MHz		160		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	420		pF
Switching	Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 47 A,		185	430	ns
t _r	Turn-On Rise Time	V_{GS} = 10 V, R_G = 25 Ω	-	210	450	ns
t _{d(off)}	Turn-Off Delay Time		-	520	1100	ns
t _f	Turn-Off Fall Time	(Note 4)	-	75	160	ns
Qg	Total Gate Charge	V _{DS} = 480 V, I _D = 47 A,	-	210	270	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V	-	38		nC
Q _{gd}	Gate-Drain Charge	(Note 4)	-	110		nC
Drain-Sou	rce Diode Characteristics and Maximun	n Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				47	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				141	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 47 A	-		1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 47 A,		240		ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	-	2.04		μС

Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. $\rm I_{AS}$ = 18 A, $\rm V_{DD}$ = 50 V, $\rm R_{G}$ = 25 $\Omega,$ starting $\rm T_{J}$ = 25°C.
- 3. I $_{SD}$ \leq 47 A, di/dt \leq 1200 A/µs, V $_{DD}$ \leq BV $_{DSS}$, starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

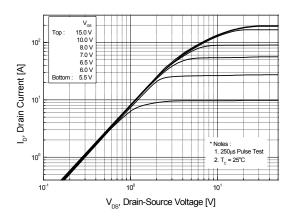


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

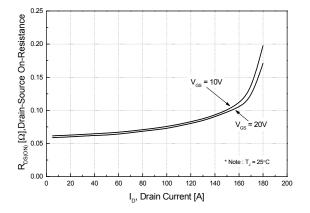


Figure 2. Transfer Characteristics

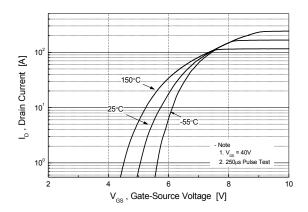


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

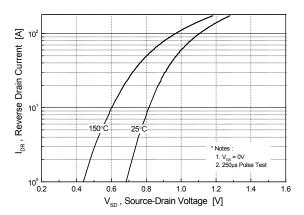


Figure 5. Capacitance Characteristics

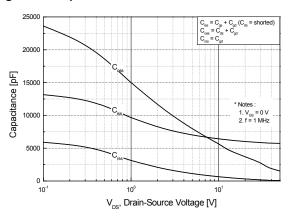
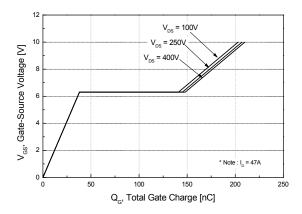


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

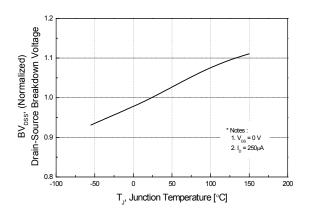


Figure 8. On-Resistance Variation vs. Temperature

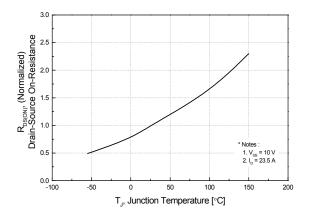


Figure 9. Safe Operating Area

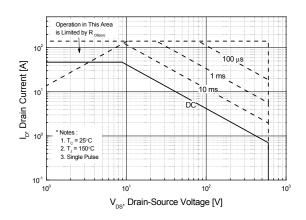


Figure 10. Maximum Drain Current vs. Case Temperature

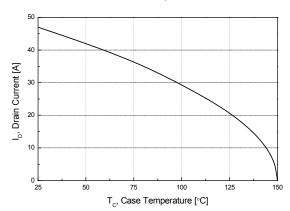


Figure 11. Transient Thermal Response Curve

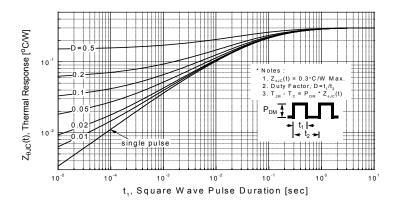


Figure 12. Gate Charge Test Circuit & Waveform

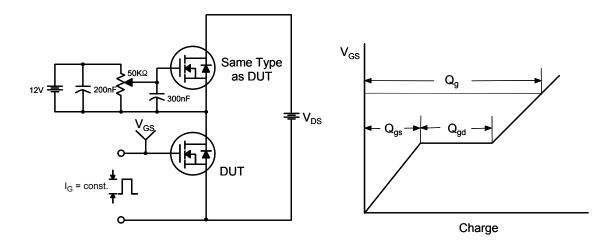


Figure 13. Resistive Switching Test Circuit & Waveforms

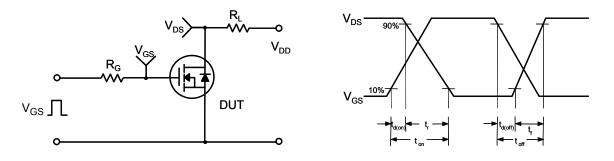
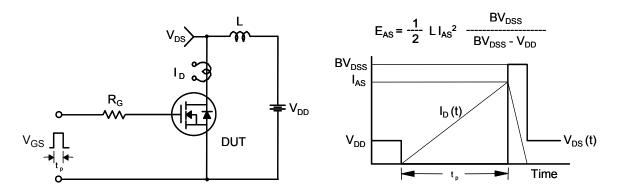


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

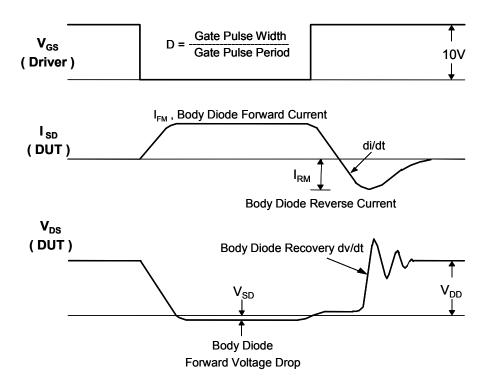


Driver

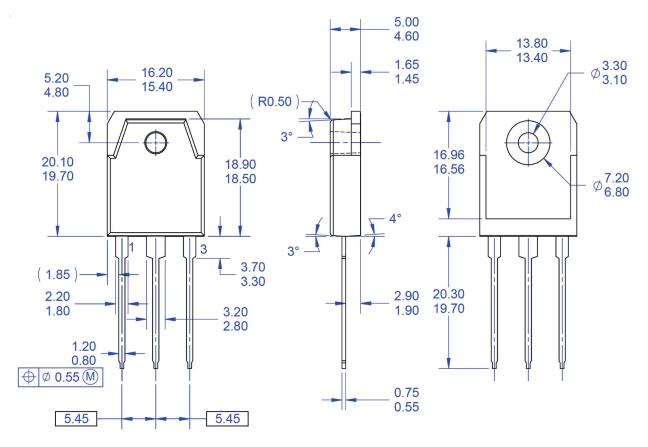
Same Type
as DUT

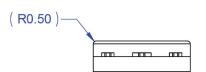
• dv/dt controlled by R_G
• l_{sD} controlled by pulse period

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions





NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.
 E) DRAWING FILE NAME: TO3PN03AREV1.
- F) FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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