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FCA76N60N N-Channel SupreMOS[®] MOSFET

600 V, 76 A, 36 m Ω

Features

- $R_{DS(on)}$ = 28 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 38 A
- Ultra Low Gate Charge (Typ. Q_g = 218 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 914 pF)
- 100% Avalanche Tested
- RoHS Compliant

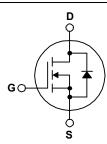
Application

- Solar Inverter
- AC-DC Power Supply

Description

The SupreMOS[®] MOSFET is ON Semiconductor's next generation of high voltage super-junction (SJ) technology employing a deep trench filling process that differentiates it from the conventional SJ MOSFETs. This advanced technology and precise process control provides lowest Rsp on-resistance, superior switching performance and ruggedness. SupreMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FCA76N60N	Unit	
V _{DSS}	Drain to Source Voltage			600	V	
V _{GSS}	Gate to Source Voltage			±30	V	
I _D	Drain Current	- Continuous (T _C = 25 ^o C)		76	^	
		- Continuous (T _C = 100 ^o C)		48.1	Α	
I _{DM}	Drain Current	- Pulsed (I	Note 1)	228	А	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		Note 2)	8022	mJ	
I _{AR}	Avalanche Current		Note 1)	76	А	
E _{AR}	Repetitive Avalanche Ener	rgy (I	Note 1)	5.40	mJ	
dv/dt	MOSFET dv/dt Ruggedness (Note 3)		Note 3)	100	Mag	
	Peak Diode Recovery dv/c	Diode Recovery dv/dt		12	V/ns	
P _D	Power Dissipation	$(T_{\rm C} = 25^{\rm o}{\rm C})$		543	W	
		- Derate Above 25°C		5.40	W/ ^o C	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C	
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300	°C	

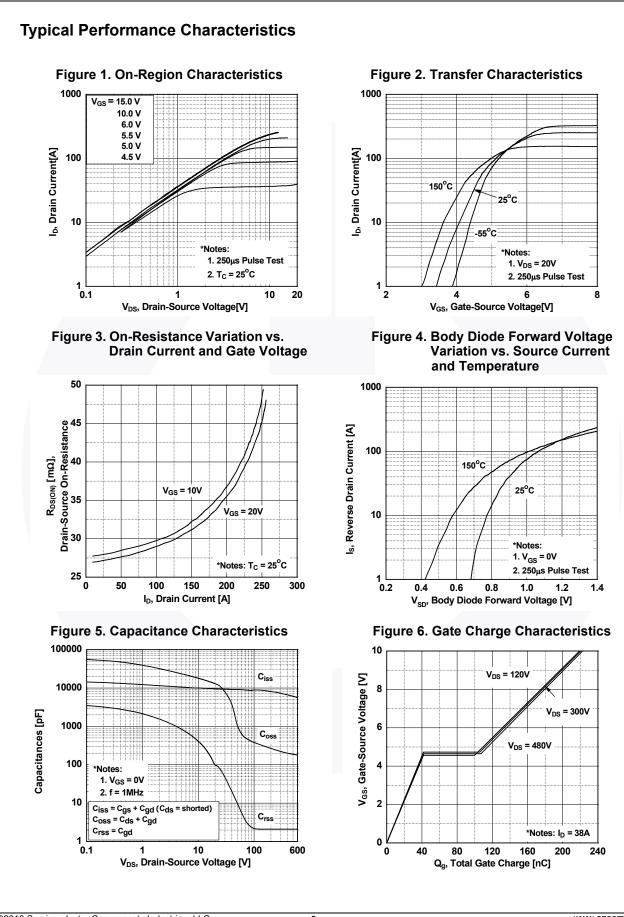
Thermal Characteristics

Symbol	Parameter	FCA76N60N	Unit
R_{\thetaJC}	Thermal Resistance, Junction to Case, Max.	0.23	°C/W
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	40	C/W

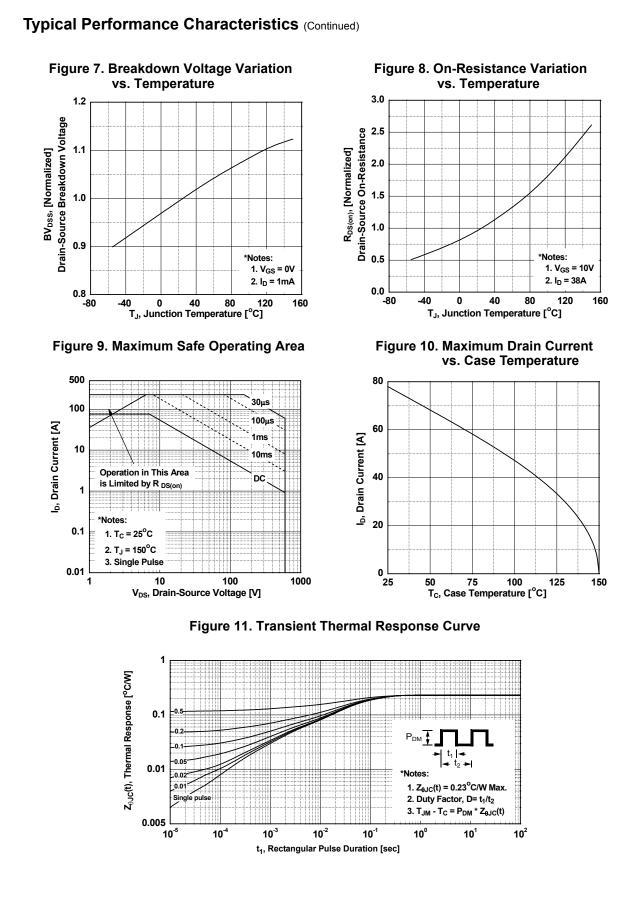
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FCA76N60N TO-3			N/A	20 1	inits
Parameter	ess otherwise noted.		IN/A	30 0	11113
Parameter	ess otherwise noted.				
			r	1	
	Test Conditions	Min.	Тур.	Max.	Unit
ristics					
rain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V,T _J = 25 ^o C	600	-	-	V
reakdown Voltage Temperature		_	0.73	_	V/°C
oefficient	5				V/ C
ero Gate Voltage Drain Current		-	-	10 100	μA
ente te Dedu Leekege Current		-			-
ate to Body Leakage Current	$v_{GS} = \pm 30 v, v_{DS} = 0 v$	-	-	±100	nA
istics					
ate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \ \mu A$	2.0	-	4.0	V
tatic Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 38 \text{ A}$	-	28.5	36.0	mΩ
orward Transconductance	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 38 \text{ A}$	-	88	-	S
ractoristics					
			0010	1000-	
	$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V},$				pF
	f = 1 MHz	-			pF
	$V_{-2} = 380 V V_{-2} = 0 V f = 1 MHz$	-		5.0	pF pF
		-		-	pr
		-	-	285	nC
ů.	V _{DS} = 380 V, I _D = 38 A,	-	39	-	nC
v	V _{GS} = 10 V	_		_	nC
5	, ,				Ω
			1.0	_	32
aracteristics					
urn-On Delay Time		-	34	78	ns
urn-On Rise Time	V_{DD} = 380 V, I _D = 38 A, V _{GS} = 10 V, R _G = 4.7 Ω		24	58	ns
urn-Off Delay Time			235	480	ns
urn-Off Fall Time	(Note 4)	-	32	74	ns
Diode Characteristics					
	ada Famuard Currant			76	۸
			-		A A
			-		V
•			613	-	ns
,				-	μC
	oefficient ero Gate Voltage Drain Current iate to Body Leakage Current fistics iate Threshold Voltage tatic Drain to Source On Resistance orward Transconductance iracteristics put Capacitance utput Capacitance utput Capacitance intervention ffective Output Capacitance otal Gate Charge at 10V ate to Source Gate Charge ate to Drain "Miller" Charge quivalent Series Resistance (G-S) aracteristics urn-On Delay Time urn-Off Delay Time urn-Off Fall Time Diode Characteristics aximum Continuous Drain to Source Di	oefficient $I_D = T MA, Referenced to 25°Cero Gate Voltage Drain CurrentV_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}vate to Body Leakage CurrentV_{GS} = 480 \text{ V}, V_{DS} = 0 \text{ V}iate to Body Leakage CurrentV_{GS} = 480 \text{ V}, V_{DS} = 0 \text{ V}isticsiate Threshold VoltageV_{GS} = 100 \text{ V}, V_{DS} = 0 \text{ V}iate Drain to Source On ResistanceV_{GS} = 10 \text{ V}, I_D = 38 \text{ A}invard TransconductanceV_{DS} = 20 \text{ V}, I_D = 38 \text{ A}invard TransconductanceV_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, I_D = 38 \text{ A}interceristicsinterceristicsinto CapacitanceV_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, I_D = 38 \text{ A}into CapacitanceV_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, I_D = 38 \text{ A}into CapacitanceV_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, I_D = 38 \text{ A}, V_{CS} = 10 \text{ V}into CapacitanceV_{DS} = 380 \text{ V}, I_D = 38 \text{ A}, V_{CS} = 10 \text{ V}into Source Gate ChargeV_{DS} = 380 \text{ V}, I_D = 38 \text{ A}, V_{CS} = 10 \text{ V}, V$	oefficientIDT MA, Referenced to 25°C-ero Gate Voltage Drain Current $V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}$ -vate to Body Leakage Current $V_{GS} = 480 \text{ V}, V_{DS} = 0 \text{ V}$ -istics $V_{GS} = 480 \text{ V}, V_{DS} = 0 \text{ V}$ -isticsiste Threshold Voltage $V_{GS} = 100 \text{ V}, V_{DS} = 0 \text{ V}$ -isticsvalue Threshold Voltage $V_{GS} = 100 \text{ V}, I_D = 38 \text{ A}$ -orward Transconductance $V_{DS} = 20 \text{ V}, I_D = 38 \text{ A}$ -inductance $V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ -isticsinture Capacitance $V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ -inture Capacitance $V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ -inture Capacitance $V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ -inture Capacitance $V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ -inture Capacitance $V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$ -ite to Drain "Miller" Charge $V_{DS} = 380 \text{ V}, I_D = 38 \text{ A}, f = 0 \text{ V}, GS = 10 \text{ V}$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $



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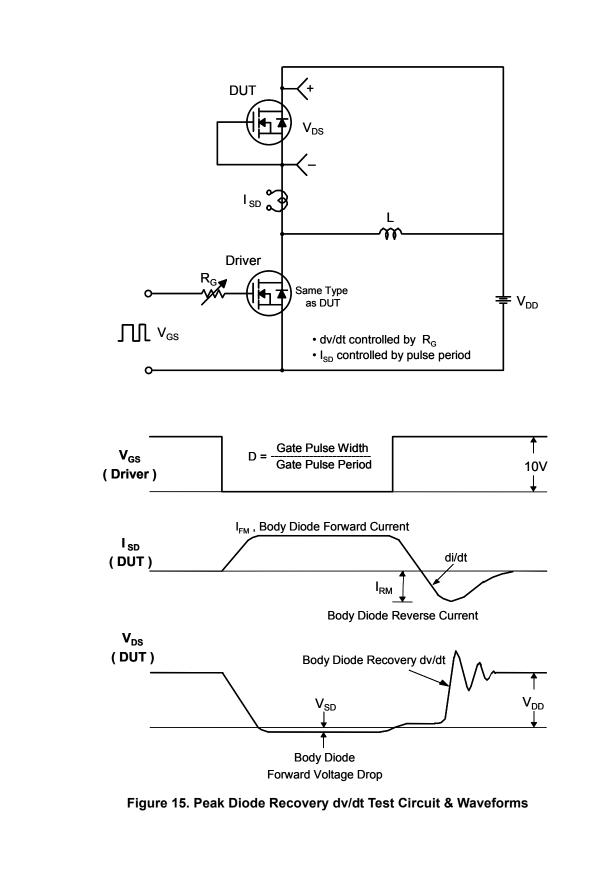


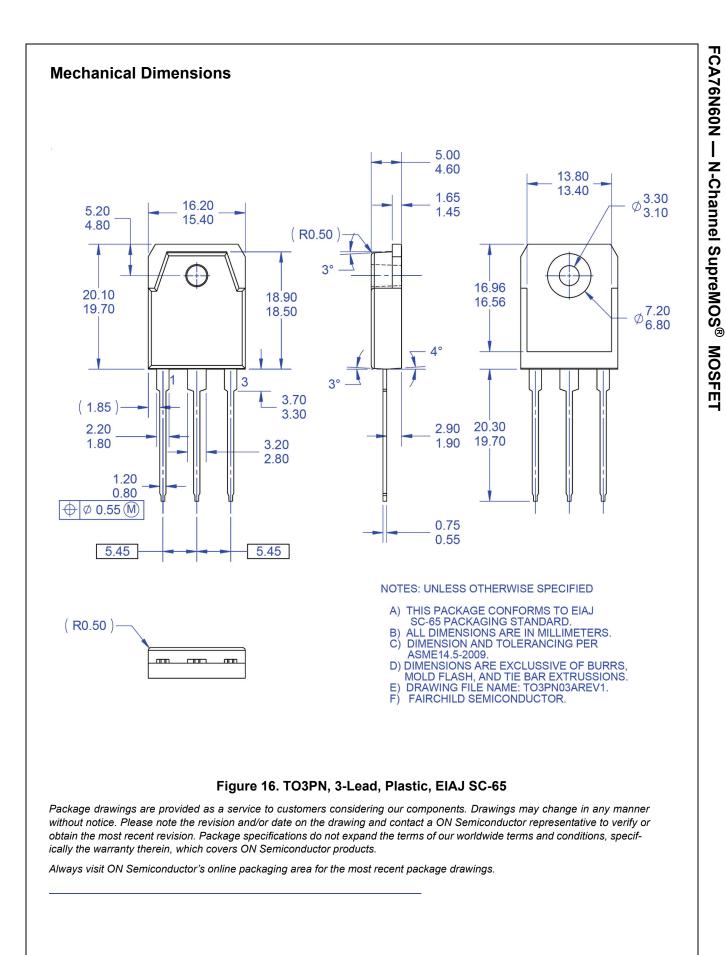
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 V_{GS} ξ ק Q_g V_{DS} Q_{gd} Q_{gs} DUT I_G = const. Charge Figure 12. Gate Charge Test Circuit & Waveform R VDS VDS 90% V_{DD} GS R_{G} 10% V_{GS} V_{GS} ∏ DUT 0 C Figure 13. Resistive Switching Test Circuit & Waveforms L $E_{AS} = \frac{1}{2} L I_{AS}^2$ V_{DS} $\mathsf{BV}_{\mathsf{DSS}}$ ID a AS R_{G} **∔** ∨_{DD} $I_D(t)$ V_{GS} $V_{DS}(t)$ V_{DD} DUT Time t_p Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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