

FCH040N65S3

MOSFET – Power, N-Channel, SUPERFET® III, Easy Drive

650 V, 65 A, 40 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 35.4\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 136\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 1154\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

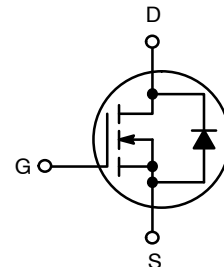
- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar



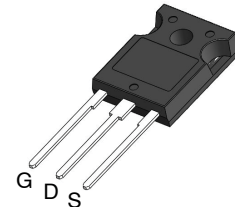
ON Semiconductor®

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V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	40 mΩ @ 10 V	65 A



POWER MOSFET



TO-247 LONG LEADS
CASE 340CH

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FCH040N65S3	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH040N65S3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	FCH040N65S3-F155	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±30
		- AC (f > 1 Hz)	±30
I _D	Drain Current	- Continuous (T _C = 25°C)	65
		- Continuous (T _C = 100°C)	41
I _{DM}	Drain Current	- Pulsed (Note 1)	162.5
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	358	mJ
I _{AS}	Avalanche Current (Note 2)	8.1	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	4.17	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	417
		- Derate Above 25°C	3.33
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. I_{AS} = 8.1 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 32.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH040N65S3-F155	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.3	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH040N65S3-F155	FCH040N65S3	TO-247 G03	Tube	N/A	N/A	30 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	-	-	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.64	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 520 V, T _C = 125°C	-	4.5	-	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 1.7 mA	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 32.5 A	-	35.4	40	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 32.5 A	-	46	-	S

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	–	4740	–	pF
C_{oss}	Output Capacitance		–	120	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	1154	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	171	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400\text{ V}, I_D = 32.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	–	136	–	nC
Q_{gs}	Gate to Source Gate Charge		–	33	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	59	–	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	–	0.7	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 32.5\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 3.3\ \Omega$ (Note 4)	–	35	–	ns
t_r	Turn-On Rise Time		–	51	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	95	–	ns
t_f	Turn-Off Fall Time		–	30	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current	–	–	65	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	162.5	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 32.5\text{ A}$	–	–	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 32.5\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$	–	534	–	ns
Q_{rr}	Reverse Recovery Charge		–	13.6	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

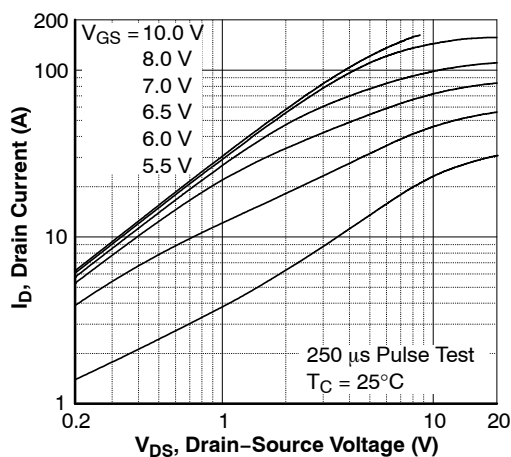


Figure 1. On-Region Characteristics

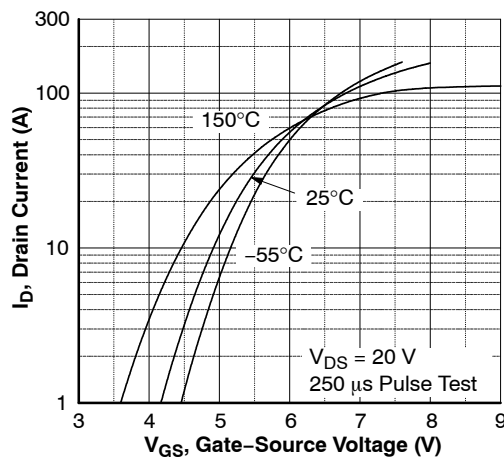


Figure 2. Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

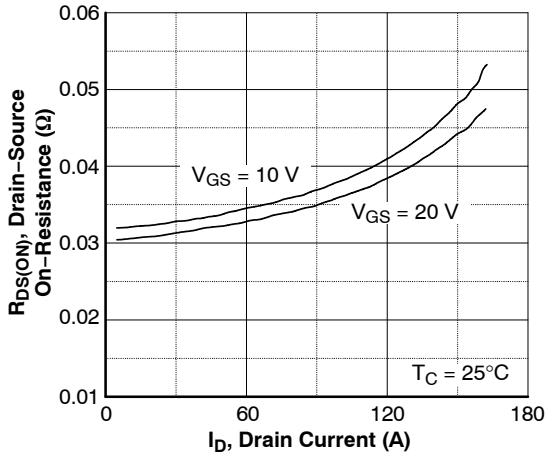


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

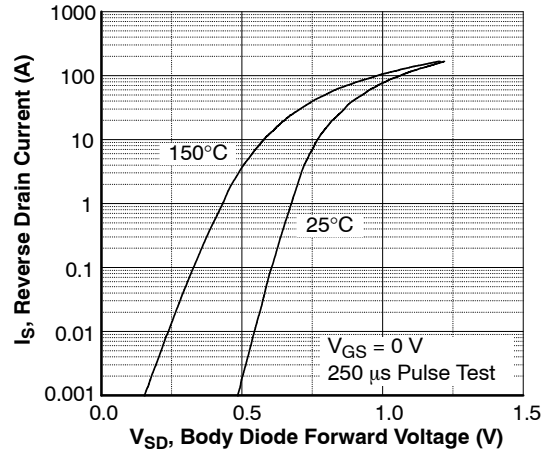


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

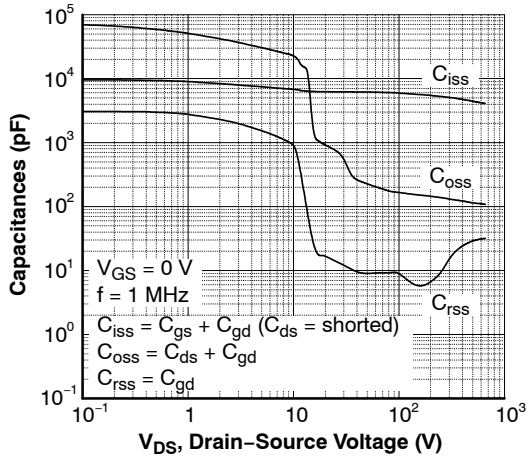


Figure 5. Capacitance Characteristics

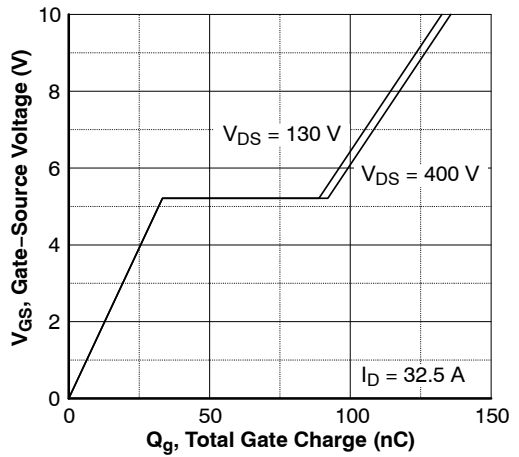


Figure 6. Gate Charge Characteristics

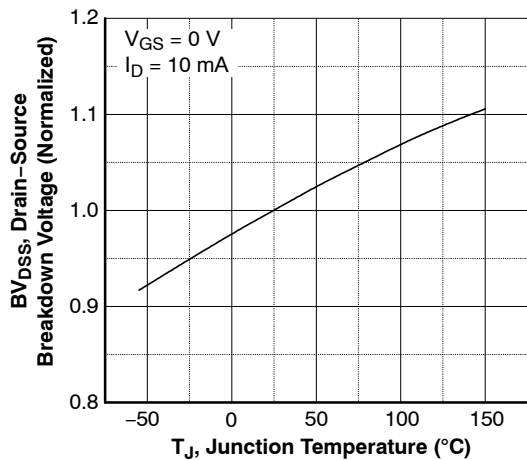


Figure 7. Breakdown Voltage Variation vs. Temperature

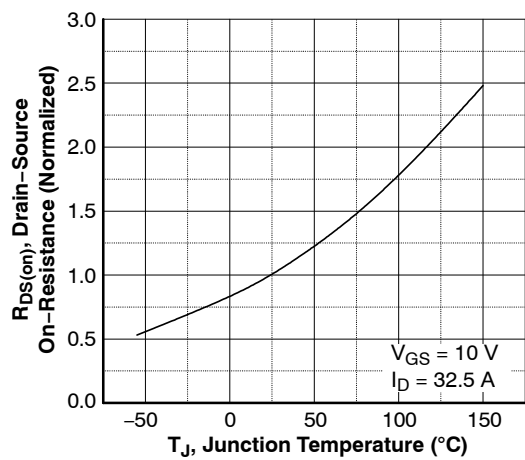


Figure 8. On-Resistance Variation vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

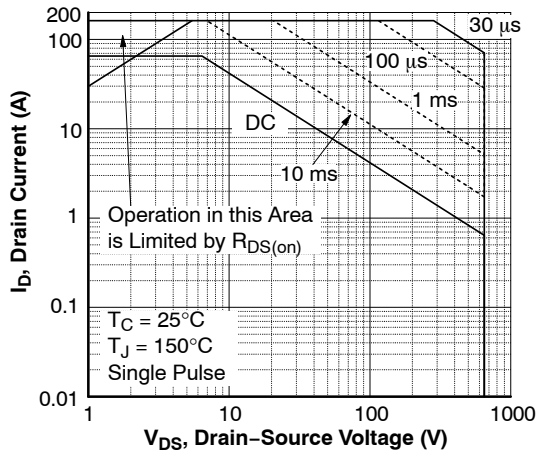


Figure 9. Maximum Safe Operating Area

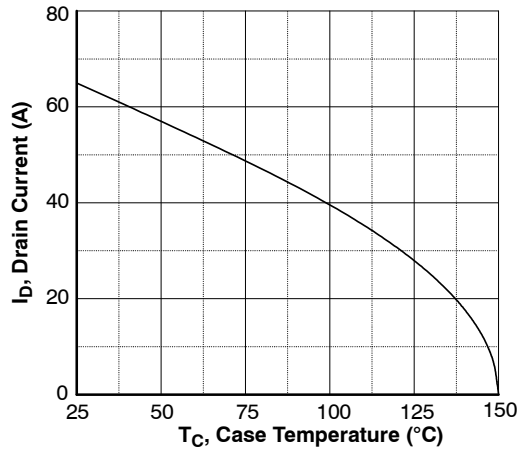


Figure 10. Maximum Drain Current vs. Case Temperature

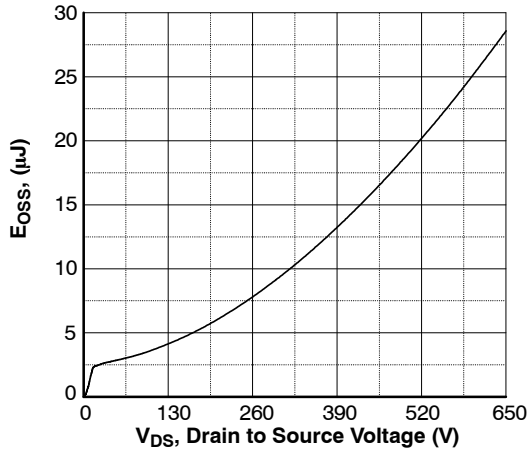


Figure 11. E_{OSS} vs. Drain to Source Voltage

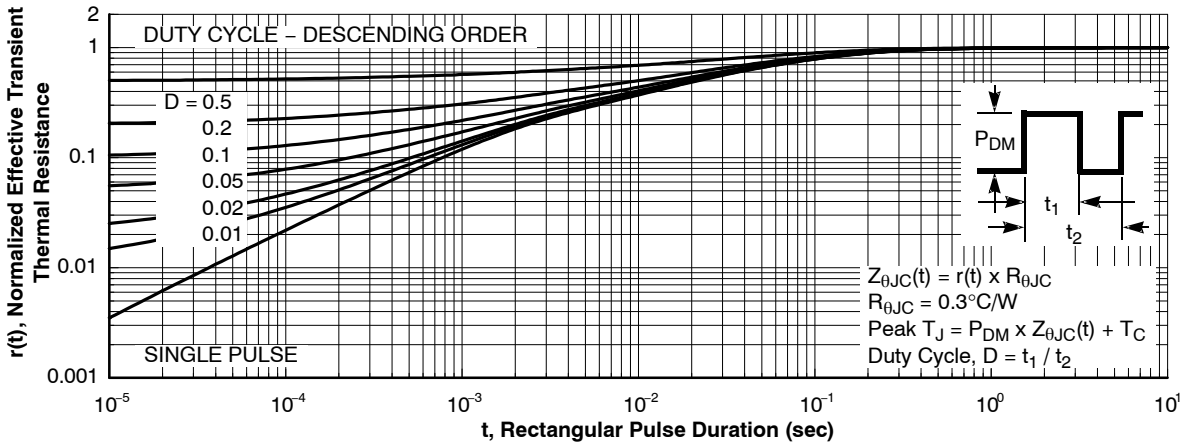


Figure 12. Transient Thermal Response Curve

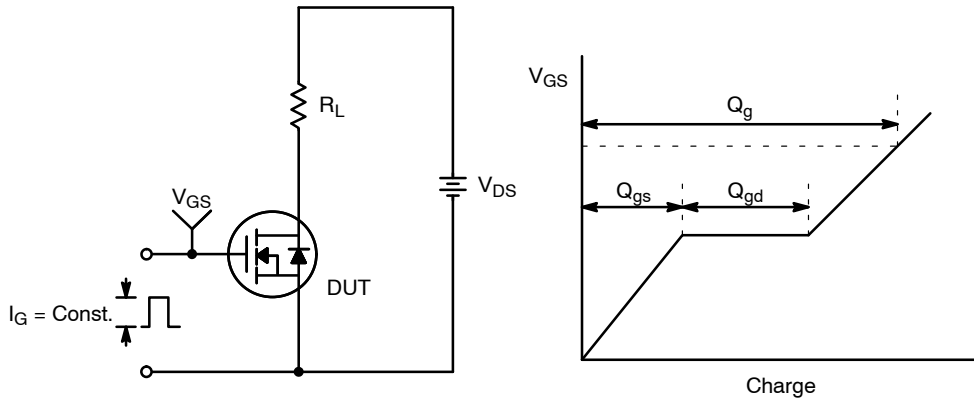


Figure 13. Gate Charge Test Circuit & Waveform

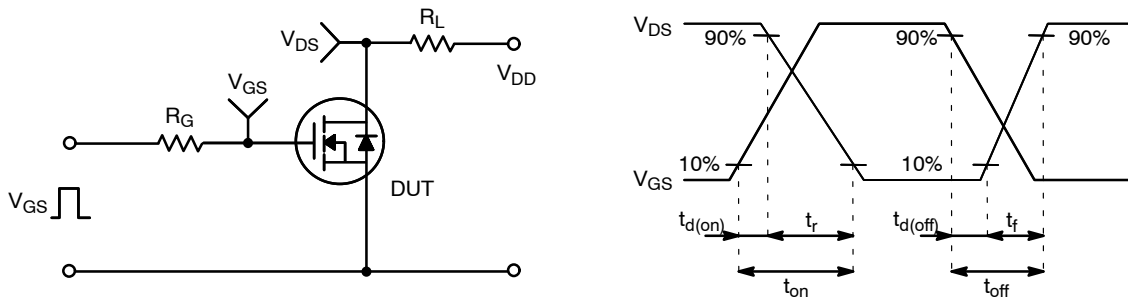


Figure 14. Resistive Switching Test Circuit & Waveforms

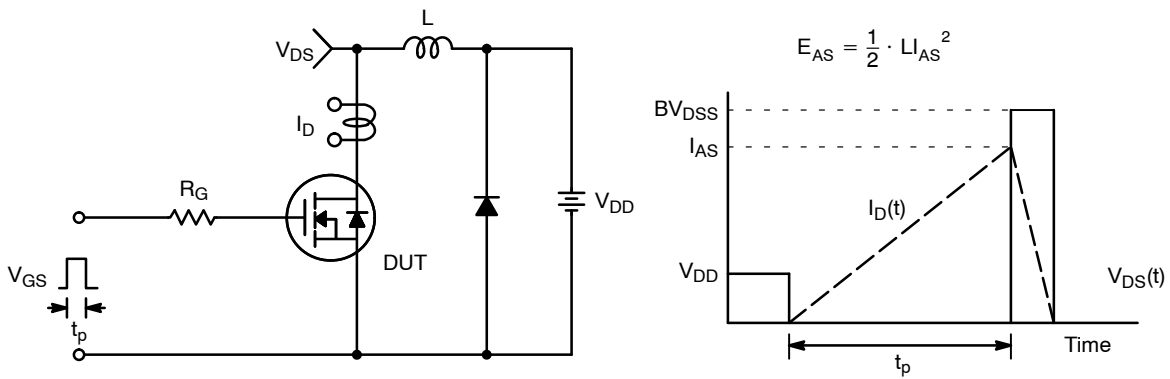


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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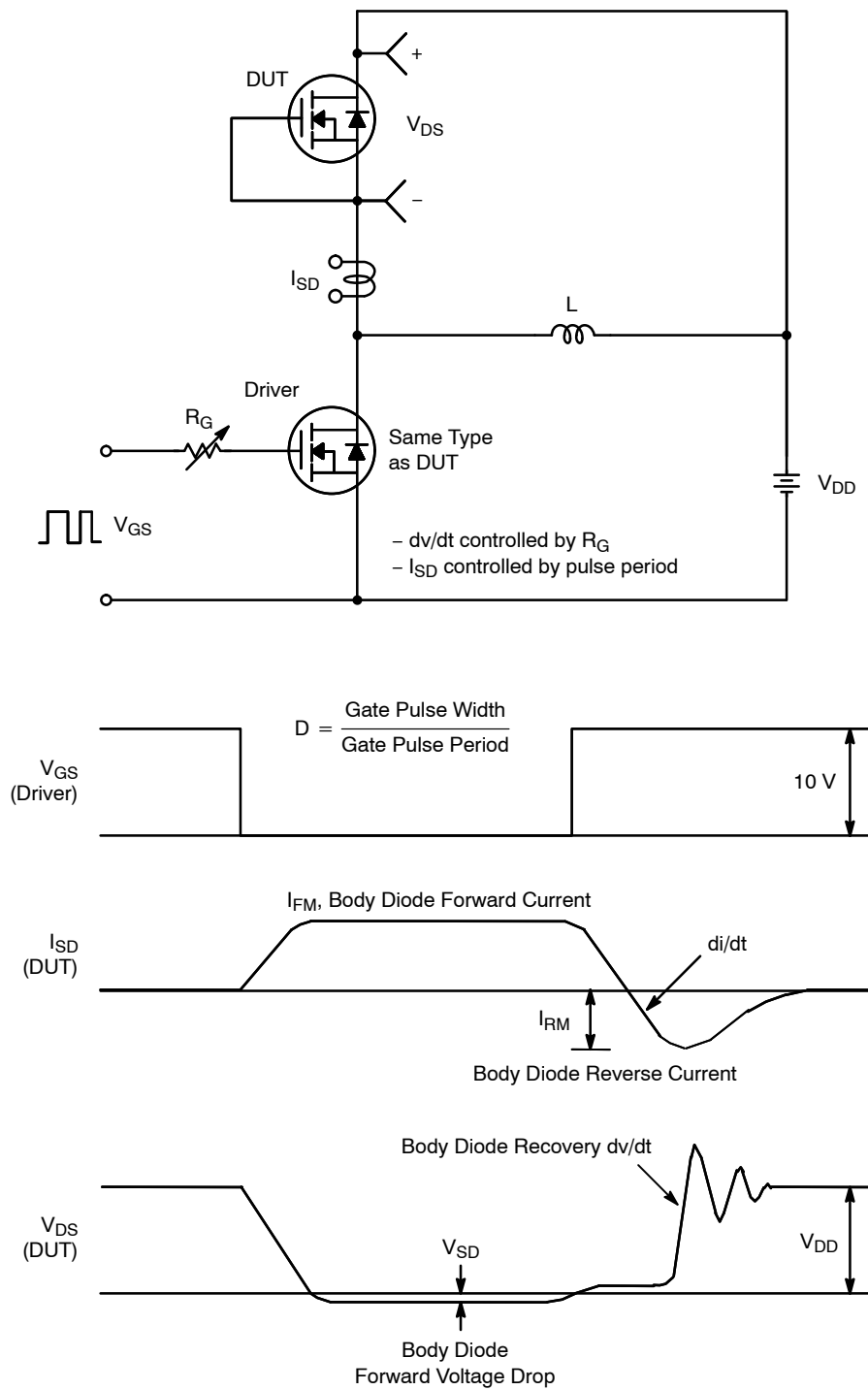


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CH
ISSUE A

DATE 09 OCT 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.29	2.475	2.66
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.61	6.73	6.85

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