MOSFET – N-Channel, SUPERFET II

600 V, 22 A, 170 m Ω

FCH170N60

Description

SUPERFET[®] II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SUPERFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.

Features

- $650 \text{ V} @ \text{T}_{\text{J}} = 150^{\circ}\text{C}$
- Typ. $R_{DS(on)} = 150 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 42 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 190 pF)
- 100% Avalanche Tested
- This Device is Pb–Free and is RoHS Compliant

Applications

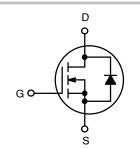
- Telecom / Server Power Supplies
- Industrial Power Supplies
- AC-DC Power Supply



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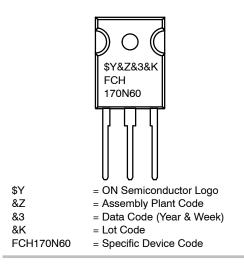
V _{DSS}	R _{DS(ON)} MAX	I _D MAX		
600 V	$170 \text{ m}\Omega$	22 A		



N-Channel MOSFET



MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol	Parameter	FCH170N60	Unit	
V _{DSS}	Drain to Source Voltage		600	V
V _{GSS}	Gate to Source Voltage	-DC	±20	V
		–AC (f > 1 Hz)	±30	
Ι _D	Drain Current	–Continuous (T _C = 25°C)	T _C = 25°C) 22	
		–Continuous (T _C = 100°C)	14	
I _{DM}	Drain Current	-Pulsed (Note 1)	66	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		525	mJ
I _{AR}	Avalanche Current (Note 1)	5	А	
E _{AR}	Repetitive Avalanche Energy (Note 1)	2.27	mJ	
dv/dt	MOSFET dv/dt (Note 3) Peak Diode Recovery dv/dt		100	V/ns
			20	
PD	Power Dissipation	(T _C = 25°C)	227	W
		-Derate Above 25°C	1.82	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		300	°C

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 5 \text{ A}$, $R_G = 25 \Omega$, Starting $T_J = 25^{\circ}\text{C}$. 3. $I_{SD} \le 11 \text{ A}$, di/dt $\le 200 \text{ A/}\mu\text{s}$, $V_{DD} \le 380 \text{ V}$, Starting $T_J = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH170N60	Unit
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case, Max.	0.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

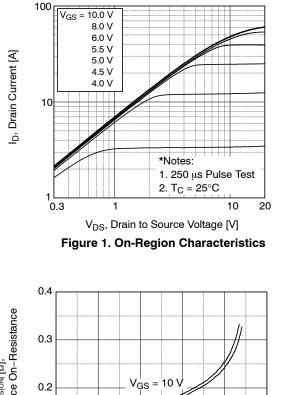
Part Number	Top Marking	Package	Reel Size	Tape Width	Quantity
FCH170N60	FCH170N60	TO-247	-	-	30 Units

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	ERISTICS	-				-
BV _{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C	600	-	-	V
		V_{GS} = 0 V, I _D = 10 mA, T _J = 150°C	650	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	-	0.67	_	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ
		V_{DS} = 480 V, V_{GS} = 0 V, T_{C} = 125°C	-	1.2	-	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA
ON CHARACTE	RISTICS	-				-
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 11 A	-	150	170	mΩ
9fs	Forward Transconductance	V _{DS} = 20 V, I _D = 11 A	-	17	-	S
DYNAMIC CHA	RACTERISTICS	•				
C _{iss}	Input Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	-	2150	2860	pF
C _{oss}	Output Capacitance		-	60	80	pF
C _{rss}	Reverse Transfer Capacitance		-	2.65	-	pF
C _{oss(eff.)}	Effective Output Capacitance	$V_{DS} = 0 \text{ V}$ to 480 V, $V_{GS} = 0 \text{ V}$	-	190	-	pF
Q _{g(tot)}	Total Gate Charge at 10 V	$V_{DS} = 380 \text{ V}, \text{ I}_{D} = 11 \text{ A}, \text{ V}_{GS} = 10 \text{ V}$	-	42	55	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)	-	9	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	11	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.95	-	Ω
SWITCHING CH	IARACTERISTICS	-				-
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 380 \text{ V}, \text{ I}_{D} = 11\text{ A},$	-	21	50	ns
t _r	Turn-On Rise Time	V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	-	12	35	ns
t _{d(off)}	Turn-Off Delay Time		-	55	120	ns
t _f	Turn-Off Fall Time		-	3.8	18	ns
DRAIN-SOURC	E- DIODE CHARACTERISTICS	-				-
۱ _S	Maximum Continuous Drain to Source Diode Forward Current			-	22	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	66	А
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \text{ I}_{SD} = 11 \text{ A}$	-	-	1.2	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 V, I_{SD} = 11 A,$	-	346	-	ns
Q _{rr}	Reverse Recovery Charge	dl _F /dt = 100 A/μs	-	6.2	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS



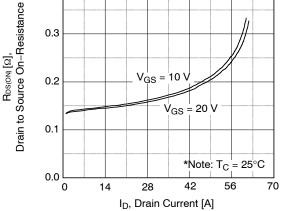


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

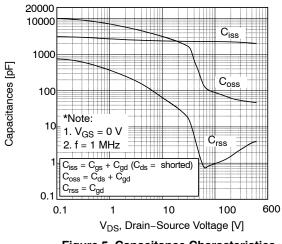
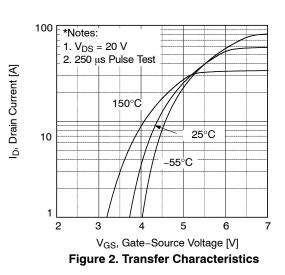


Figure 5. Capacitance Characteristics



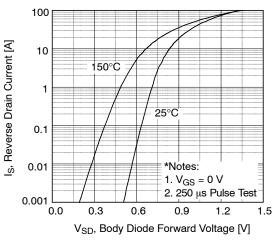
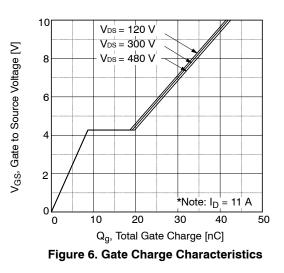
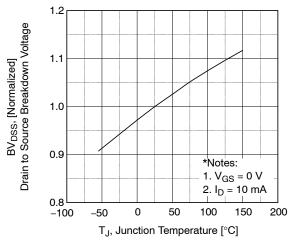
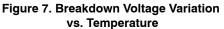


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)





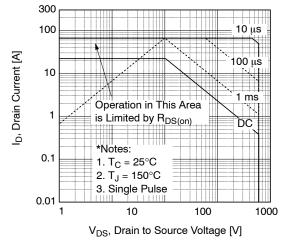
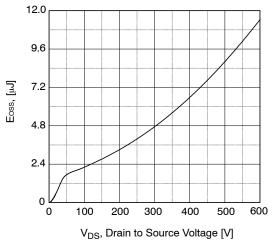


Figure 9. Maximum Safe Operation Area





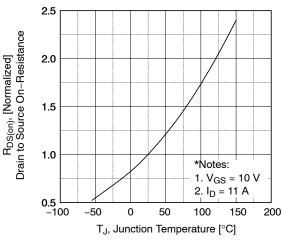
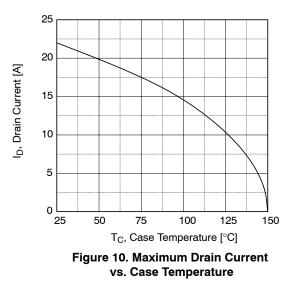


Figure 8. On-Resistance Variation vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

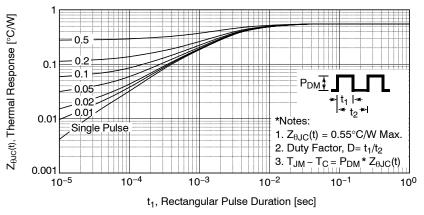
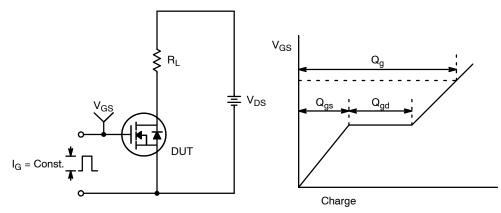
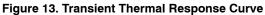


Figure 12. Transient Thermal Response Curve





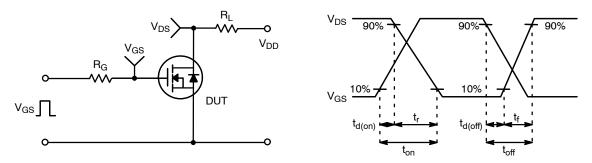


Figure 14. Resistive Switching Test Circuit & Waveforms

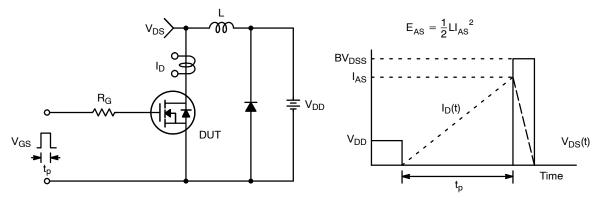


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

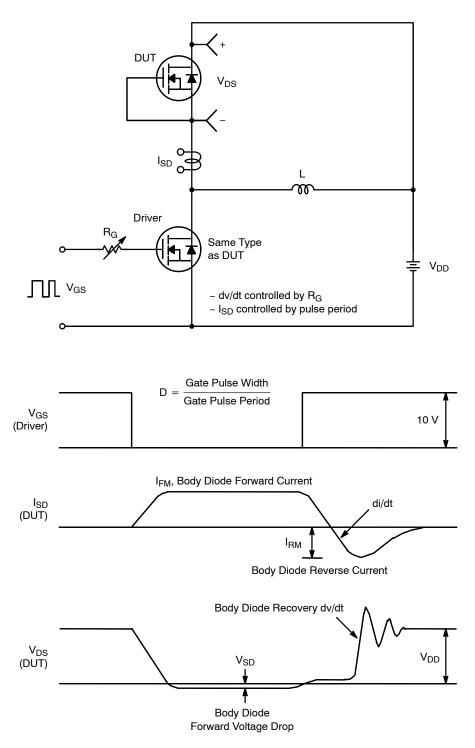


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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