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FAIRCHILD

June 2014

# FCP104N60

## N-Channel SuperFET® II MOSFET

### 600 V, 37 A, 104 mΩ

## Features

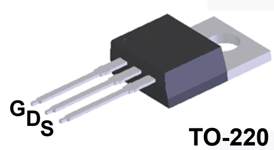
- 650 V @ $T_J$ = 150°C
- Typ. $R_{DS(on)}$ = 96 mΩ
- Ultra Low Gate Charge (Typ. $Q_g$ = 63 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 280 pF)
- 100% Avalanche Tested
- RoHS Compliant

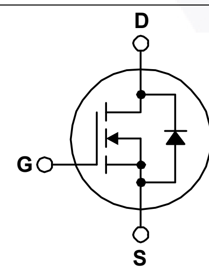
## Applications

- Telecom / Sever Power Supplies
- Industrial Power Supplies

## Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.




## Absolute Maximum Ratings $T_C$ = 25°C unless otherwise noted.

| Symbol | Parameter | | FCP104N60 | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | | 600 | V |
| $V_{GSS}$ | Gate to Source Voltage | - DC | ±20 | V |
| | | - AC (f > 1 Hz) | ±30 | |
| $I_D$ | Drain Current | - Continuous ($T_C$ = 25°C) | 37 | A |
| | | - Continuous ($T_C$ = 100°C) | 24 | |
| $I_{DM}$ | Drain Current | - Pulsed (Note 1) | 111 | A |
| $E_{AS}$ | Single Pulsed Avalanche Energy (Note 2) | | 809 | mJ |
| $I_{AR}$ | Avalanche Current (Note 1) | | 6.8 | A |
| $E_{AR}$ | Repetitive Avalanche Energy (Note 1) | | 3.57 | mJ |
| dv/dt | MOSFET dv/dt | | 100 | V/ns |
| | Peak Diode Recovery dv/dt (Note 3) | | 20 | |
| $P_D$ | Power Dissipation | ($T_C$ = 25°C) | 357 | W |
| | | - Derate Above 25°C | 2.85 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | FCP104N60 | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Max. | 0.35 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient, Max. | 40 | |

## Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|---|
| FCP104N60 | FCP104N60 | TO-220 | Tube | N/A | N/A | 50 units |

## Electrical Characteristics $T_C$ = 25°C unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 25°C | 600 | - | - | V |
| | | $V_{GS}$ = 0 V, $I_D$ = 10 mA, $T_J$ = 150°C | 650 | - | - | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 10 mA, Referenced to 25°C | - | 0.67 | - | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | - | - | 1 | μA |
| | | $V_{DS}$ = 480 V, $V_{GS}$ = 0 V, $T_C$ = 125°C | - | 1.98 | - | |
| $I_{GSS}$ | Gate to Body Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | - | - | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.5 | - | 3.5 | V |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 18.5 A | - | 96 | 104 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20 V, $I_D$ = 18.5 A | - | 33 | - | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 380 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 3130 | 4165 | pF |
| $C_{oss}$ | Output Capacitance | | - | 75 | 100 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 3.66 | - | pF |
| $C_{oss(eff.)}$ | Effective Output Capacitance | $V_{DS}$ = 0 V to 480 V, $V_{GS}$ = 0 V | - | 280 | - | pF |
| $Q_{g(tot)}$ | Total Gate Charge at 10V | $V_{DS}$ = 380 V, $I_D$ = 18.5 A, $V_{GS}$ = 10 V (Note 4) | - | 63 | 82 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | - | 14 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | - | 15 | - | nC |
| ESR | Equivalent Series Resistance | f = 1 MHz | - | 0.97 | - | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 380 V, $I_D$ = 18.5 A, $V_{GS}$ = 10 V, $R_g$ = 4.7 Ω (Note 4) | - | 26 | 62 | ns |
| $t_r$ | Turn-On Rise Time | | - | 18 | 46 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 72 | 154 | ns |
| $t_f$ | Turn-Off Fall Time | | - | 3.3 | 17 | ns |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 37 | A |
| $I_{SM}$ | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 114 | A |
| $V_{SD}$ | Drain to Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 18.5 A | - | - | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_{SD}$ = 18.5 A, $dI_F/dt$ = 100 A/μs | - | 414 | - | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | - | 8.8 | - | μC |

**Notes:**

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS}$ = 6.8 A, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 18.5 A, di/dt ≤ 200 A/μs, $V_{DD}$ ≤ 380 V, Starting $T_J$ = 25°C
4. Essentially independent of operating temperature.

## Typical Performance Characteristics

**Figure 1. On-Region Characteristics**

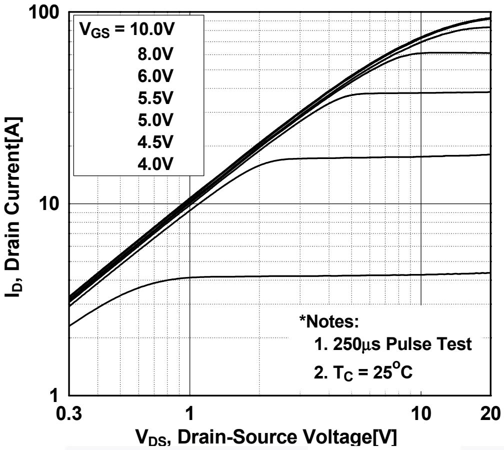



**Figure 2. Transfer Characteristics**

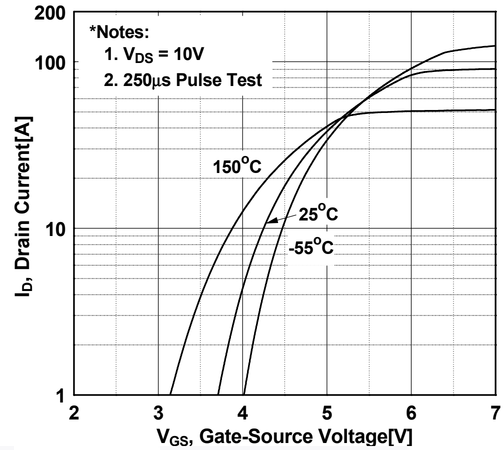



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

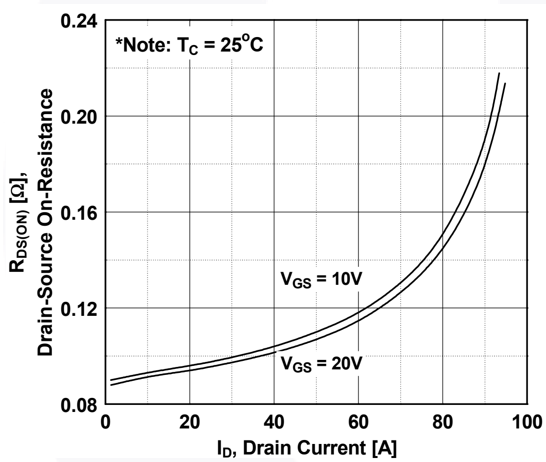



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

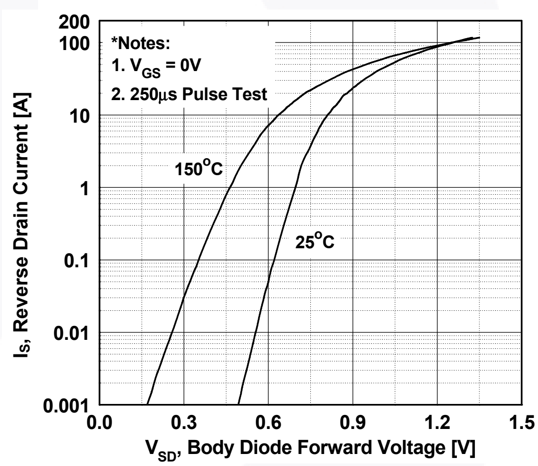



**Figure 5. Capacitance Characteristics**

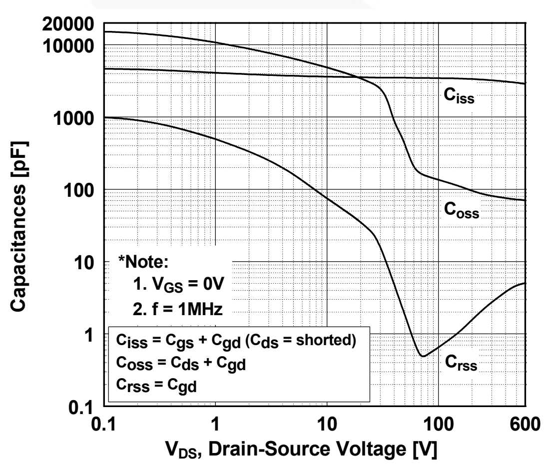
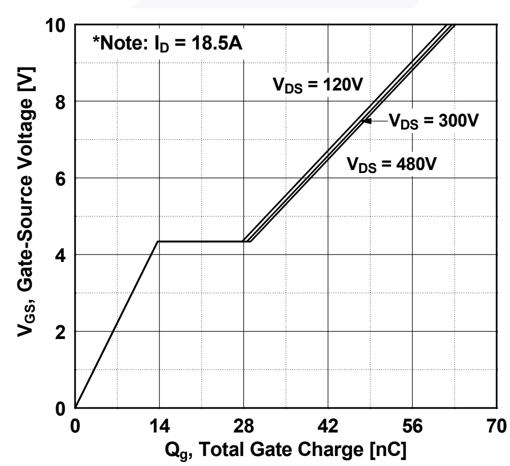



**Figure 6. Gate Charge Characteristics**



## Typical Performance Characteristics (Continued)

**Figure 7. Breakdown Voltage Variation vs. Temperature**

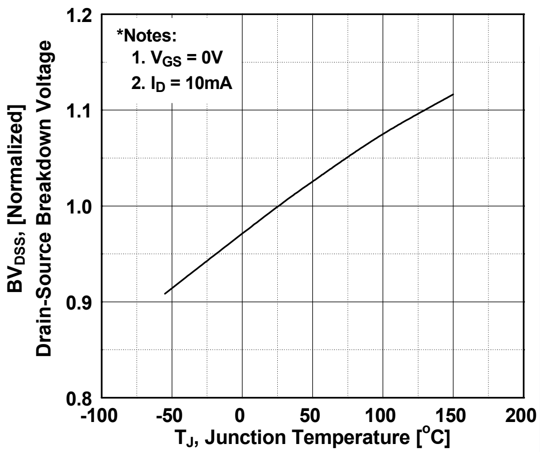



**Figure 8. On-Resistance Variation vs. Temperature**

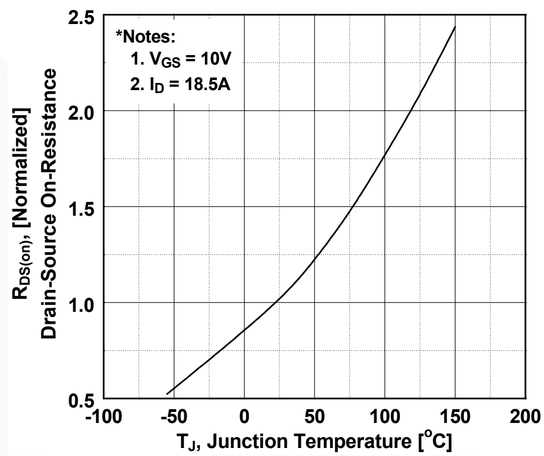



**Figure 9. Maximum Safe Operating Area**

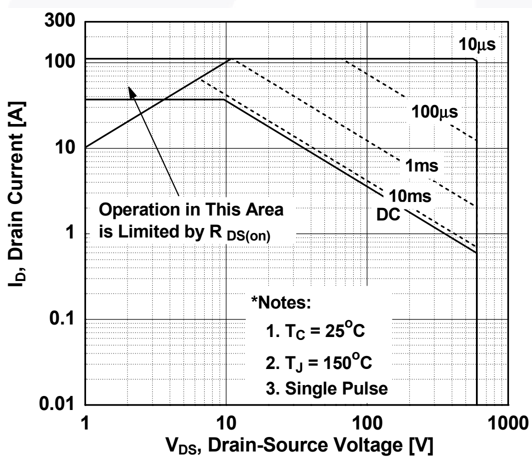



**Figure 10. Maximum Drain Current vs. Case Temperature**

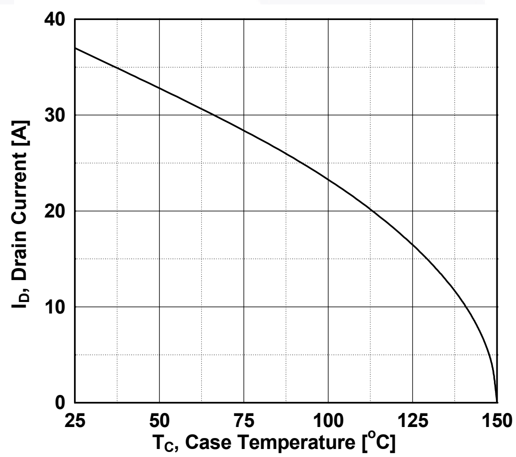
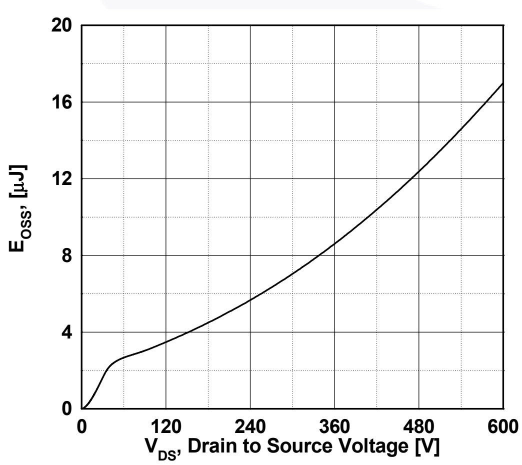



**Figure 11. Eoss vs. Drain to Source Voltage**



## Typical Characteristics (Continued)

**Figure 12. Transient Thermal Response Curve**

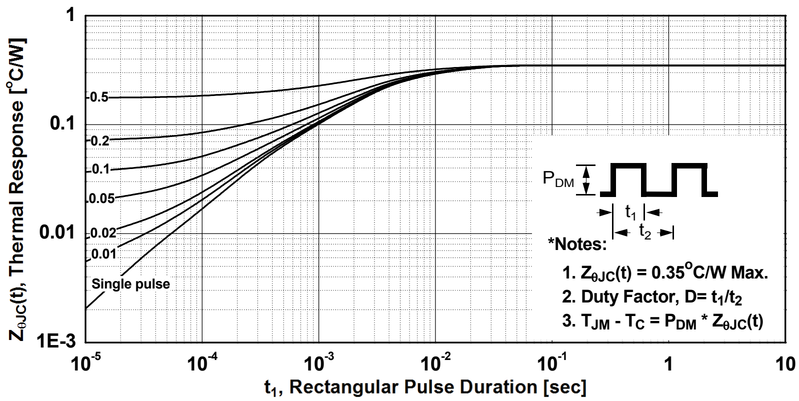


**Figure 13. Gate Charge Test Circuit & Waveform**

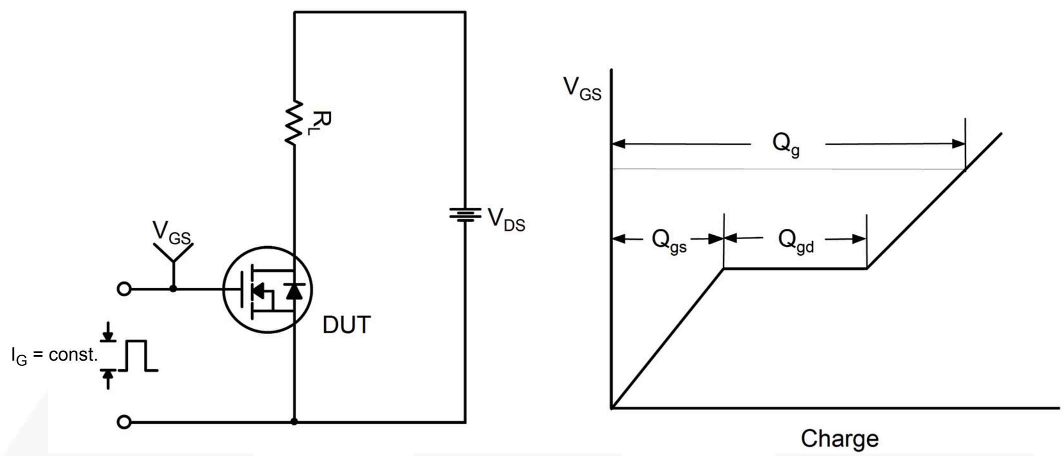



**Figure 14. Resistive Switching Test Circuit & Waveforms**

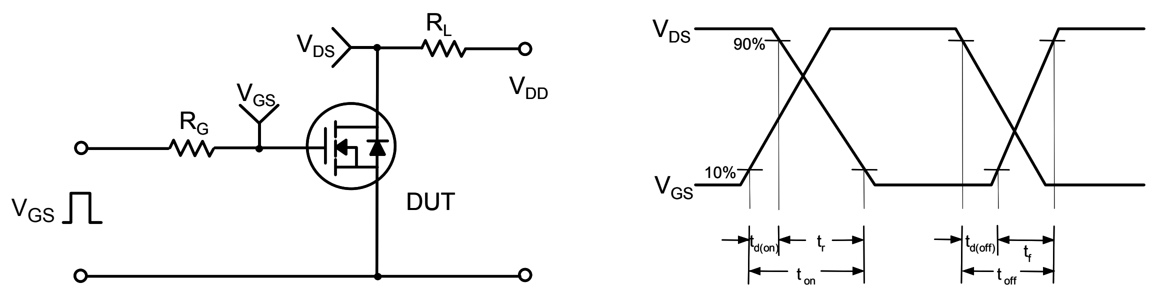



**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**

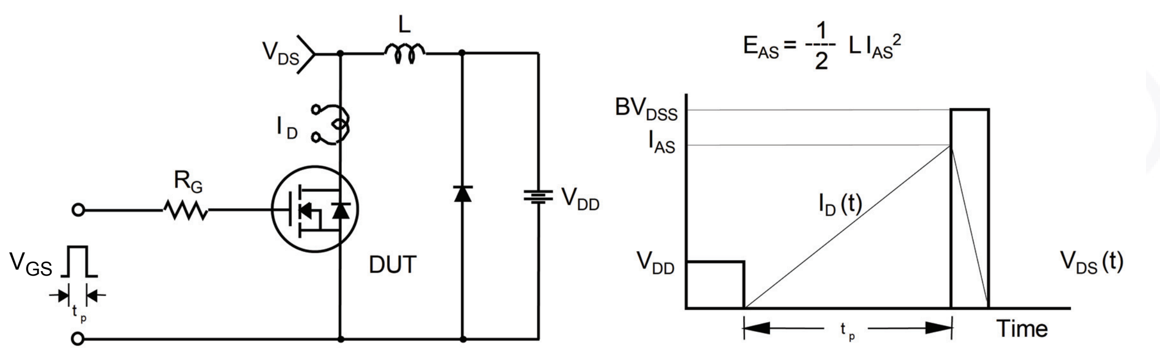
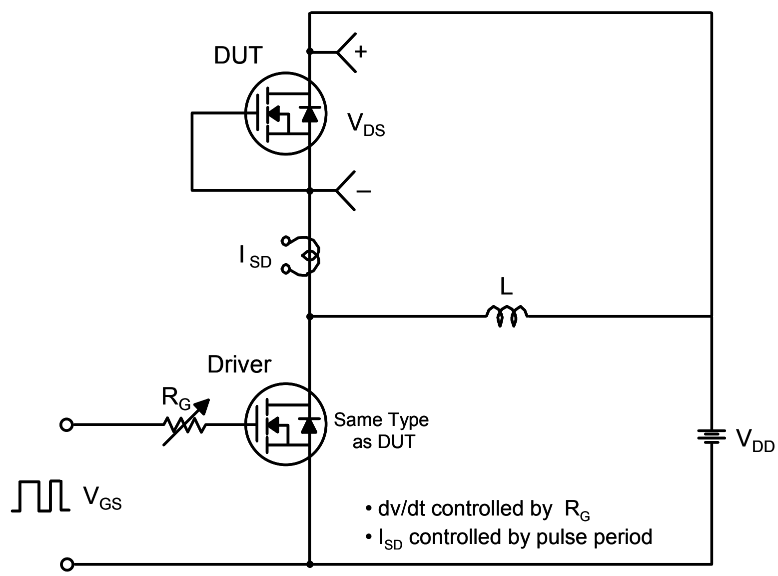
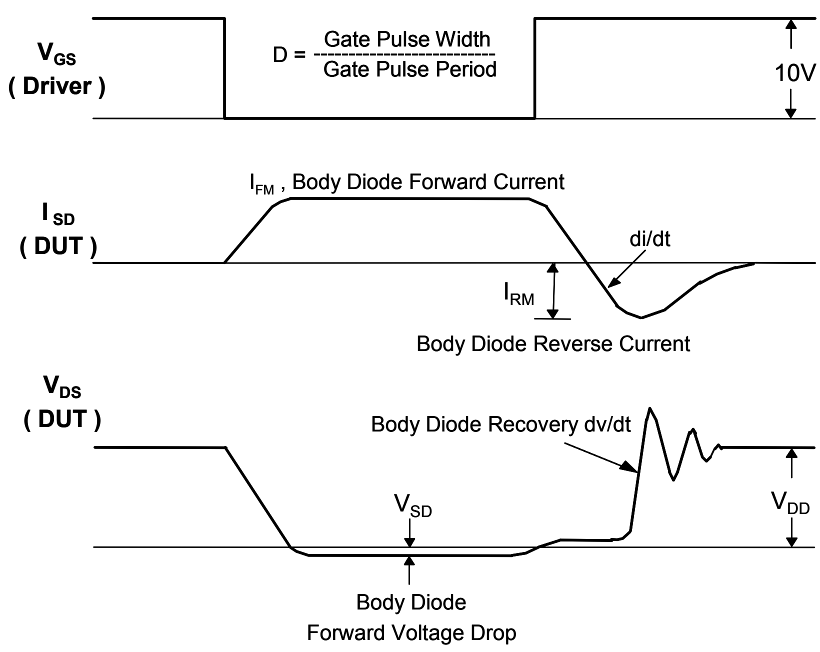
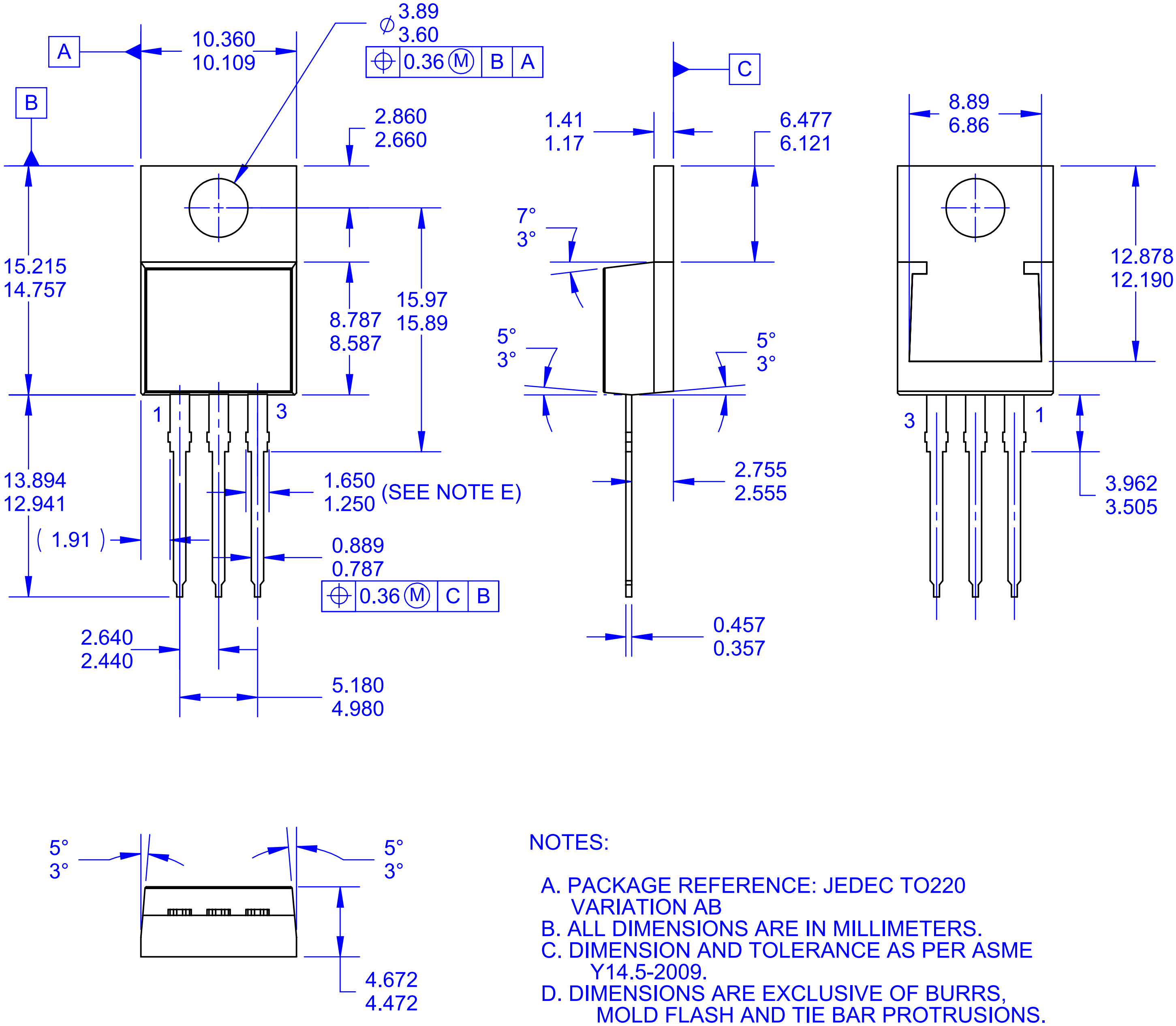


**Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms**






NOTES:

A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. MAX WIDTH FOR F102 DEVICE = 1.35mm.
F. DRAWING FILE NAME: TO220T03REV4.
G. FAIRCHILD SEMICONDUCTOR.

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