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#### FCP104N60

#### June 2014

# N-Channel SuperFET® II MOSFET

**600 V, 37 A, 104 m**Ω

#### **Features**

- 650 V @ T<sub>J</sub> = 150°C
- Typ.  $R_{DS(on)}$  = 96 m $\Omega$
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 63 nC)
- Low Effective Output Capacitance (Typ. Coss(eff.) = 280 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

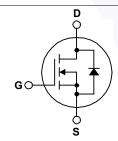
#### **Applications**

- · Telecom / Sever Power Supplies
- · Industrial Power Supplies

#### Description

SuperFET<sup>®</sup> II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.





#### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter			FCP104N60	Unit
$V_{DSS}$	Drain to Source Voltage			600	V
V <sub>GSS</sub>	Cata ta Sauraa Valtaga	- DC		±20	V
	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	_ v
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	/	37	^
	Drain Current	- Continuous (T <sub>C</sub> = 100°C)		24	A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	111	Α
E <sub>AS</sub>	Single Pulsed Avalanche Energy		(Note 2)	809	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	6.8	Α
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	3.57	mJ
	MOSFET dv/dt		100	1//	
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
D.	Davis Diagination	$(T_C = 25^{\circ}C)$		357	W
$P_{D}$	Power Dissipation  - Derate Above 25°C			2.85	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range			-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for S	oldering, 1/8" from Case for 5 Se	conds	300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FCP104N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	°C/VV

## **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP104N60	FCP104N60	TO-220	Tube	N/A	N/A	50 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
	Drain to Source Breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
1	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	1	1.98	-	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.5	-	3.5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18.5 A	-	96	104	mΩ
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 18.5 A	-	33	-	S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 200 V V 0 V	-	3130	4165	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 380 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	75	100	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 1 1 1 1 1 2	-\	3.66	-	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	$V_{DS}$ = 0 V to 480 V, $V_{GS}$ = 0 V	-	280	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 380 V, I <sub>D</sub> = 18.5 A,	- \	63	82	nC
$Q_{gs}$	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V	-	14	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(Note 4)	-	15	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.97	-	Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	26	62	ns
t <sub>r</sub>		$V_{DD} = 380 \text{ V}, I_D = 18.5 \text{ A},$	-	18	46	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_g$ = 4.7 $\Omega$	-	72	154	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	_	3.3	17	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	37	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	114	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 18.5 A	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 18.5 A,	-	414	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	8.8	-	μС

#### Notes:

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2.  $I_{AS}$  = 6.8 A,  $R_{G}$  = 25  $\Omega$ , Starting  $T_{J}$  = 25°C
- 3. I  $_{SD}$   $\leq$  18.5 A, di/dt  $\leq$  200 A/ $\mu$ s, V  $_{DD}$   $\leq$  380 V, Starting T  $_{J}$  = 25°C
- 4. Essentially independent of operating temperature.

#### **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

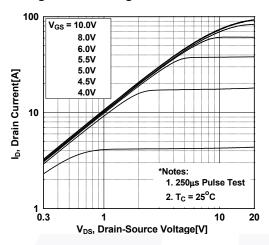


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

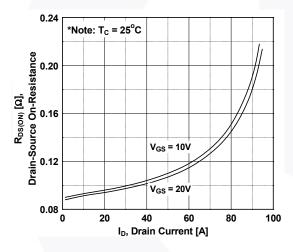


Figure 5. Capacitance Characteristics

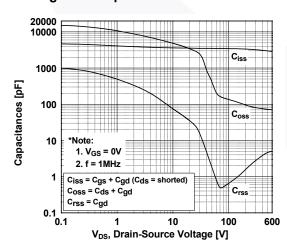


Figure 2. Transfer Characteristics

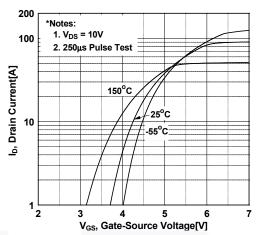


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

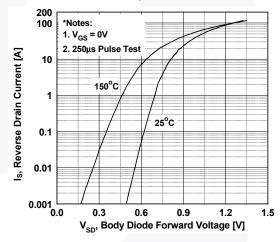
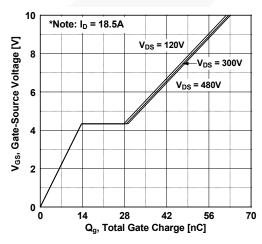


Figure 6. Gate Charge Characteristics



#### **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

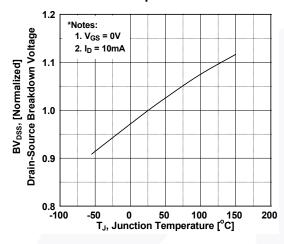


Figure 9. Maximum Safe Operating Area

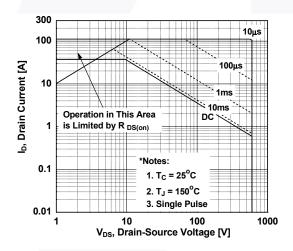


Figure 11. Eoss vs. Drain to Source Voltage

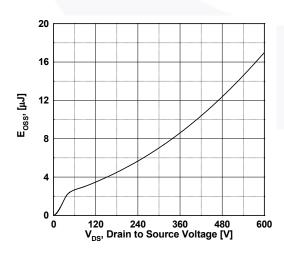


Figure 8. On-Resistance Variation vs. Temperature

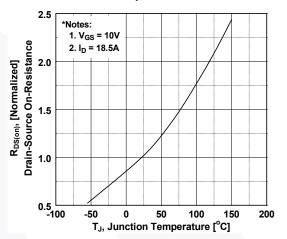
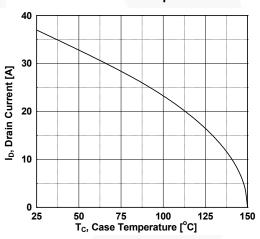


Figure 10. Maximum Drain Current vs. Case Temperature



## **Typical Characteristics** (Continued)

Figure 12. Transient Thermal Response Curve

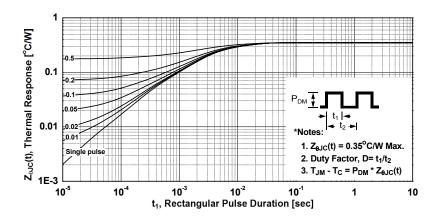


Figure 13. Gate Charge Test Circuit & Waveform

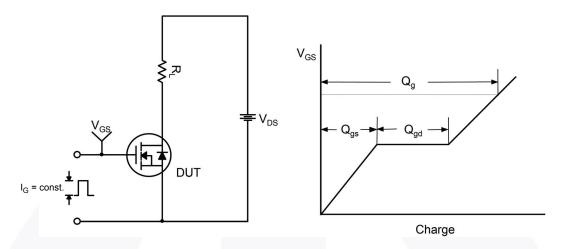


Figure 14. Resistive Switching Test Circuit & Waveforms

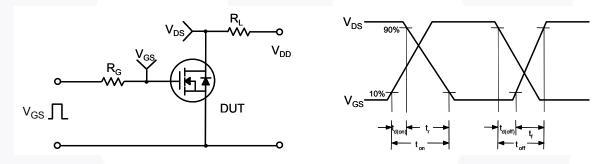
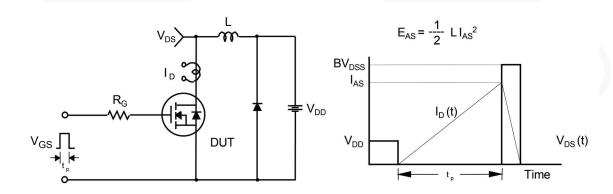


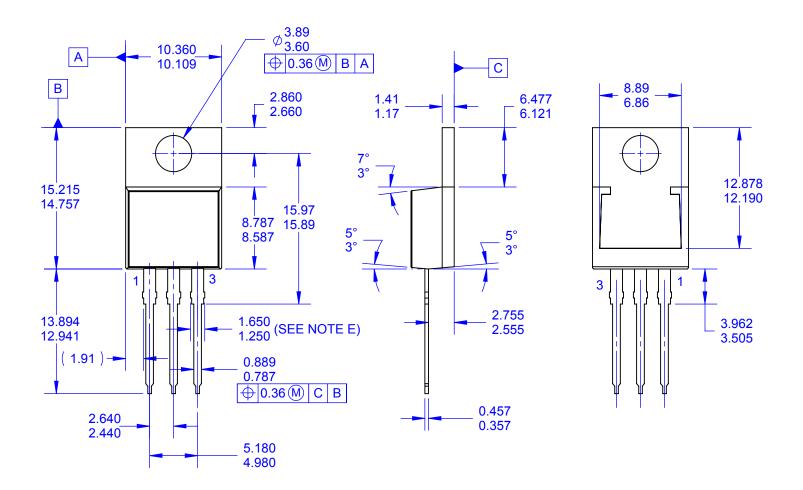
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

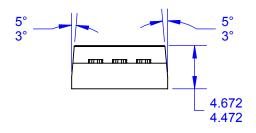


DUT Driver Same Type as DUT  $V_{DD}$  $\bullet$  dv/dt controlled by  $R_G$ • I<sub>SD</sub> controlled by pulse period Gate Pulse Width  $\mathbf{V}_{\mathbf{GS}}$ Gate Pulse Period 10V (Driver) I<sub>FM</sub> , Body Diode Forward Current I<sub>SD</sub> di/dt (DUT) **Body Diode Reverse Current** V<sub>DS</sub> (DUT) Body Diode Recovery dv/dt

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Body Diode Forward Voltage Drop





#### NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 **VARIATION AB**
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm. F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.

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