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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

December 2015

FCP290N80

N-Channel SuperFET® II MOSFET

800 V, 17 A, 0.29 Ω

Features

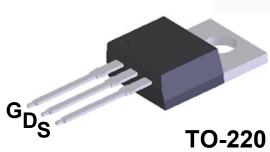
- Typ. $R_{DS(on)}$ = 0.245 Ω
- Ultra Low Gate Charge (Typ. Q_g = 58 nC)
- Low E_{oss} (Typ. 5.6 uJ @ 400 V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 240 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

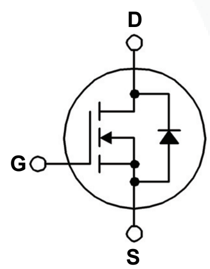
- AC-DC Power Supply
- LED Lighting

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



TO-220



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCP290N80	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC (f >1 Hz)	±30	
I_D	Drain Current	- Continuous (T_C = 25°C)	17	A
		- Continuous (T_C = 100°C)	10.8	
I_{DM}	Drain Current	- Pulsed (Note 1)	42	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	882	mJ
I_{AR}	Avalanche Current	(Note 1)	3.4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	2.12	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt	(Note 3)	20	
P_D	Power Dissipation	(T_C = 25°C)	212	W
		- Derate Above 25°C	1.7	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCP290N80	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.59	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP290N80	FCP290N80	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	-	0.8	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 640 V, T_C = 125°C	-	-	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 1.7 mA	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8.5 A	-	0.245	0.290	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 8.5 A	-	20	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	2410	3205	pF
C_{oss}	Output Capacitance		-	75	100	pF
C_{rss}	Reverse Transfer Capacitance		-	0.36	-	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	-	35	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	240	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 640 V, I_D = 17 A, V_{GS} = 10 V (Note 4)	-	58	75	nC
Q_{gs}	Gate to Source Gate Charge		-	11	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	22	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.75	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	-	22	54	ns
t_r	Turn-On Rise Time		-	14	38	ns
$t_{d(off)}$	Turn-Off Delay Time		-	61	132	ns
t_f	Turn-Off Fall Time		-	2.6	15	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	17	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	42	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 17 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 17 A, dI_F/dt = 100 A/μs	-	511	-	ns
Q_{rr}	Reverse Recovery Charge		-	12	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 3.4 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le$ 17 A, di/dt $\le$ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

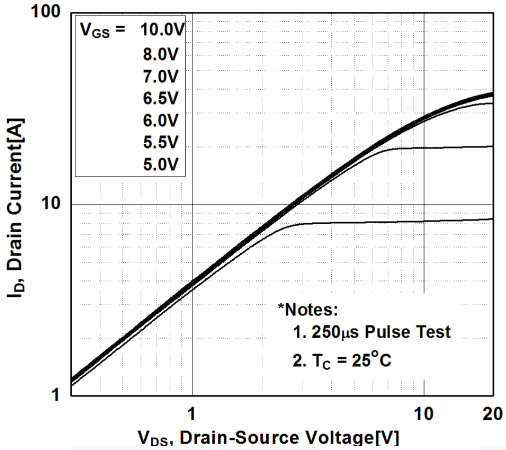


Figure 2. Transfer Characteristics

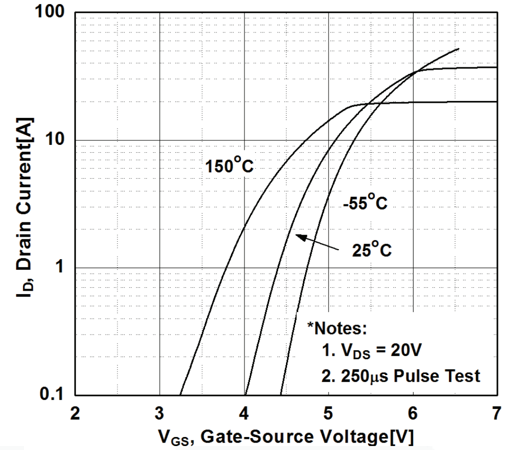


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

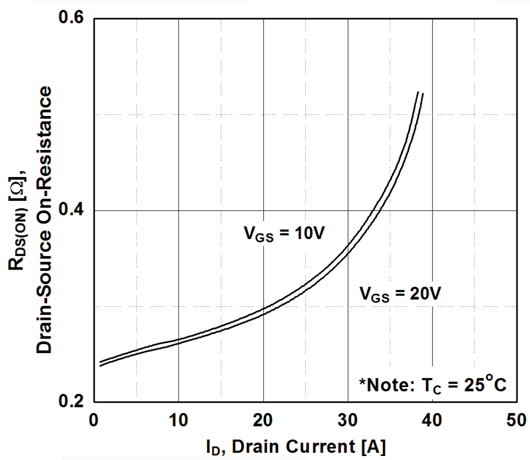


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

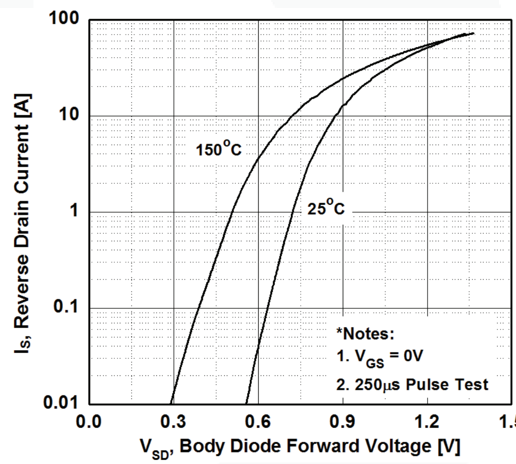


Figure 5. Capacitance Characteristics

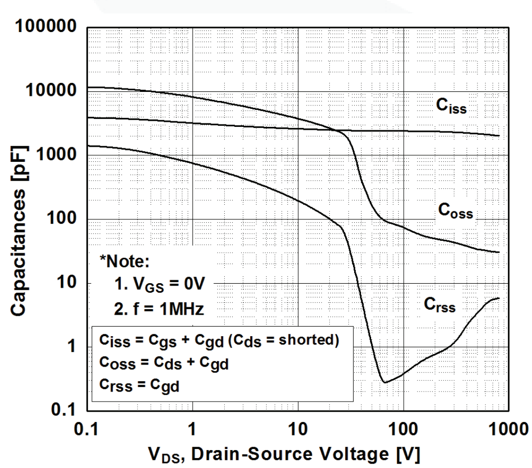
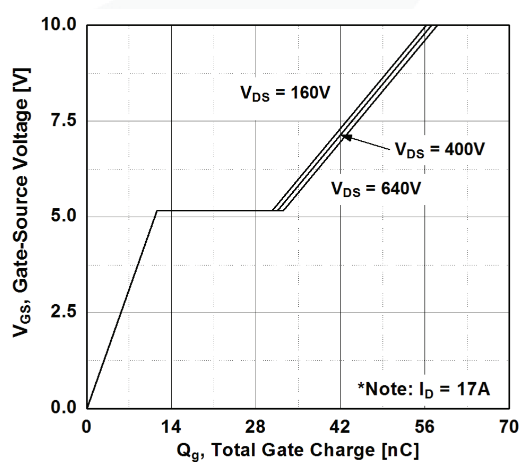


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

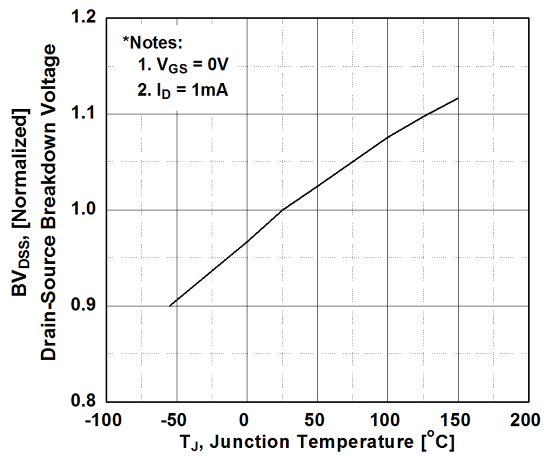


Figure 8. On-Resistance Variation vs. Temperature

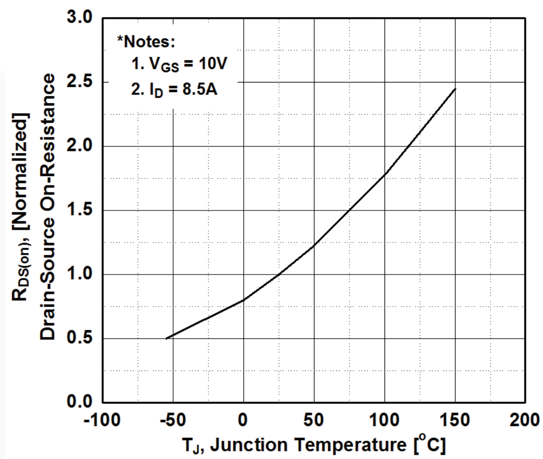


Figure 9. Maximum Safe Operating Area

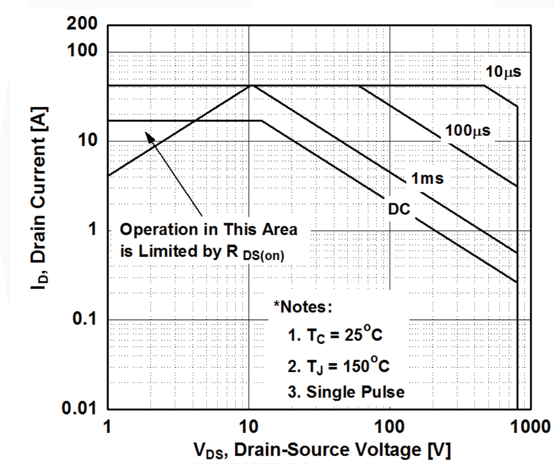


Figure 10. Maximum Drain Current vs. Case Temperature

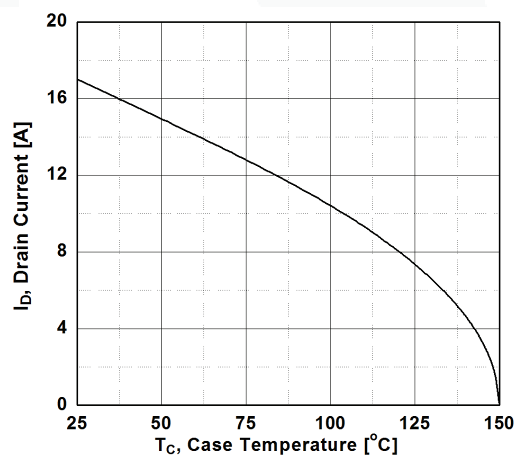
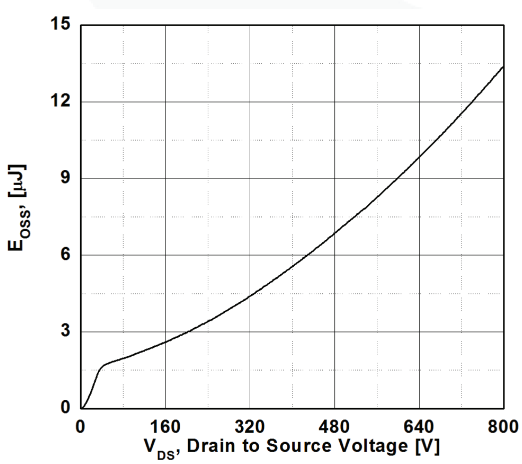
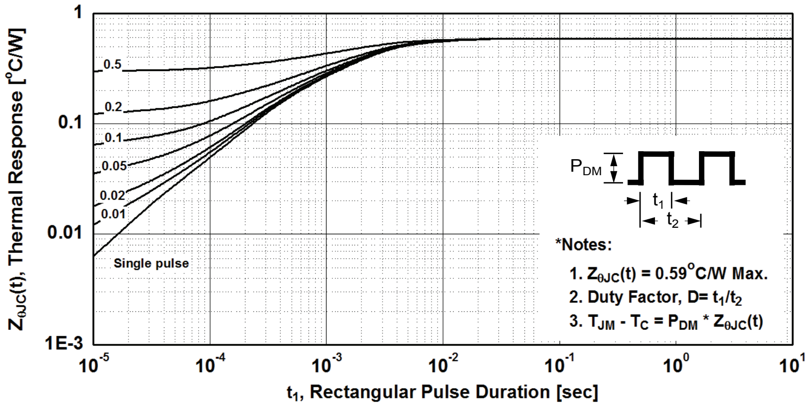


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



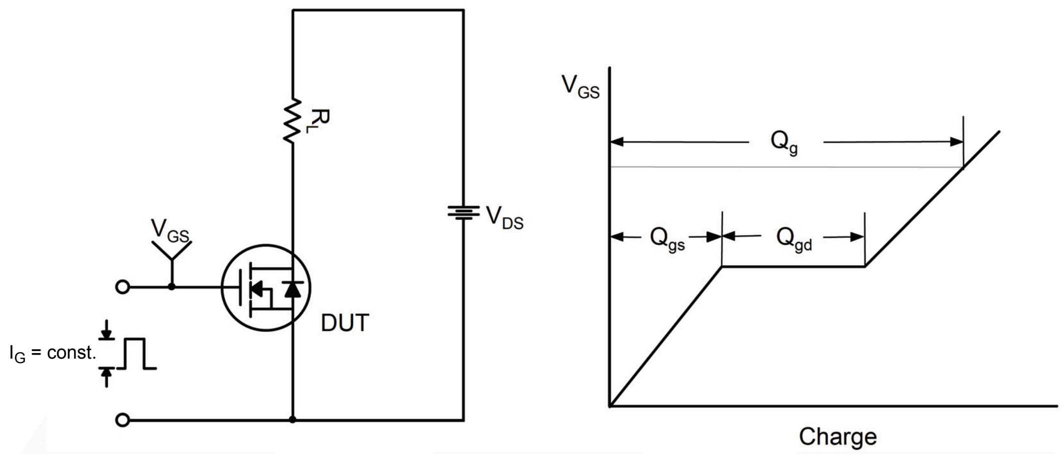


Figure 13. Gate Charge Test Circuit & Waveform

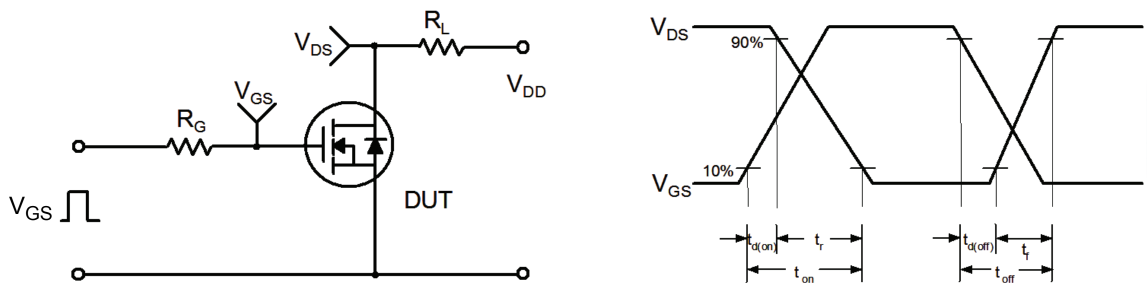


Figure 14. Resistive Switching Test Circuit & Waveforms

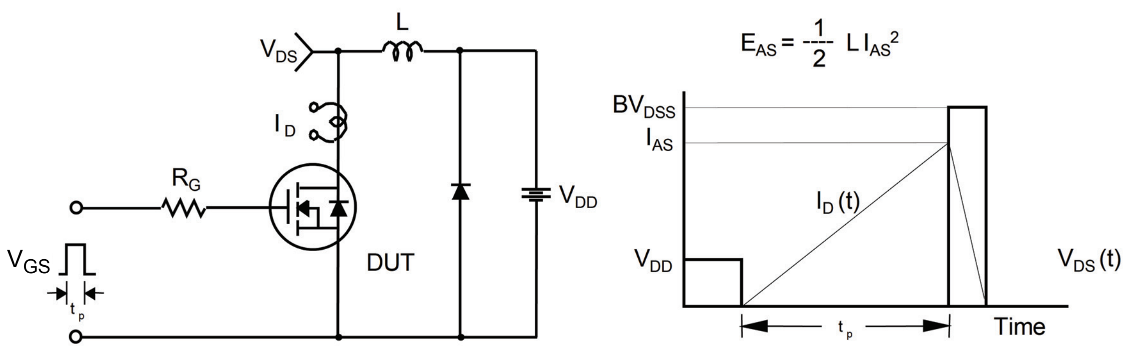


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

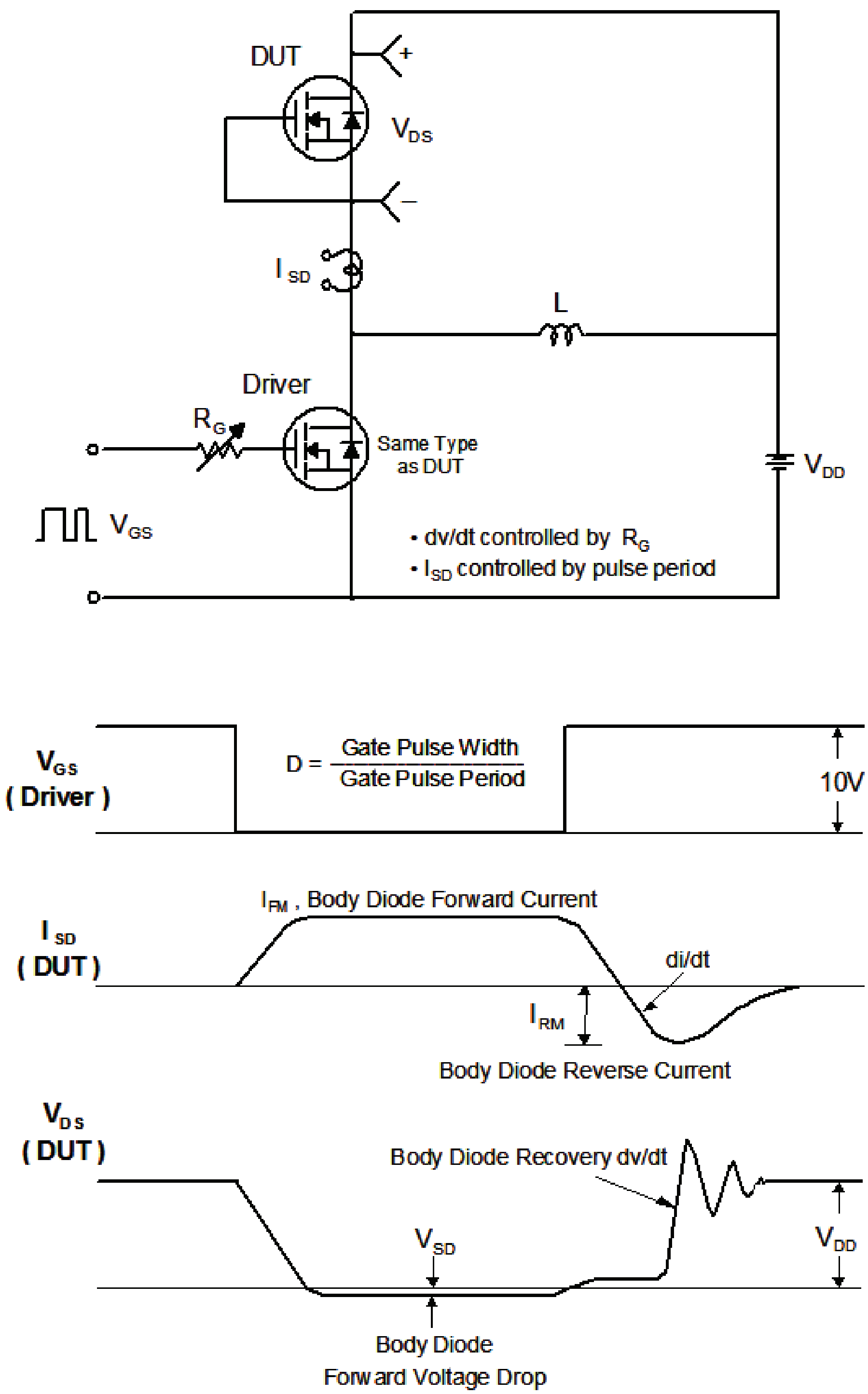
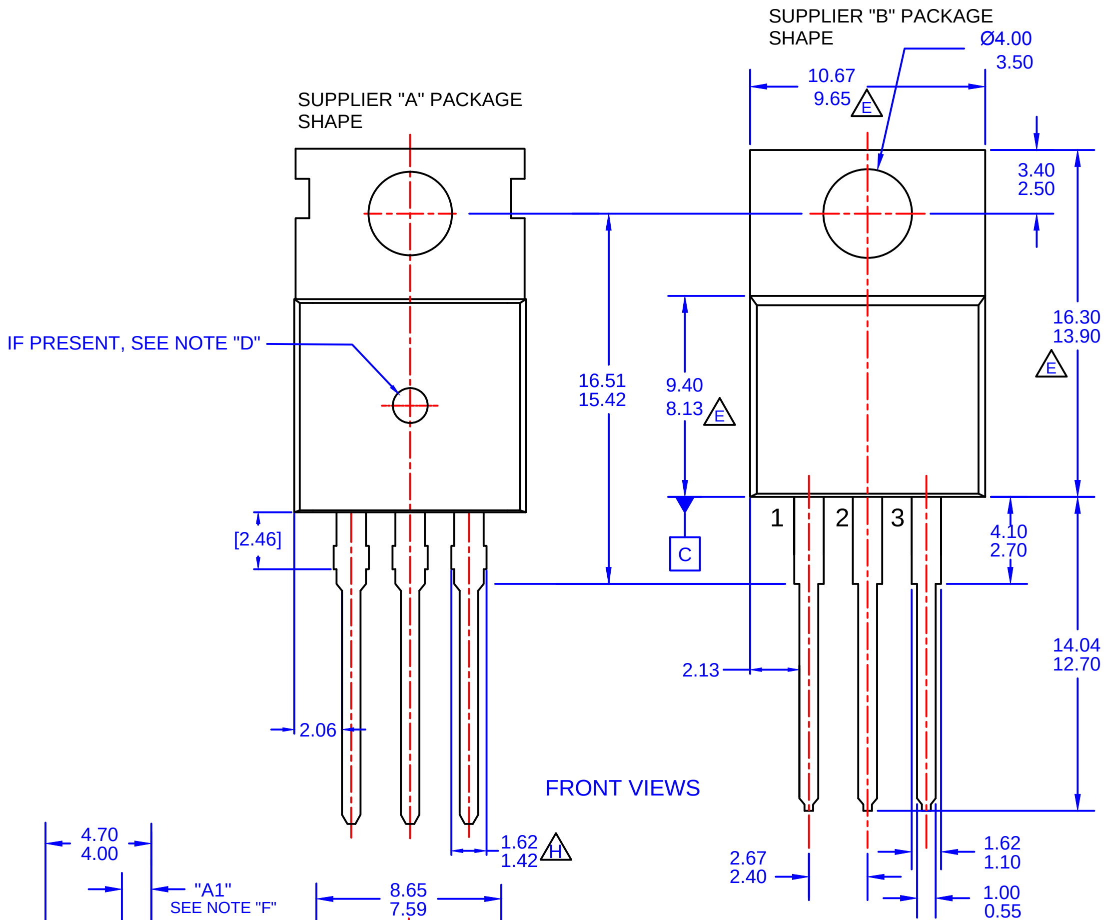
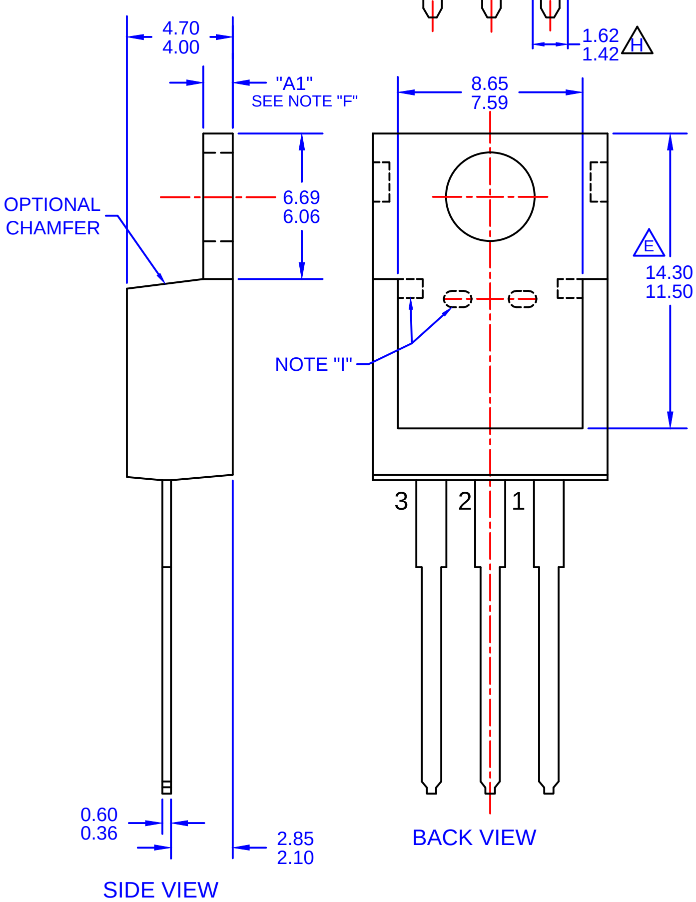
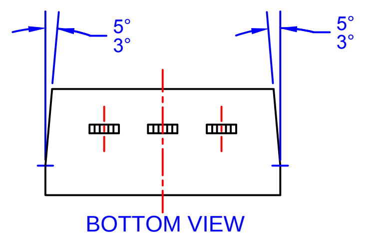


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms







NOTES:

A) REFERENCE JEDEC, TO-220, VARIATION AB

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].

D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)

E DOES NOT COMPLY JEDEC STANDARD VALUE.

F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45

G) DRAWING FILE NAME: TO220B03REV9

H PRESENCE IS SUPPLIER DEPENDENT

I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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