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## FDA20N50-F109

# N-Channel UniFET<sup>TM</sup> MOSFET 500 V, 20 A, 230 m $\Omega$

#### **Features**

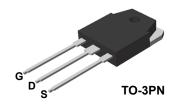
- $R_{DS(on)}$  = 230 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D$  = 10 A
- Low Gate Charge (Typ. 45.6 nC)
- Low C<sub>rss</sub> (Typ. 27 pF)
- · 100% Avalanche Tested
- · Improved dv/dt Capability

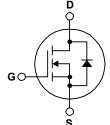
#### **Applications**

- PDP TV
- · Uninterruptible Power Supply
- AC-DC Power Supply

### **Description**

UniFET<sup>TM</sup> MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FDA20N50-F109	Unit	
V <sub>DSS</sub>	Drain-Source Voltage		500	V	
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)		22 13.2	A A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	88	А
V <sub>GSS</sub>	Gate-Source voltage		± 30	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy		(Note 2)	1110	mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	22	А
E <sub>AR</sub>	Repetitive Avalanche Energy		(Note 1)	28.0	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C) - Derate above 25°C		280 2.3	W W/°C
T <sub>J,</sub> T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C	

#### **Thermal Characteristics**

Symbol	Parameter	FDA20N50-F109	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.44	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W	

# **Package Marking and Ordering Information**

<b>Device Marking</b>	Device	Package	Reel Size	Tape Width	Quantity	
FDA20N50	FDA20N50-F109	TO-3PN	Tube	N/A	30 units	

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
Off Characteristics							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0V$ , $I_D = 250\mu A$ , $T_J = 25^{\circ}C$	500			V	
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C		0.50		V/°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 400V, T <sub>C</sub> = 125°C			1 10	μ <b>Α</b> μ <b>Α</b>	
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V			100	nA	
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V			-100	nA	
On Charac	teristics					•	
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V	
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 11A		0.20	0.23	Ω	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 11A		24.6		S	
Dynamic C	haracteristics				•		
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$		2400	3120	pF	
C <sub>oss</sub>	Output Capacitance	f = 1.0MHz		355	465	pF	
C <sub>rss</sub>	Reverse Transfer Capacitance			27		pF	
Switching	Characteristics				_		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250V, I <sub>D</sub> = 20A		95	200	ns	
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25\Omega$		375	760	ns	
t <sub>d(off)</sub>	Turn-Off Delay Time			100	210	ns	
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		105	220	ns	
Qg	Total Gate Charge	V <sub>DS</sub> = 400V, I <sub>D</sub> = 20A		45.6	59.5	nC	
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = 10V		14.8		nC	
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)		21.6		nC	
Drain-Sour	ce Diode Characteristics and Maximun	n Ratings		I.		ı	
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				20	Α	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				80	Α	
$V_{SD}$	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 22A			1.4	V	
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 20A		507		ns	
Q <sub>rr</sub>	Reverse Recovery Charge	dl <sub>F</sub> /dt =100A/μs		7.20		μС	

<sup>1.</sup> Repetitive Rating: Pulse width limited by maximum junction temperature

<sup>2.</sup> L = 4.1mH, I $_{AS}$  = 22A, V $_{DD}$  = 50V, R $_{G}$  = 25 $\Omega$ , Starting T $_{J}$  = 25 $^{\circ}$ C

<sup>3.</sup> I  $_{SD}$   $\leq$  22A, di/dt  $\leq$  200A/ $\mu$ s, V  $_{DD}$   $\leq$  BV  $_{DSS}$ , Starting T  $_{J}$  = 25°C

<sup>4.</sup> Essentially Independent of Operating Temperature Typical Characteristics

### **Typical Characteristics**

Figure 1. On-Region Characteristics

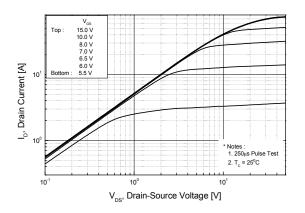


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

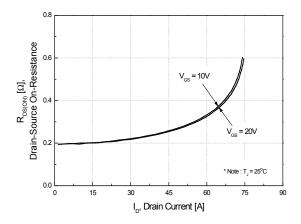


Figure 5. Capacitance Characteristics

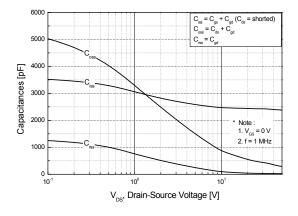


Figure 2. Transfer Characteristics

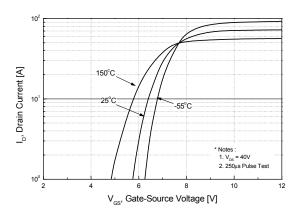


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

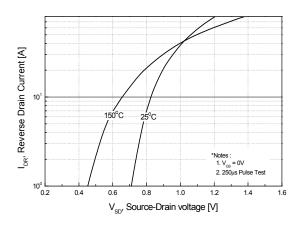
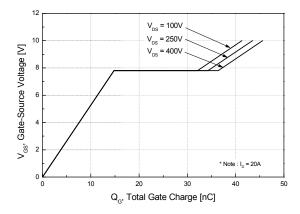


Figure 6. Gate Charge Characteristics



### Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

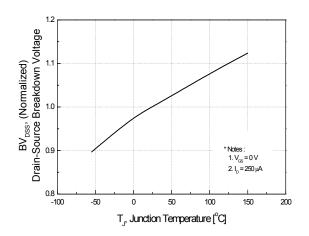


Figure 8. On-Resistance Variation vs. Temperature

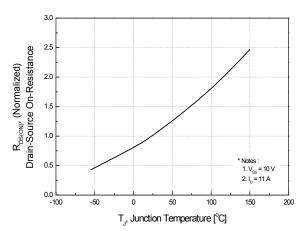
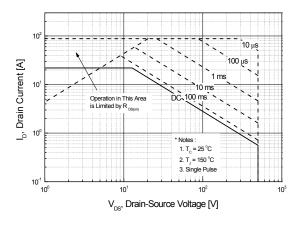


Figure 9. Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature



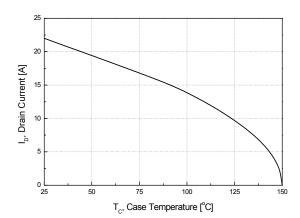


Figure 11. Transient Thermal Response Curve

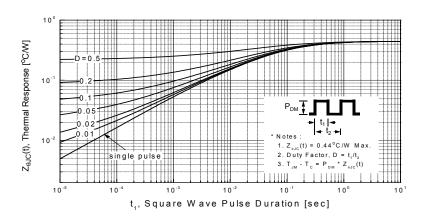


Figure 12. Gate Charge Test Circuit & Waveform

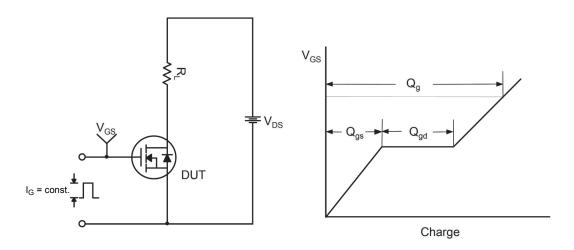


Figure 13. Resistive Switching Test Circuit & Waveforms

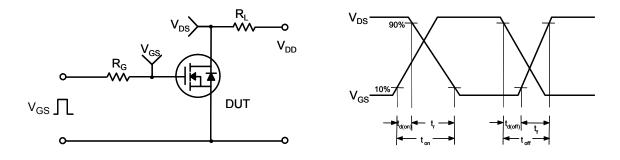
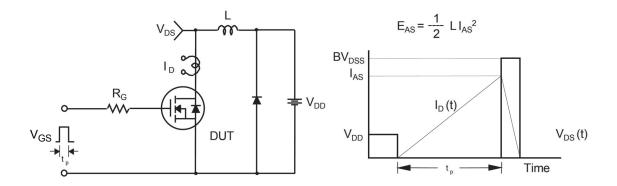


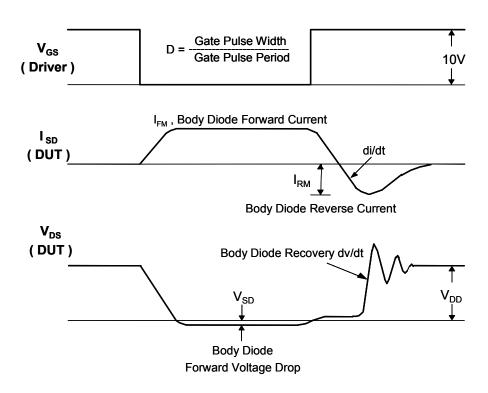
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



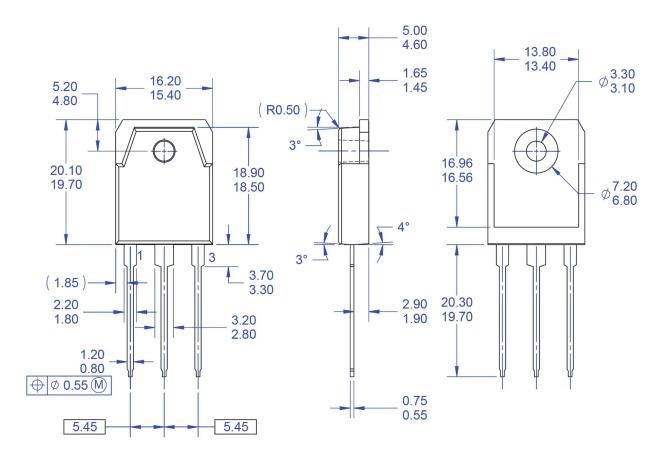
DUT I<sub>SD</sub> 🔦 Driver Same Type as DUT **Ļ** V<sup>DD</sup>

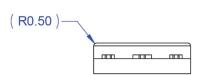
• dv/dt controlled by R<sub>G</sub> • I<sub>SD</sub> controlled by pulse period

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



#### **Mechanical Dimensions**





#### NOTES: UNLESS OTHERWISE SPECIFIED

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- F) FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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