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May 2013

FDB86135 N-Channel Shielded Gate PowerTrench[®] MOSFET 100V, 176A, 3.5mΩ

Features

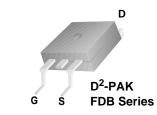
- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 3.5m Ω at V_{GS} = 10V, I_D = 75A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{\text{DS}(\text{on})}$
- High Power and Current Handling Capability
- RoHS Compliant

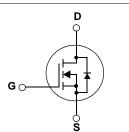
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Applications

- DC-DC primary bridge
- DC-DC Synchronous rectification
- Hot swap





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units	
V _{DSS}	Drain to Source Voltage			100	V	
V _{GSS}	Gate to Source Voltage			±20	V	
ID	Drain Curren - Continuous (Silicon Limited) $T_{C} = 25^{\circ}C$			176	A	
	- Continuous(Package Limited) T _C = 25°C			120		
	- Continuous		T _C = 25 ^o C(Note 1a)	75		
	- Pulsed			704	А	
E _{AS}	Single Pulsed Avalanche Energy		(Note 3)	658	mJ	
P _D	Power Dissipation	- T _C = 25 ^o C	(Note 1a)	227	W	
		- T _A = 25 ^o C	(Note 1b)	2.4	W/ºC	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +175	°C	

Thermal Characteristics

Symbol	Parameter	Ratings	Units		
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	(Note 1)	0.66	°C/W	
R_{\thetaJA}	Thermal Resistance, Junction to Ambient	(Note 1a)	62.5	-C/W	

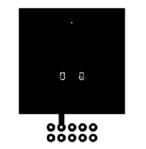
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB86135	FDB86135	D2-PAK	330mm	24mm	800

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V, T_C = 25 ^o C	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to $25^{\circ}C$	-	0.07	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 80V, V _{GS} = 0V	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	±100	nA
On Charac	teristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10V, I _D = 75A	-	3.0	3.5	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 10V, I _D = 75A	-	167	-	S
C _{iss}	Characteristics Input Capacitance	$V_{DS} = 25V. V_{CS} = 0V$	-	5485	7295	pF
C _{oss}	Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V$	-	2430	3230	pF
C _{rss}	Reverse Transfer Capacitance	f = 1MHz	-	210	-	pF
Q _{g(tot)}	Total Gate Charge at 10V		-	89	116	nC
Q _{gs}	Gate to Source Gate Charge	V _{DS} = 80V, I _D = 75A	-	24	-	nC
Q _{gs2}	Gate Charge Threshold to Plateau	$V_{GS} = 10V$	-	8	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	25	-	nC
	Characteristics		-			
t _{d(on)}	Turn-On Delay Time		-	22	54	ns
t _r	Turn-On Rise Time	$V_{DD} = 50V, I_D = 75A$	-	54	118	ns
t _{d(off)}	Turn-Off Delay Time	$-V_{GS}$ = 10V, R _{GEN} = 4.7 Ω	-	37	84	ns
t _f	Turn-Off Fall Time		-	11	32	ns
Drain-Sou	rce Diode Characteristics					
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 75A (Note 2)	-	-	1.25	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0V, I_{SD} = 75A, V_{DD} = 80V$	-	72	-	ns
Q _{rr}	Reverse Recovery Charge	dl _F /dt = 100A/μs	_	129		nC

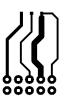
NOTES:

1. R_{0JA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0 %. 3. Starting T_J = 25 °C, L = 1 mH, I_{AS} = 36.3 A, V_{DD} = 100 V, V_{GS} = 10 V.

a) 40 °C/W when mounted on a 1 in² pad of 2 oz copper



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b) 62.5 °C/W when mounted on a minimum pad of 2 oz copper



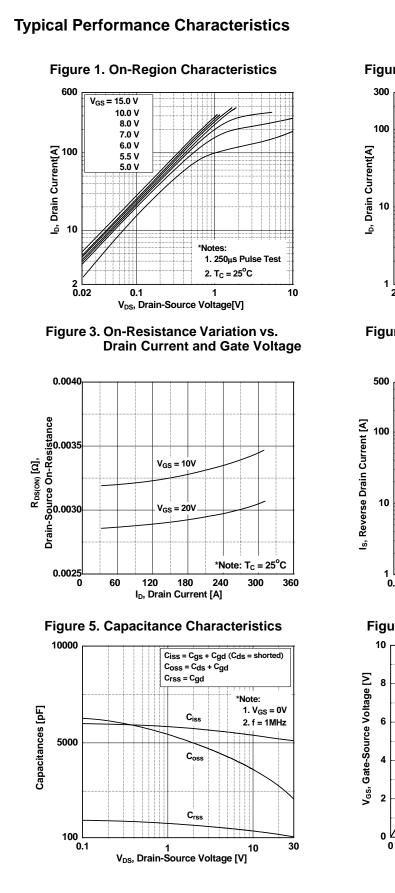
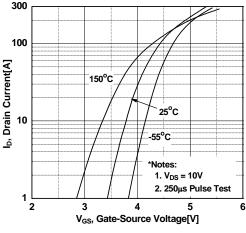
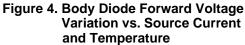
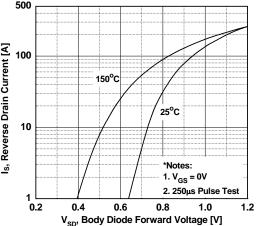


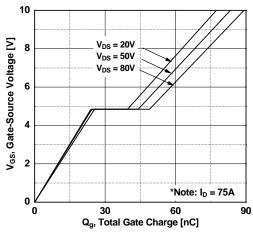
Figure 2. Transfer Characteristics

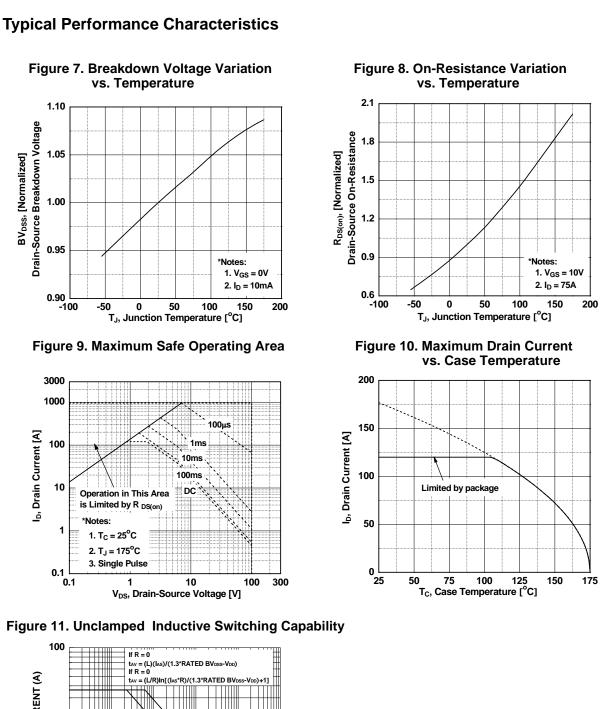




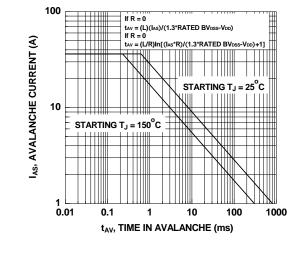


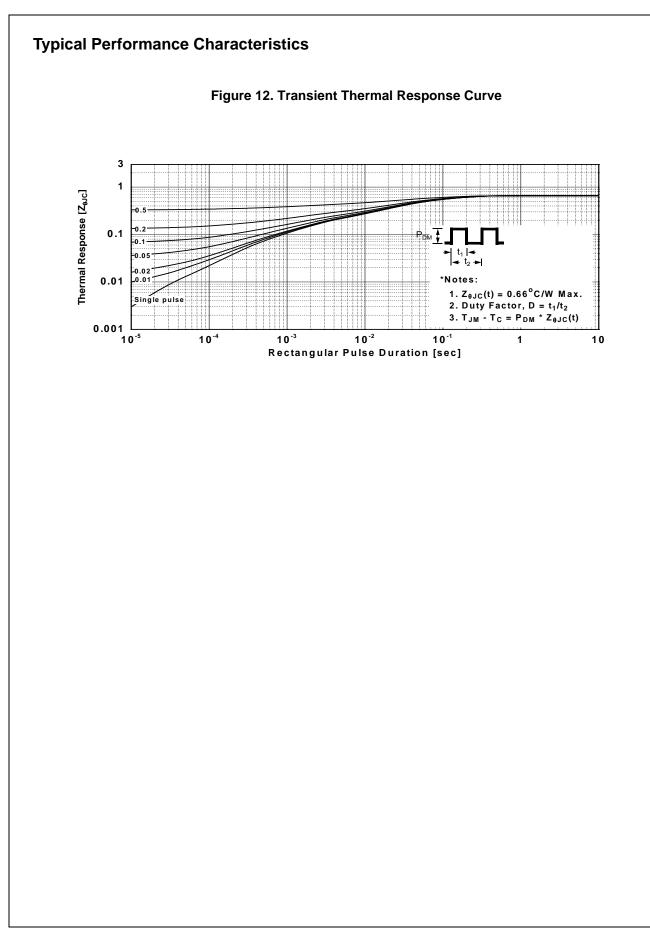


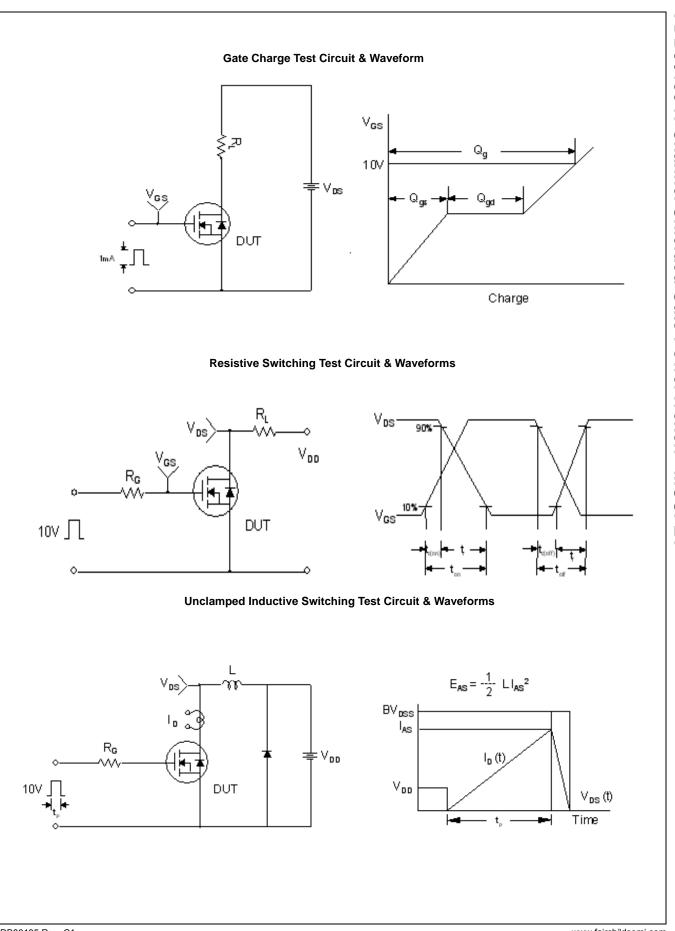




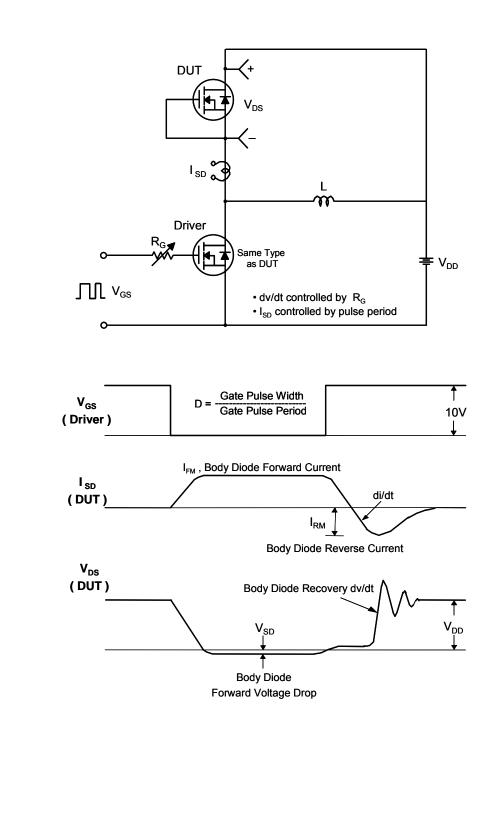


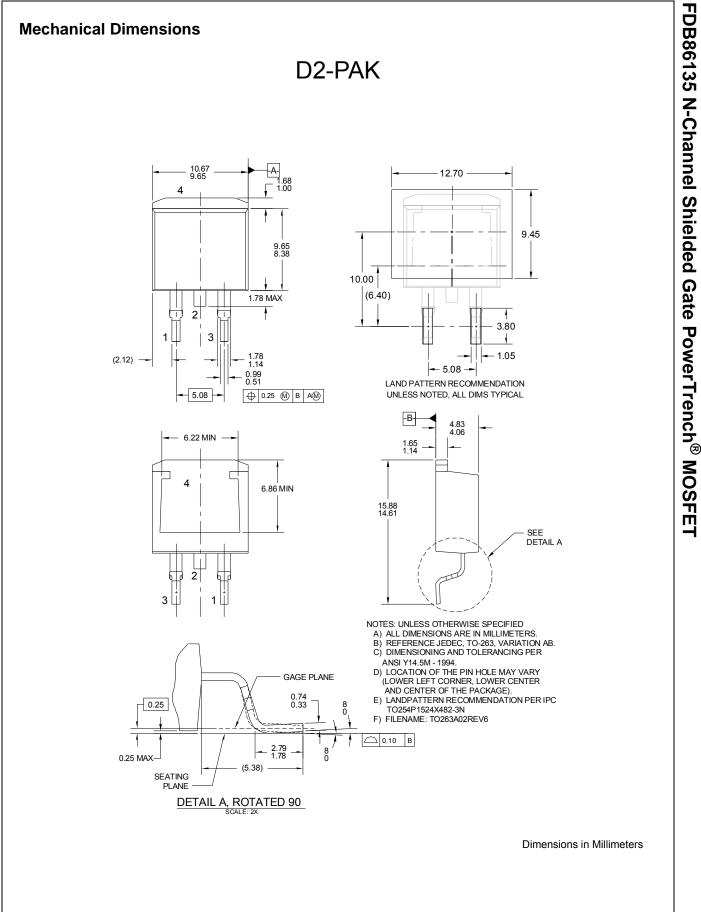






Peak Diode Recovery dv/dt Test Circuit & Waveforms







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