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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

April 2015

# FDBL0210N80

N-Channel PowerTrench® MOSFET

80 V, 240 A, 2.0 mΩ

Features

- Typical $R_{DS(on)}$ = 1.5 mΩ at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 130 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automations
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch
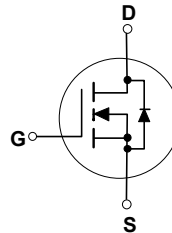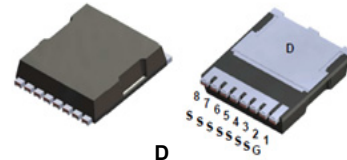
For current package drawing, please refer to the Fairchild website at http://www.fairchildsemi.com/dwg/PS/PSOF08A.pdf.

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		80	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1) T_C = 25°C		240	A
	Pulsed Drain Current T_C = 25°C		See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)		512	mJ
P_D	Power Dissipation		357	W
	Derate Above 25°C		2.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{θJC}$	Thermal Resistance, Junction to Case		0.42	°C/W
$R_{θJA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)		43	°C/W

Notes:
1: Current is limited by silicon.
2: Starting T_J = 25°C, L = 0.25mH, I_{AS} = 64A, V_{DD} = 80V during inductor charging and V_{DD} = 0V during time in avalanche.
3: $R_{θJA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{θJC}$ is guaranteed by design, while $R_{θJA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL0210N80	FDBL0210N80	MO-299A	-	-	-

Electrical Characteristics T_J = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		80	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=80V, V_{GS} = 0V	T_J = 25°C	-	-	1	μA
			T_J = 175°C (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 80A, V_{GS}= 10V	T_J = 25°C	-	1.5	2.0	mΩ
			T_J = 175°C (Note 4)	-	3.1	4.1	mΩ
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		-	10000	-	pF
C_{oss}	Output Capacitance			-	1540	-	pF
C_{rss}	Reverse Transfer Capacitance			-	70	-	pF
R_g	Gate Resistance	f = 1MHz		-	2.8	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	V_{GS} = 0 to 10V	V_{DD} = 64V I_D = 80A	-	130	169	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	18	27	nC
Q_{gs}	Gate-to-Source Gate Charge			-	47	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge			-	24	-	nC
Switching Characteristics							
t_{on}	Turn-On Time	V_{DD} = 40V, I_D = 80A, V_{GS} = 10V, R_{GEN} = 6Ω		-	-	133	ns
$t_{d(on)}$	Turn-On Delay			-	39	-	ns
t_r	Rise Time			-	63	-	ns
$t_{d(off)}$	Turn-Off Delay			-	61	-	ns
t_f	Fall Time			-	33	-	ns
t_{off}	Turn-Off Time			-	-	140	ns
Drain-Source Diode Characteristics							
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} =80A, V_{GS} = 0V		-	-	1.25	V
		I_{SD} = 40A, V_{GS} = 0V		-	-	1.2	V
t_{rr}	Reverse-Recovery Time	I_F = 80A, dI_{SD}/dt = 100A/μs, V_{DD}=64V		-	83	108	ns
Q_{rr}	Reverse-Recovery Charge			-	118	153	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics

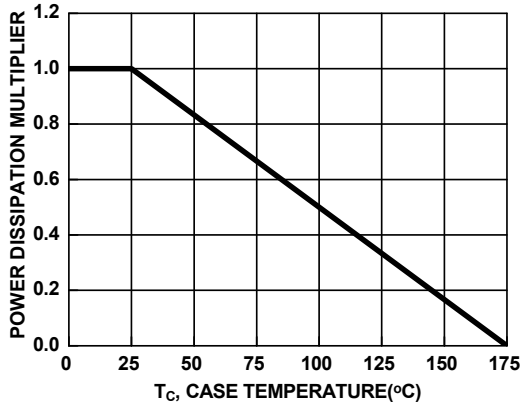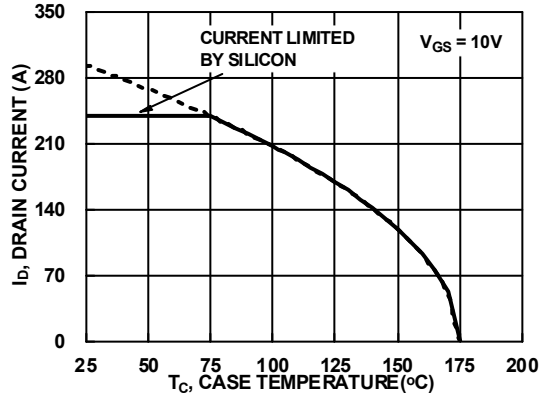Figure 1. Normalized Power Dissipation vs. Case Temperature

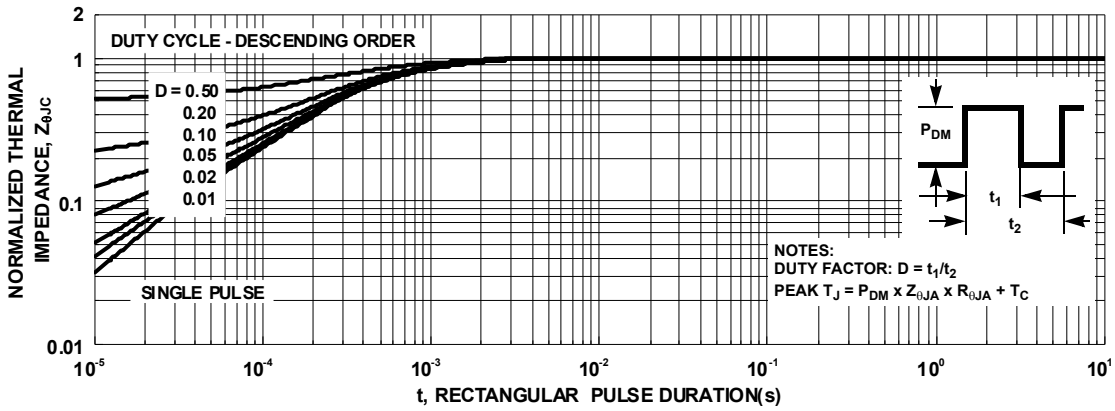Figure 2. Maximum Continuous Drain Current vs. Case Temperature

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_C

Figure 3. Normalized Maximum Transient Thermal Impedance

T_C = 25°C
FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_2 \left[\sqrt{\frac{175 - T_C}{150}} \right]$$
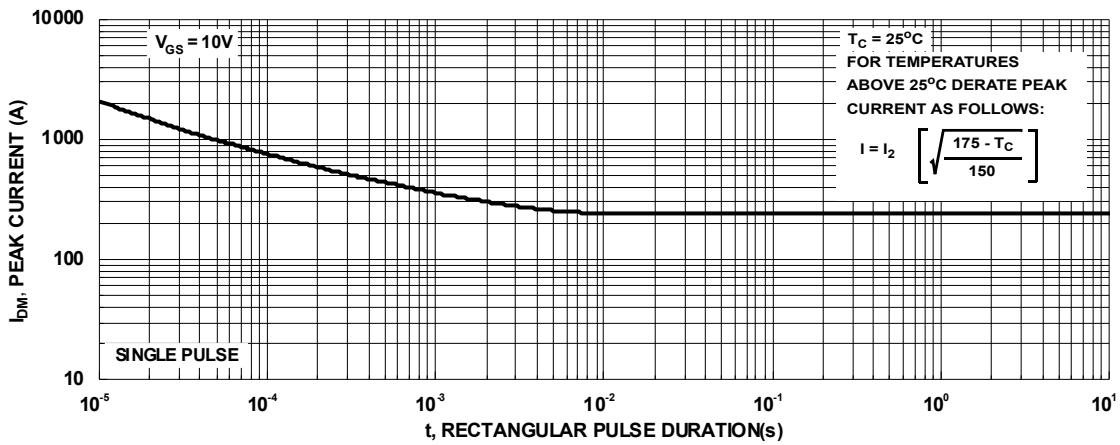
Figure 4. Peak Current Capability

Typical Characteristics
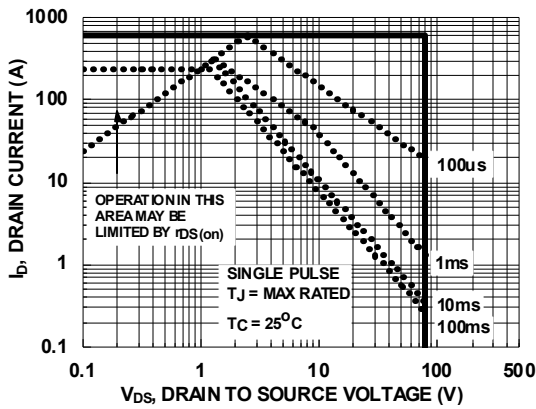
Figure 5. Forward Bias Safe Operating Area
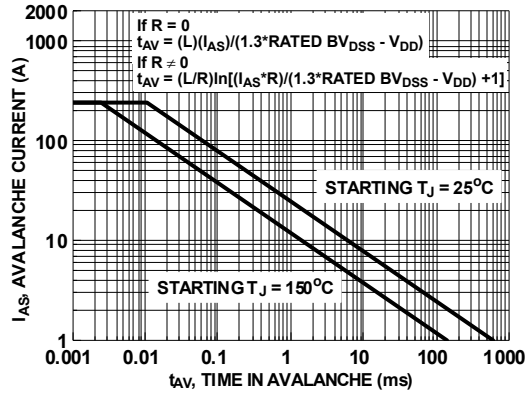
NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability
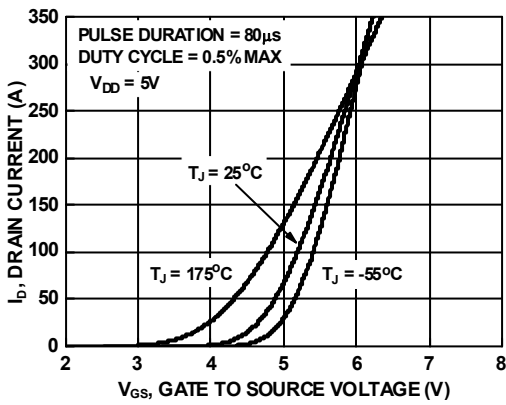
Figure 7. Transfer Characteristics
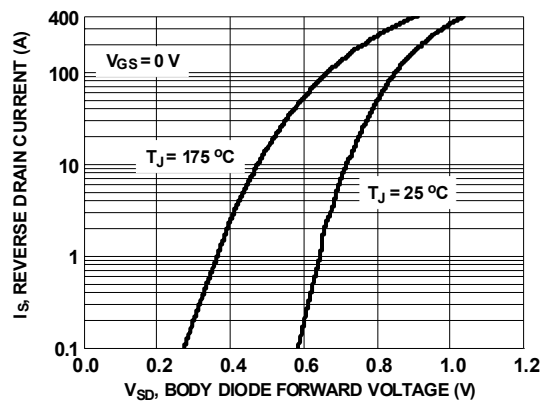
Figure 8. Forward Diode Characteristics
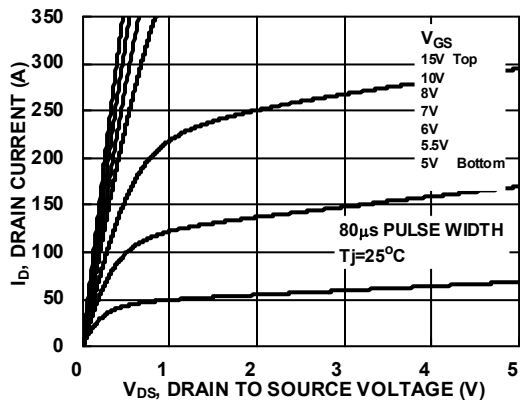
Figure 9. Saturation Characteristics
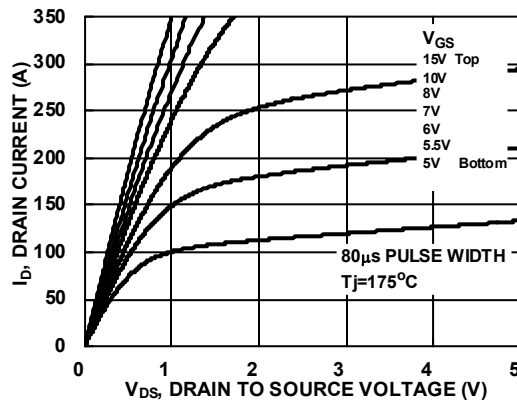
Figure 10. Saturation Characteristics

Typical Characteristics
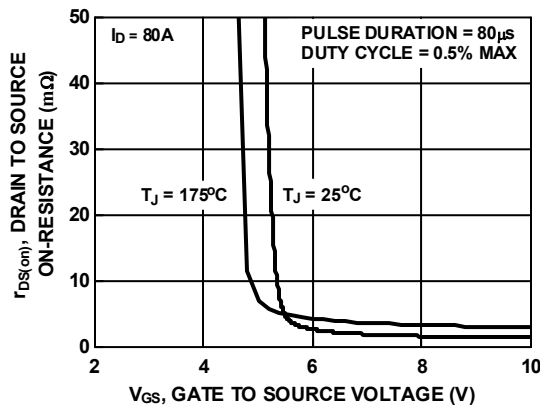
Figure 11. R$_{DSON}$ vs. Gate Voltage
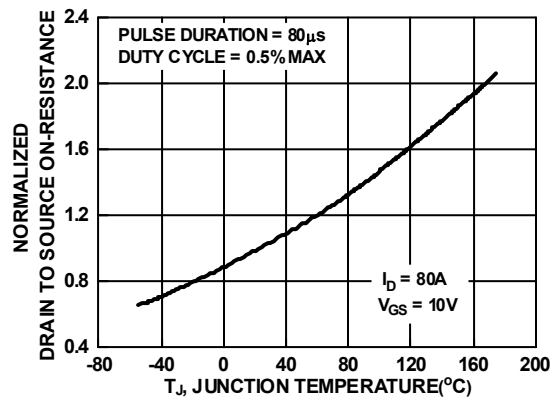
Figure 12. Normalized R$_{DSON}$ vs. Junction Temperature
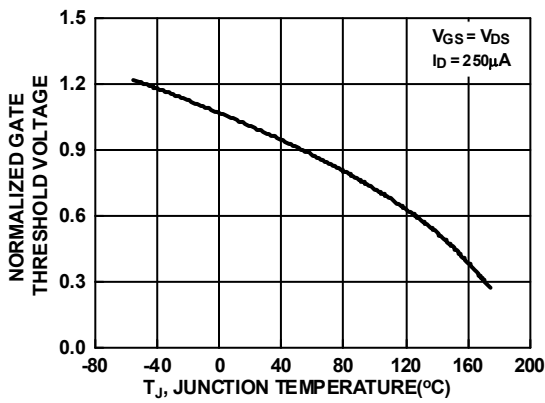
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
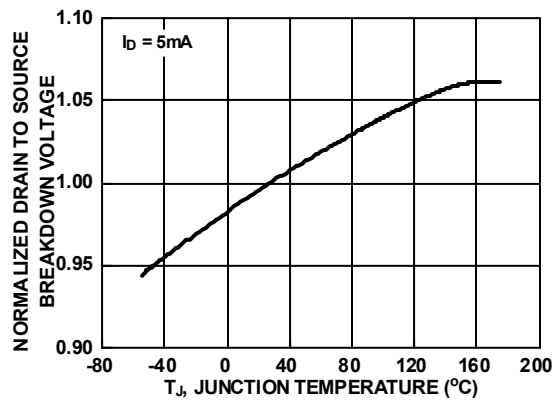
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
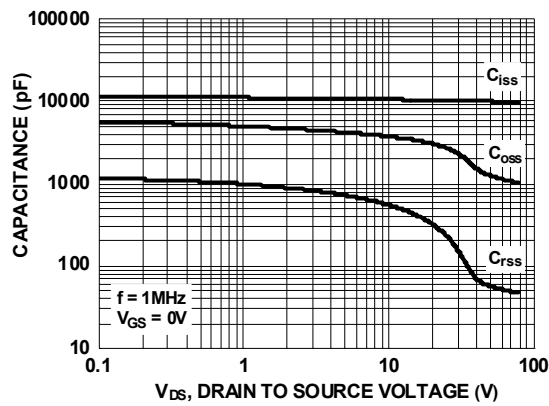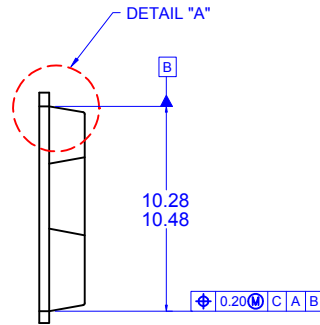

Figure 15. Capacitance vs. Drain to Source Voltage
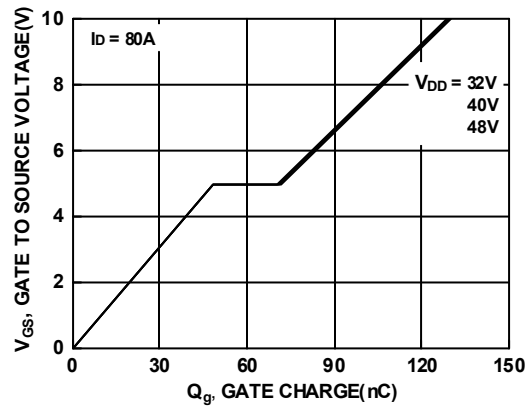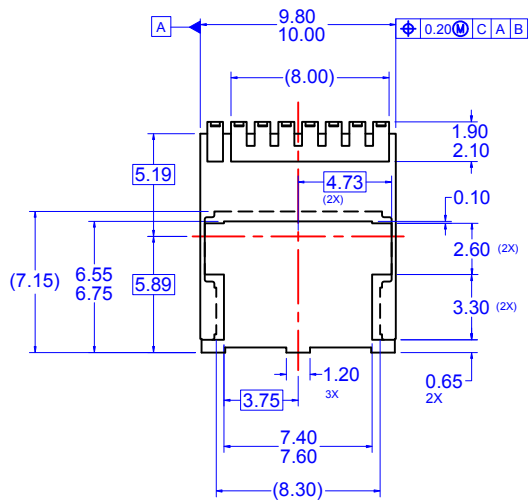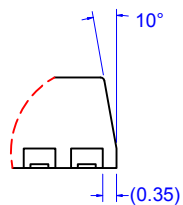

Figure 16. Gate Charge vs. Gate to Source Voltage

TOP VIEW

9.70 / 9.90

0.60 / 0.80

(0.40)

(3.30) (2X)

11.58 / 11.78

0.50 / 0.70

0.60

0.70 (8X) / 0.90

1.20 7X

(0.35)

8.40

⌖ 0.25 Ⓜ C A B
⌖ 0.20 Ⓜ C

1   8

SIDE VIEW

// 0.20 C

2.20 / 2.40

▱ 0.10 C

DETAIL "B"

0.40 / 0.60

C

BOTTOM VIEW

A   ⌖ 0.20 Ⓜ C A B

9.80 / 10.00

(8.00)

5.19

4.73 (2X)

0.10

1.90 / 2.10

2.60 (2X)

6.55 / 6.75

5.89

(7.15)

3.30 (2X)

1.20 3X

3.75

0.65 2X

7.40 / 7.60

(8.30)

DETAIL "A"

DETAIL "A"

B

10.28 / 10.48

⌖ 0.20 Ⓜ C A B

0.40 / 0.60

10°

0.60 / 0.80

DETAIL "B"

10°

(0.35)
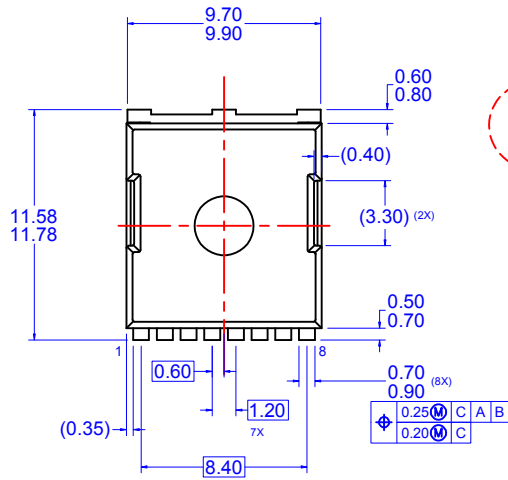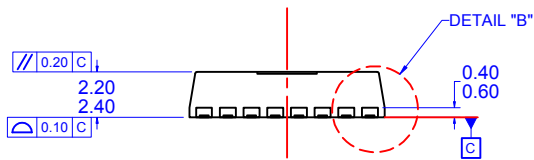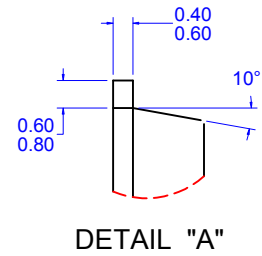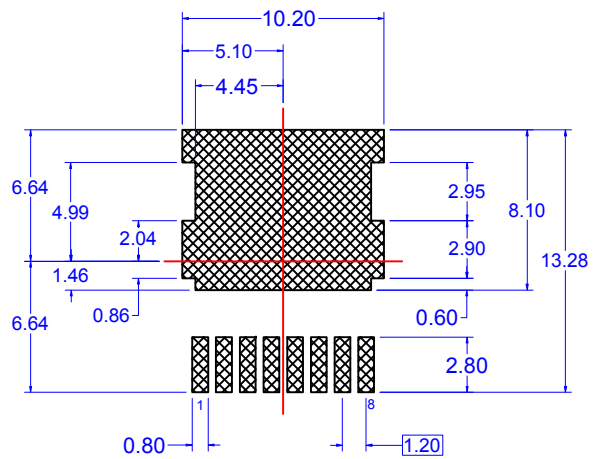
LAND PATTERN RECOMMENDATION

10.20

5.10

4.45

6.64

4.99

2.04

1.46

6.64

0.86

2.95

8.10

2.90

13.28

0.60

2.80

0.80

1.20

1   8

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE:
    JEDEC MO-299, ISSUE A, DATED NOVEMBER
    2009.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS
    OR MOLD FLASH. MOLD FLASH OR
    BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER
    ASME Y14.5M-1994.

E) DRAWING FILE NAME: MKT-PSOF08AREV3

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