MOSFET – N-Channel, POWERTRENCH®

150 V, 169 A, 6.3 mΩ

FDBL86210-F085

Features

- Typical $r_{DS(on)}$ = 5 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 70 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- AEC−Q101 Qualified and PPAP Capable
- This Device is Pb−Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

ON Semiconductor®

N−Channel

H−PSOF8L
CASE 100CU

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

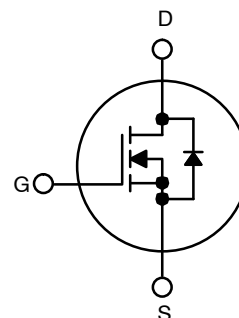| Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous (V_{GS} = 10), T_C = 25°C (Note 1)	169	A
	Pulsed Drain Current, T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	502	mJ
P_D	Power Dissipation	500	W
	Derate Above 25°C	3.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Current is limited by silicon.
2. Starting T_J = 25°C, L = 0.24 mH, I_{AS} = 64 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.
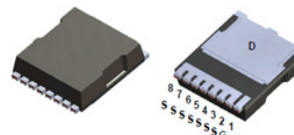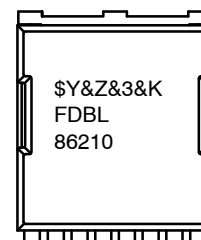
MARKING DIAGRAM


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$Y&Z&3&K
FDBL
86210
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$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86210	= Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping[†]
FDBL86210−F085	FDBL86210	H−PSOF8L	2000 Units/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu A$, $V_{GS} = 0\ V$		150	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 150\ V$, $V_{GS} = 0\ V$	$T_J = 25°C$	–	–	1	μA
			$T_J = 175°C$ (Note 4)	–	–	1	mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm20\ V$		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu A$		2.0	2.8	4.0	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 80\ A$, $V_{GS} = 10\ V$	$T_J = 25°C$	–	5	6.3	mΩ
			$T_J = 175°C$ (Note 4)	–	14	17.5	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 75\ V$, $V_{GS} = 0\ V$, $f = 1\ MHz$		–	5805	–	pF
C_{oss}	Output Capacitance			–	536	–	pF
C_{rss}	Reverse Transfer Capacitance			–	16	–	pF
R_g	Gate Resistance	$f = 1\ MHz$		–	2.2	–	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	$V_{GS} = 0$ to $10\ V$	$V_{DD} = 75\ V$, $I_D = 80\ A$	–	70	90	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to $2\ V$		–	10.5	13	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 75\ V$, $I_D = 80\ A$		–	32.5	–	nC
Q_{gd}	Gate to Drain "Miller" Charge			–	10	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	$V_{DD} = 75\ V$, $I_D = 80\ A$, $V_{GS} = 10\ V$, $R_{GEN} = 6\ \Omega$		–	–	80	ns
$t_{d(on)}$	Turn−On Delay Time			–	39	–	ns
t_r	Rise Time			–	30	–	ns
$t_{d(off)}$	Turn−Off Delay Time			–	70	–	ns
t_f	Fall Time			–	23	–	ns
t_{off}	Turn−Off Time			–	–	130	ns
DRAIN−SOURCE DIODE CHARACTERISTIC							
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\ A$, $V_{GS} = 0\ V$		–	–	1.25	V
		$I_{SD} = 40\ A$, $V_{GS} = 0\ V$		–	–	1.2	V
T_{rr}	Reverse Recovery Time	$I_F = 80\ A$, $dI_{SD}/dt = 100\ A/\mu s$, $V_{DD} = 120\ V$		–	108	125	ns
Q_{rr}	Reverse Recovery Charge			–	323	467	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. The maximum value is specified by design at $T_J = 175°C$. Product is not tested to this condition in production.

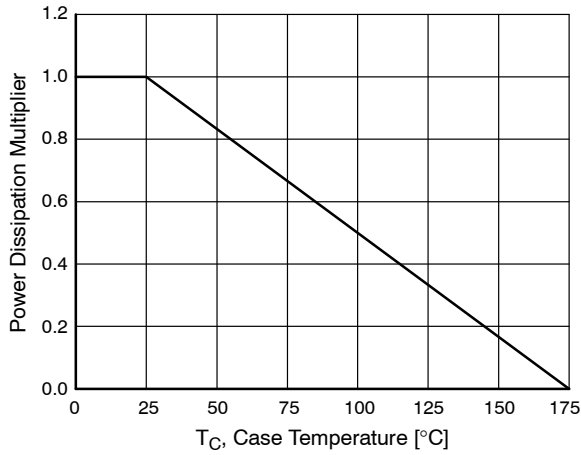## TYPICAL CHARACTERISTICS

Figure 1. Normalized Power Dissipation
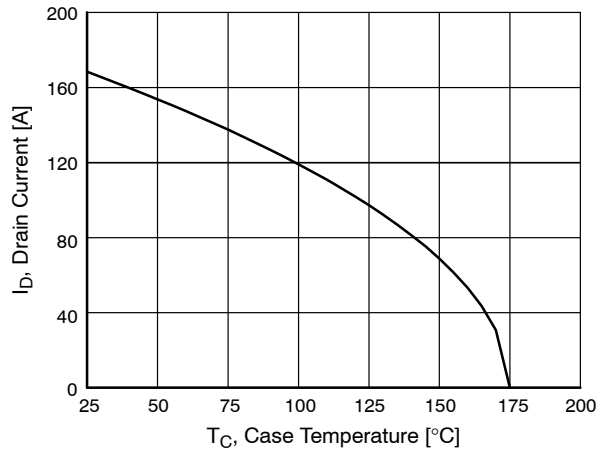vs. Case Temperature

Figure 2. Maximum Continuous Drain Current
vs. Case Temperature
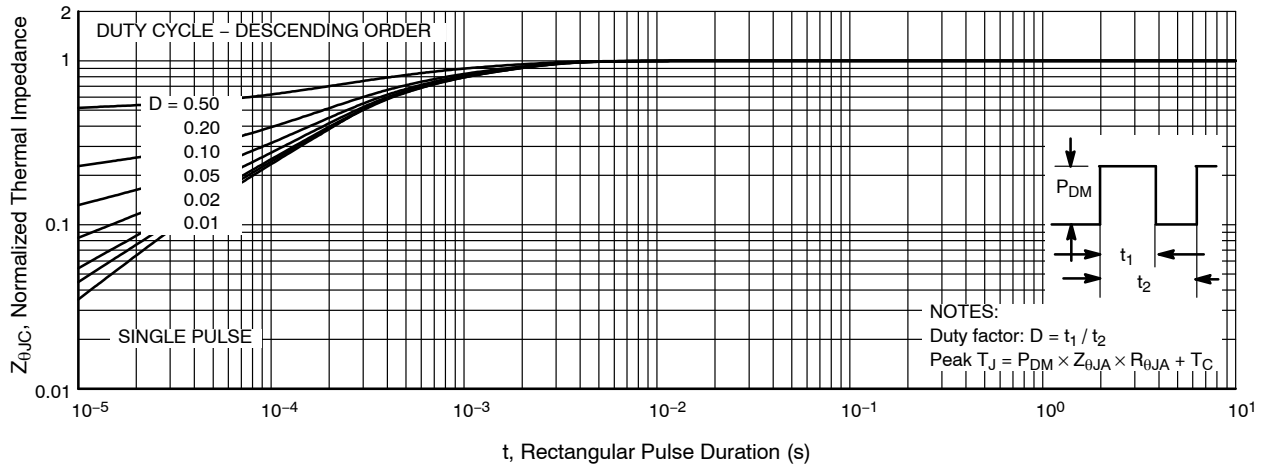

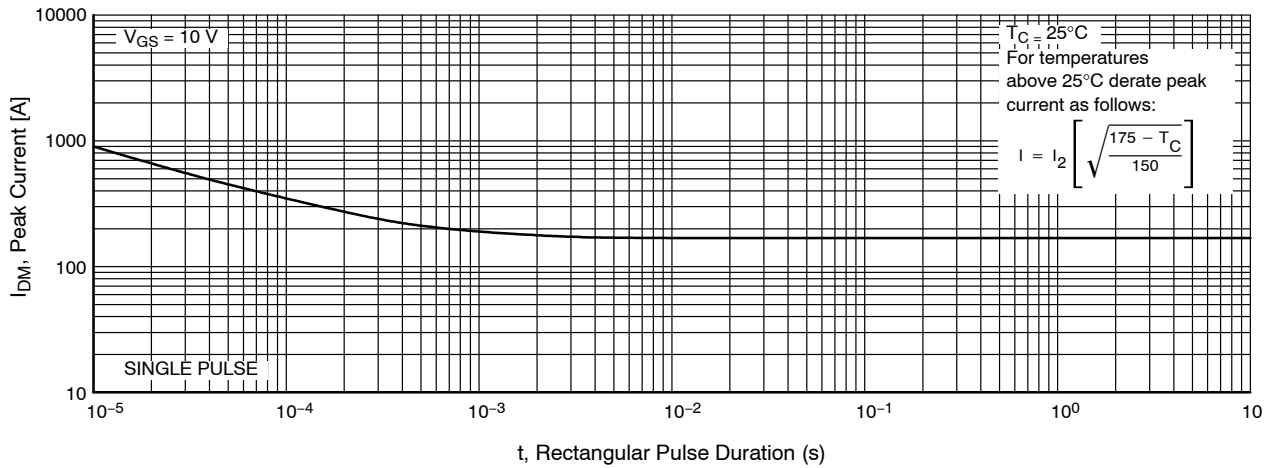Figure 3. Normalized Maximum Transient Thermal Impedance

Figure 4. Peak Current Capability
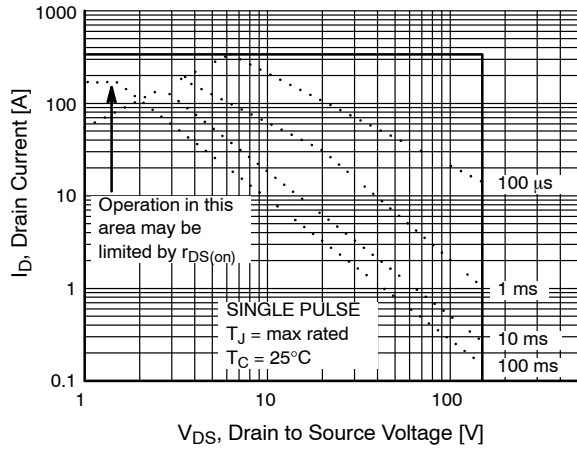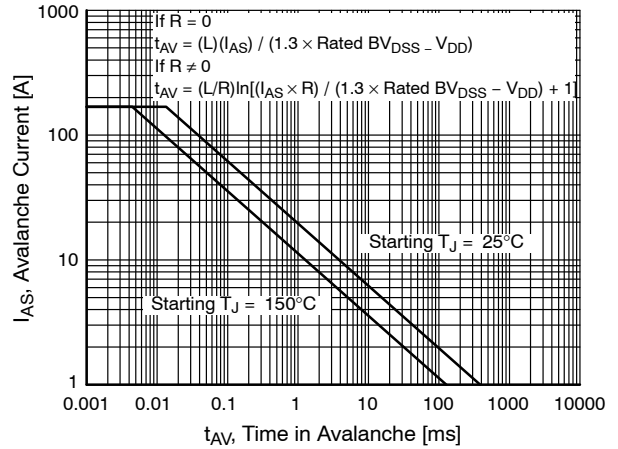
TYPICAL CHARACTERISTICS (continued)

Figure 5. Forward Bias Safe Operating Area

NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515.
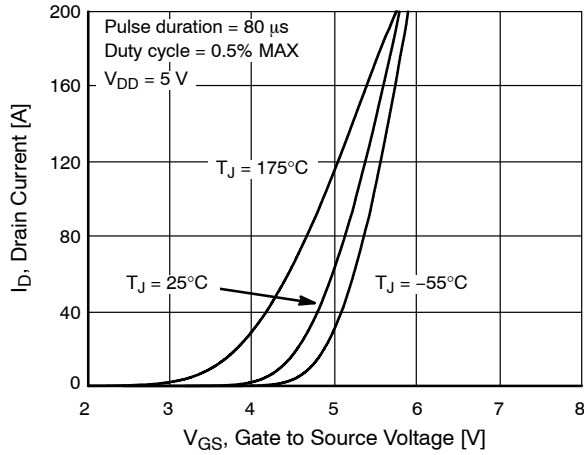
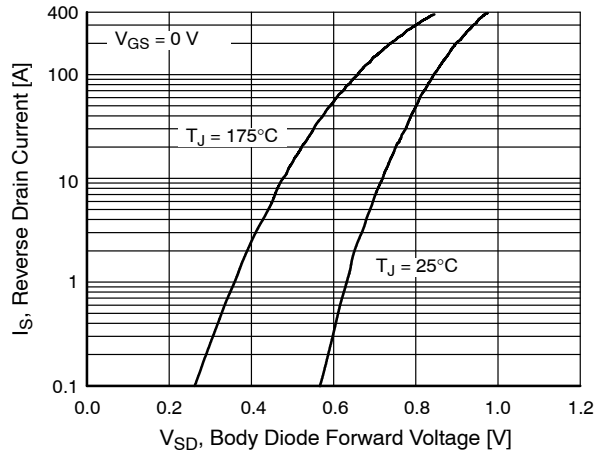Figure 6. Unclamped Inductive Switching Capability

Figure 7. Transfer Characteristics

Figure 8. Forward Diode Characteristics
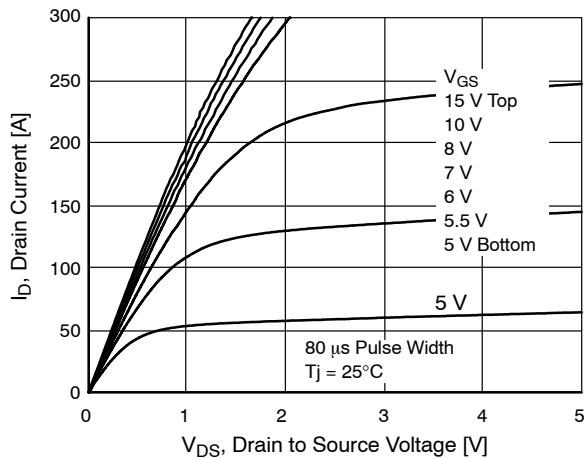
Figure 9. Saturation Characteristics
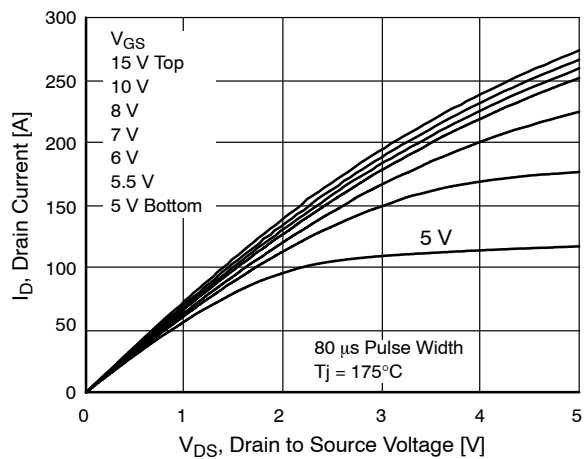
Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)
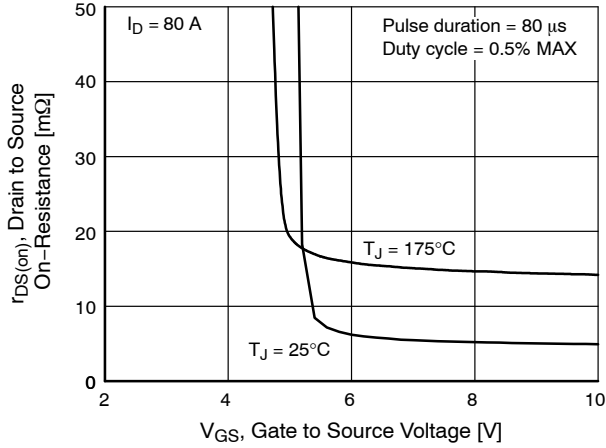
Figure 11. R$_{DSON}$ vs. Gate Voltage
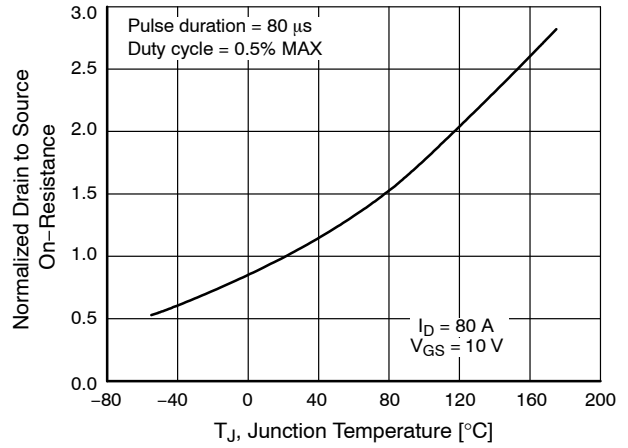
Figure 12. Normalized R$_{DSON}$ vs. Junction Temperature
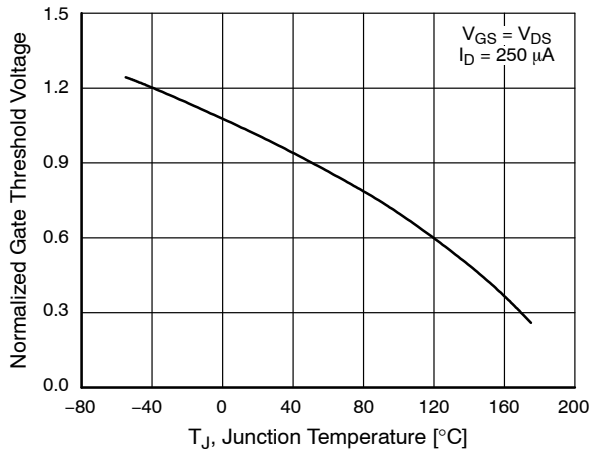
Figure 13. Normalized Gate Threshold Voltage vs. Temperature
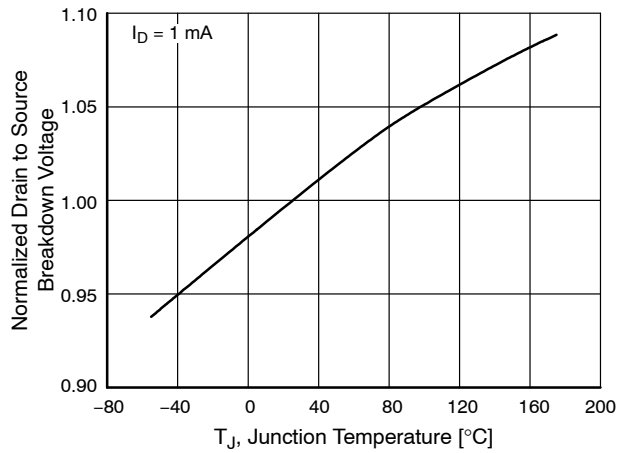
Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature
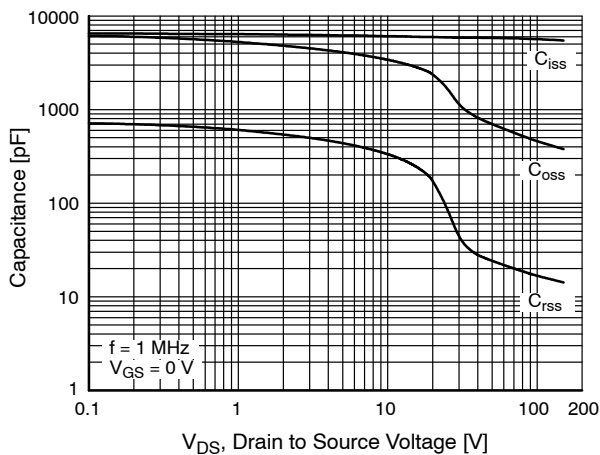
Figure 15. Capacitance vs. Drain to Source Voltage
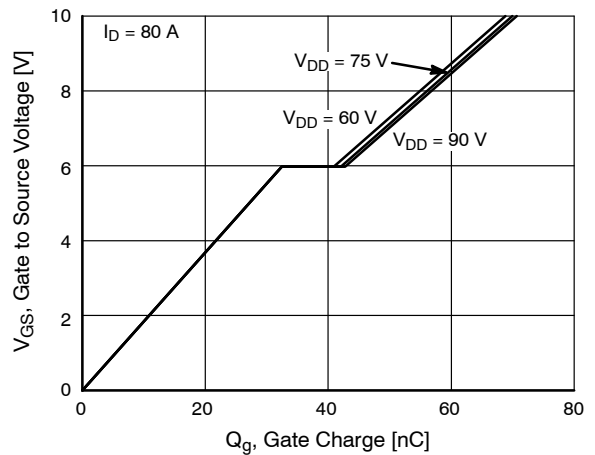
Figure 16. Gate Charge vs. Gate to Source Voltage

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H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE A

DATE 06 JAN 2020

EJECTOR
PIN MARK

E2
D3
E3 (2X)
E
D
L2
PIN 1
AREA
e/2
e
1
8
b (8X)
z
e1

TOP VIEW

DETAIL "A"

B

E1

aaa(M) C A B

SIDE VIEW

bbb(M) C A B
ddd(M) C

c

Θ

DETAIL "A"
SCALE: 2X

SEE DETAIL "B"

A3

Θ

ccc C

A

eee C

FRONT VIEW

c1

DETAIL "B"
SCALE: 2X

SEATING PLANE

C

aaa(M) C A B

A

D1

b1

1

8

E10

D2 (2X)

0.10

E4 (2X)

E8

E9

E7

E5 (2X)

E6 (2X)

D5 (3X)

D4

D6

D7

BOTTOM VIEW

L
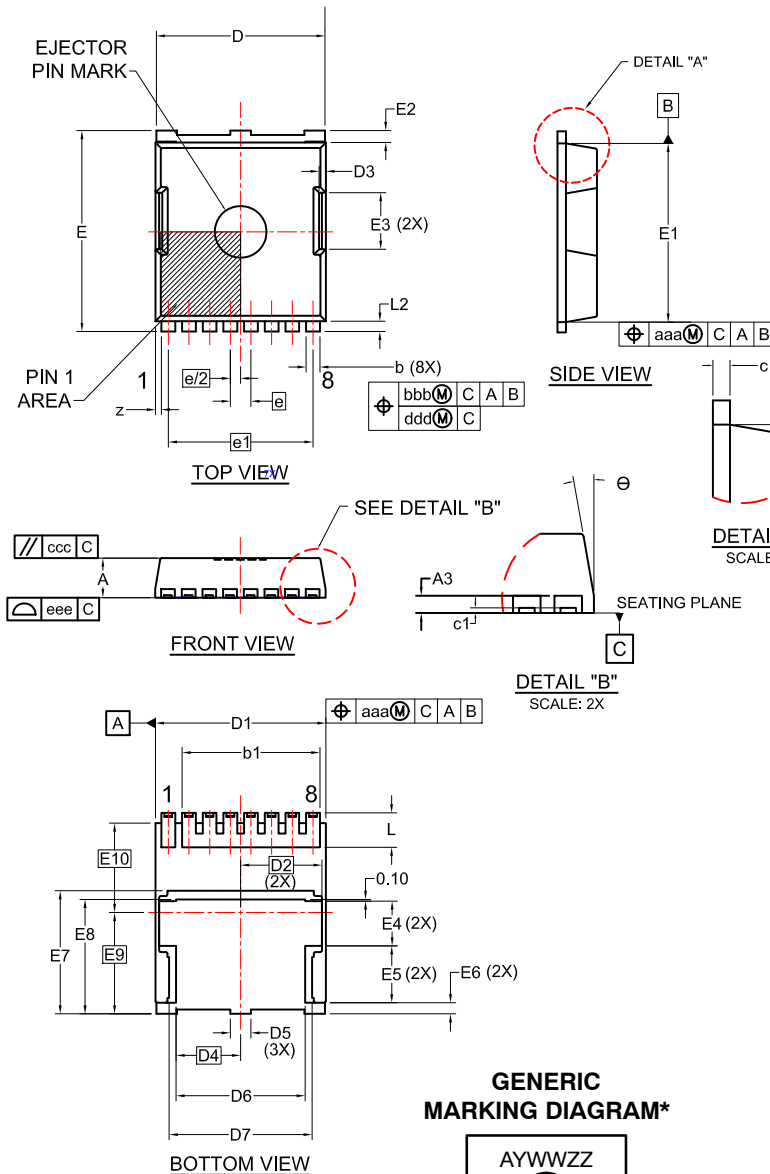
LAND PATTERN
RECOMMENDATION

10.20
5.10
4.45
6.64
4.99
2.04
1.46
6.64
0.86
0.80
2.95
8.10
2.90
13.28
0.60
2.80
1
8
1.20

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE
STRATEGY AND SOLDERING DETAILS, PLEASE
DOWNLOAD THE ON SEMICONDUCTOR SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE
TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH,
PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS
DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE
LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A3	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	—	1.20	---
D6	7.40	7.50	7.60
D7	(8.30)		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	—	2.60	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	1.50	1.57	1.70
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
Θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		
E5	---	3.30	—
E6	---	0.65	—
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		

**GENERIC
MARKING DIAGRAM***

AYWWZZ
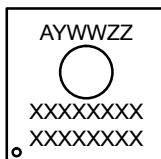
XXXXXXXX
XXXXXXXX

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "■", may
or may not be present. Some products may
not follow the Generic Marking.

DOCUMENT NUMBER:	98AON13813G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	H−PSOF8L 11.68x9.80		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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