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FDC30N20DZ

Dual N-Channel PowerTrench[®] MOSFET

30 V, 4.6 A, 31 mΩ

Features

- Max $r_{DS(on)}$ = 31 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 4.6\text{ A}$
- Max $r_{DS(on)}$ = 38 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 4.2\text{ A}$
- High Performance Trench[®] Technology for Extremely Low $r_{DS(on)}$
- Fast Switching Speed
- 100% UIL Tested
- Typical CDM ESD protection level > 2.0 kV (Note 5)
- RoHS Compliant

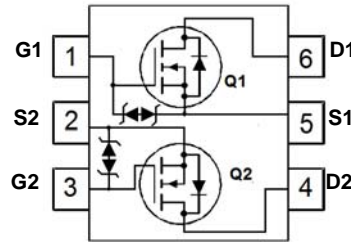
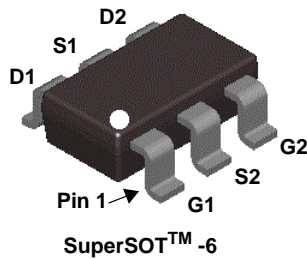


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Load Switch
- Synchronous Rectifier



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Note 1a)	4.6	A
	-Pulsed (Note 4)	30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	3	mJ
P_D	Power Dissipation (Note 1a)	0.96	W
	Power Dissipation (Note 1b)	0.69	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	130	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	180	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.30N20	FDC30N20DZ	SSOT-6	7"	8 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 4.6\text{ A}$		23	31	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 4.2\text{ A}$		27	38	
		$V_{GS} = 10\text{ V}, I_D = 4.6\text{ A}, T_J = 125\text{ }^\circ\text{C}$		31	42	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 4.6\text{ A}$		23		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		356	535	pF
C_{oss}	Output Capacitance			110	165	pF
C_{rss}	Reverse Transfer Capacitance			18	30	pF
R_g	Gate Resistance		0.1	3.5	7.0	Ω

Switching Characteristics

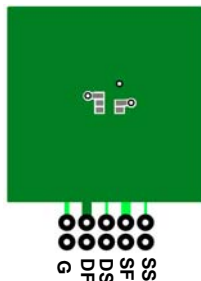
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 4.6\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6	12	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			13	21	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		5.6	7.9
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	$V_{DD} = 15\text{ V},$ $I_D = 4.6\text{ A}$	2.7	3.8	nC
Q_{gs}	Gate to Source Charge			0.9		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.8		nC

Drain-Source Diode Characteristics

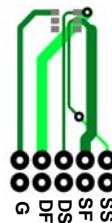
V_{SD}	Source-Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 4.6\text{ A}$ (Note 2)		0.85	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 4.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		10	20	ns
Q_{rr}	Reverse Recovery Charge			2	10	nC

NOTES:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $130\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $180\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.
- E_{AS} of 3 mJ starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 0.1\text{ mH}, I_{AS} = 8\text{ A}, V_{DD} = 27\text{ V}, V_{GS} = 10\text{ V}$.
- Pulse I_d measured at $t_d \leq 250\text{ }\mu\text{s}$, refer to SOA graph for more details.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

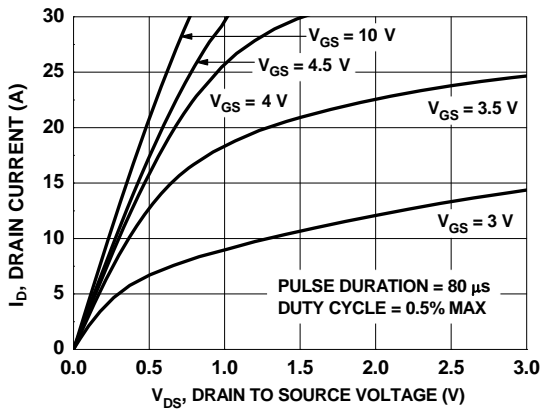


Figure 1. On-Region Characteristics

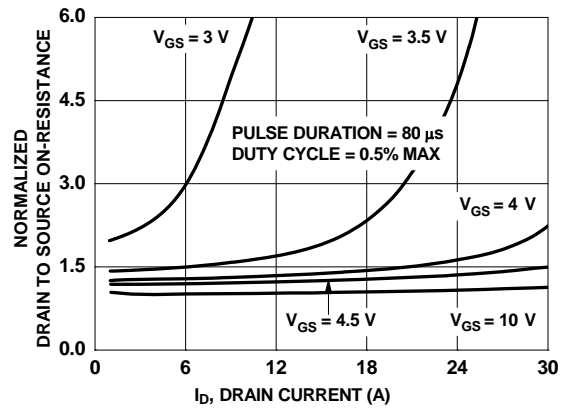


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

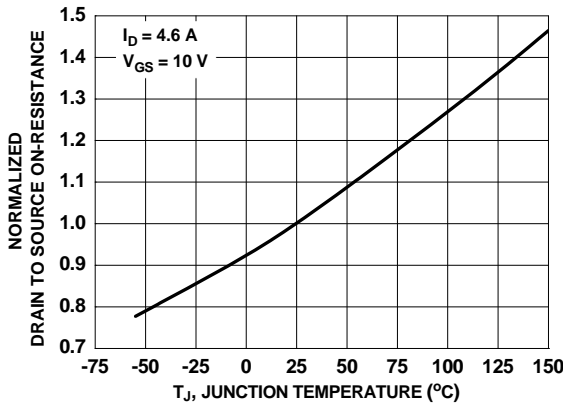


Figure 3. Normalized On-Resistance vs. Junction Temperature

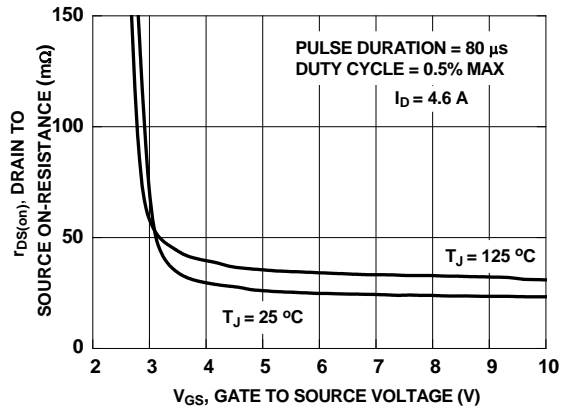


Figure 4. On-Resistance vs. Gate to Source Voltage

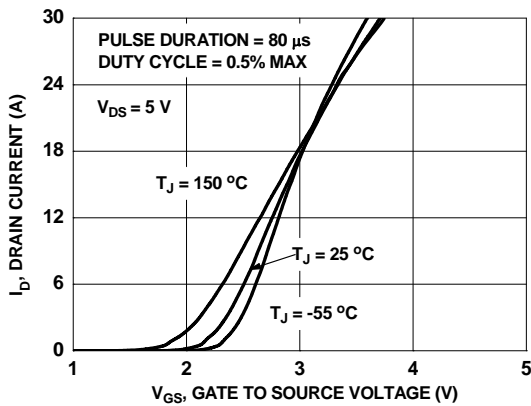


Figure 5. Transfer Characteristics

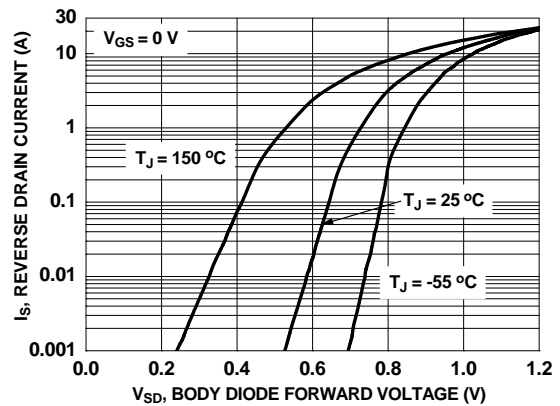


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

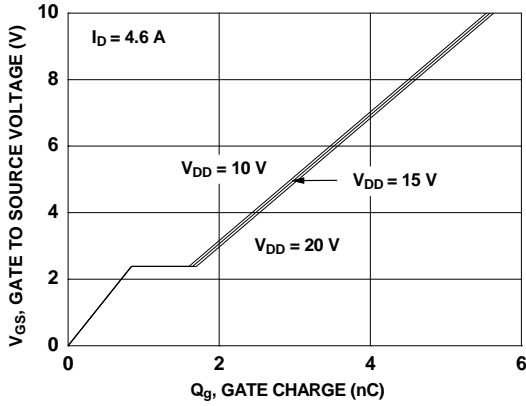


Figure 7. Gate Charge Characteristics

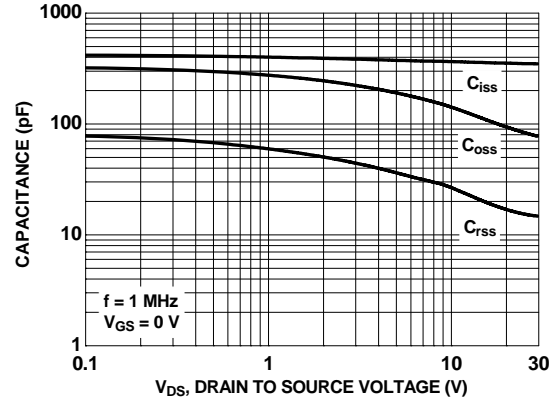


Figure 8. Capacitance vs. Drain to Source Voltage

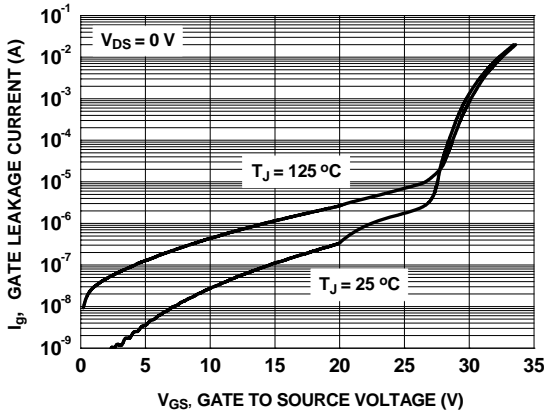


Figure 9. Gate Leakage Current vs Gate to Source Voltage

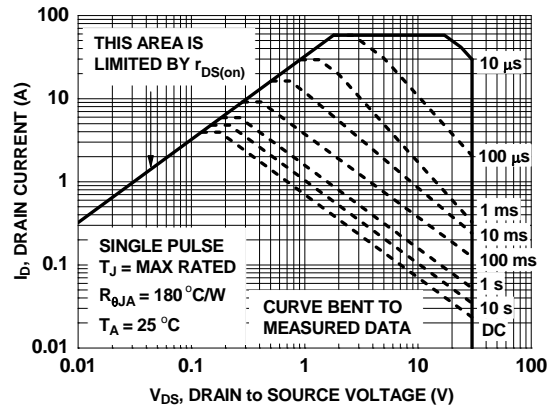


Figure 10. Forward Bias Safe Operating Area

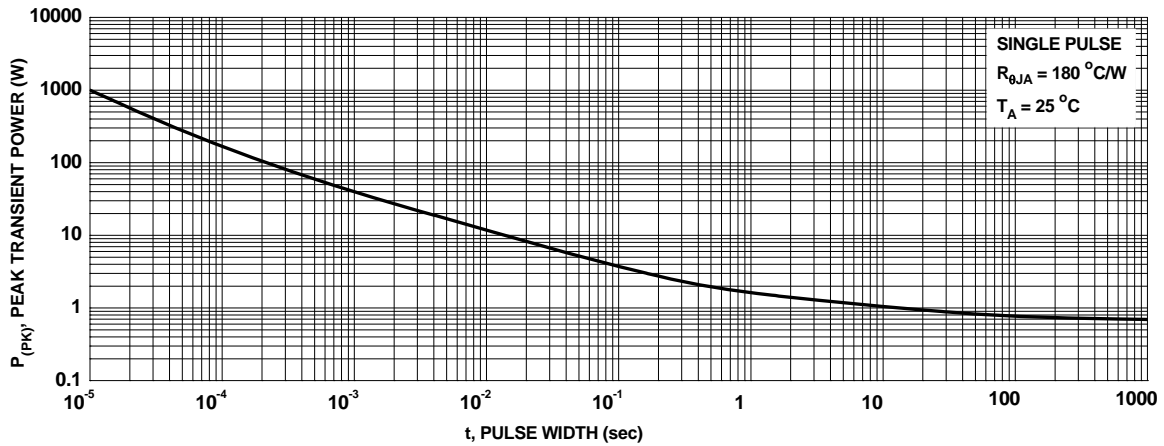


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

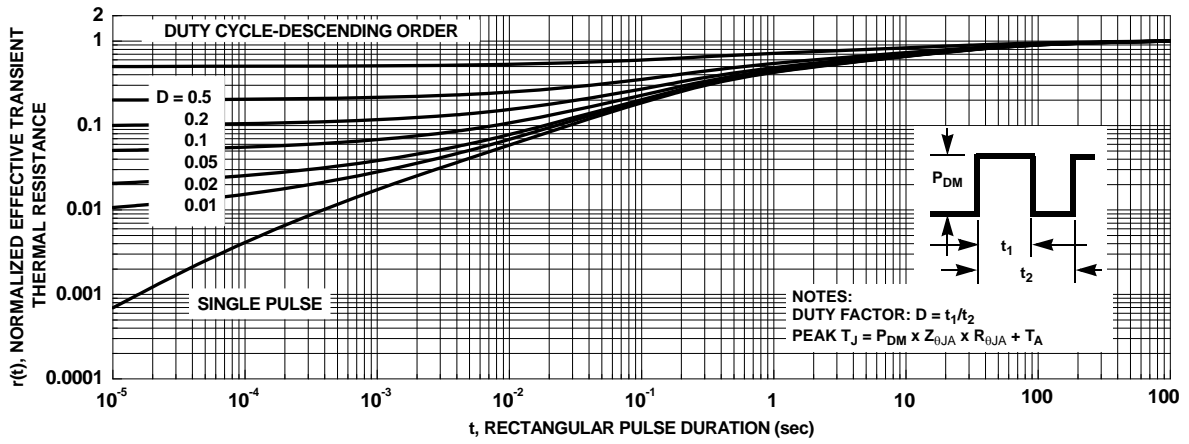
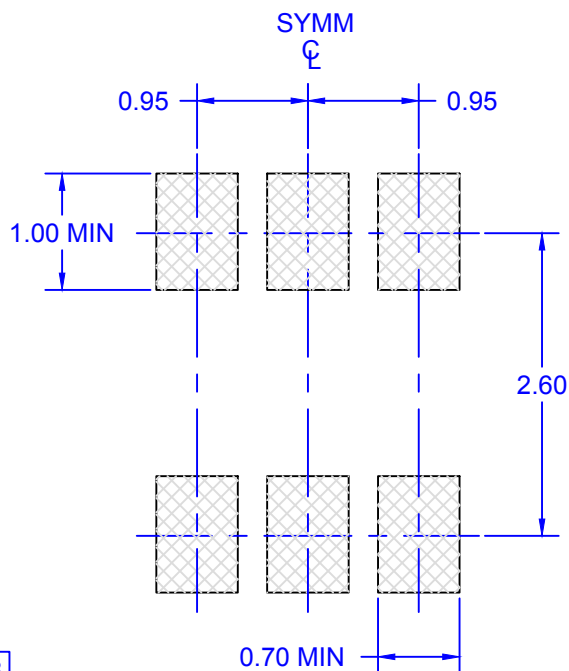
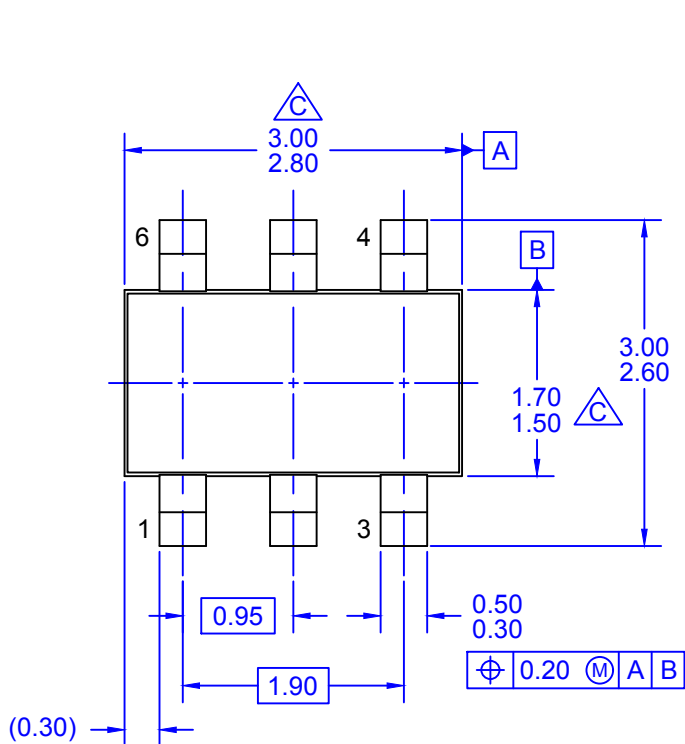
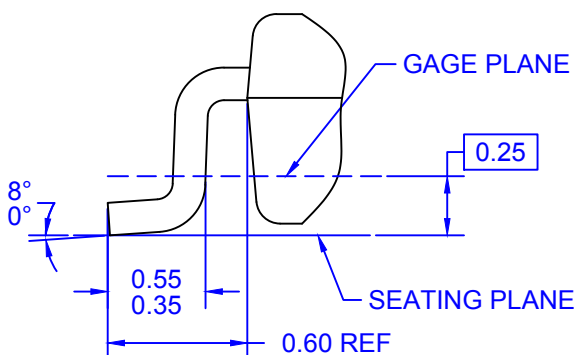
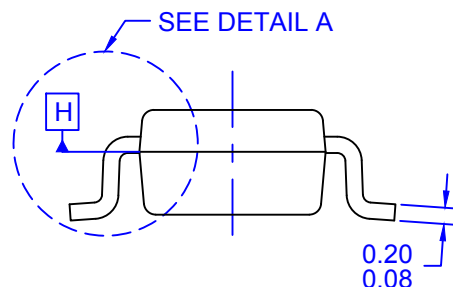
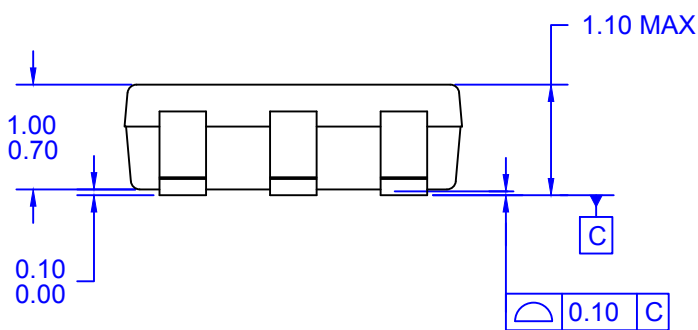


Figure 12. Junction to Ambient Transient Thermal Response Curve



LAND PATTERN RECOMMENDATION



DETAIL A
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- NOTES: UNLESS OTHERWISE SPECIFIED
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 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25mm PER END. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS ARE DETERMINED AT DATUM H.
 - D) DRAWING FILE NAME: MKT-MA06AREVF

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